Analog Circuit Test Based on a Digital Signature

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***Abstract*—Production verification of analog circuit specifications is a challenging task requiring expensive test equipment and time consuming procedures. This paper presents a method for low cost on-chip parameter verification based on the analysis of a digital signature. A 65 nm CMOS on-chip monitor is proposed and validated in practice. The monitor composes two signals $(x(t), y(t))$ and divides the X-Y plane with nonlinear boundaries in order to generate a digital code for every analog (x, y) location. A digital signature is obtained using the digital code and its time duration. A metric defining a discrepancy factor is used to verify circuit parameters. The method is applied to detect possible deviations in the natural frequency of a Biquad filter. Simulated and experimental results show the possibilities of the proposal.**

***Index Terms*—Mixed-Signal Test, Specification Verification, Monitoring, Nonlinear Zone Boundary.**

I. Introduction

As circuit complexity increases, internal signals become more embedded into the structure, making their tracking from IC's primary inputs/outputs difficult [1], [2].

Analog and mixed-signal parameter validation procedures highlight the divorce between current technologies and available test methods. The conditions attached to traditional specification based tests are manual, expensive and time consuming procedures which are applied to costly analog automatic test equipment (AATE). Built-in monitoring of analog signals, together with on-chip digital signature generation, aims to meet these challenges [3], [4].

A number of test techniques have been proposed. Oscillation based test (OBT) is widely accepted and has been lately expanded by several authors [5], [6]. Transient testing compares fault-free patterns with some characteristics of the CUT response to a simple stimulus [7], [8]. Some catastrophic structural fault based tests look for the best stimuli to excite the fault, typically shorts and opens. However, in many situations, fault-free does not mean specifications compliant, in particular with process variations in nanometric technologies [9]. Alternate test methods [10], [11] try to meet these analog test challenges by mapping easy-to-measure circuit parameters to circuit specifications by regression techniques. For test purposes, X-Y zoning uses straight lines to divide the plane into zones in order to monitor signal compositions (Lissajous curves) [12], [13]. Recently, a generalization of the monitoring method for multiple variables has been proposed. The study is based on Lissajous compositions in a CUT with multitone excitation [14].

Several approaches using oscillation test method [6], alternate test [11], and zoning [13], [14], have been used in combination with BIST techniques, yielding promising results in analog and mixed-signal applications.

The paper describes: (a) a CMOS digital signature generator based on X-Y zoning and (b) a test method based on the definition of a discrepancy factor which quantifies the difference between golden digital signatures and the monitor-generated signatures.

The paper is organized as follows. Section II presents the X-Y zoning method, its possibilities and benefits in circuit testing. Section III introduces the proposed signature generator structure and provides an on-chip nanometric implementation and some preliminary experimental results. Section IV is devoted to signature comparison through the discrepancy factor and its direct application to testing a Biquad filter. Section V summarizes the work and draws some conclusions.

II. X-Y Zoning Method Description

In the X-Y zone testing method, signal monitoring is based on the composition of two circuit signals, $x(t)$ and $y(t)$, in a similar way as an oscilloscope in X-Y mode represents the trace on the screen. If the frequency ratio of the periodic signals is rational, the resultant curve is also periodic, thus becoming the well-known Lissajous curve.

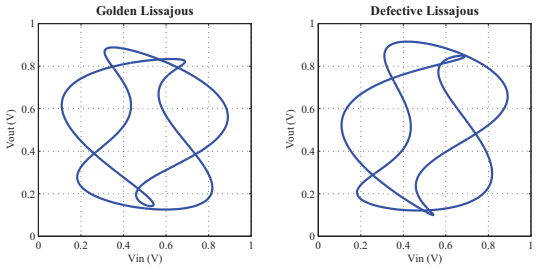

Fig. 1. Lissajous composition of a multitone input signal and the low pass output of a Biquad filter. Nominal shape (left) and 10% shift in the natural frequency of the filter (right).

In previous work on monitoring signals in the X-Y plane [12], [15], the plane is devided by straight lines that delimit the zones. As an example of application, the output of a low pass filter is plotted as a function of its multitone input, generating the Lissajous curve of the CUT. The nominal fault-free curve is represented on the left side of Fig. 1. On the right, the Lissajous curve with parameters of the filter out of specification tolerance is shown. In this way, a large set of parametric and catastrophic defects can be detected just by checking whether the Lissajous curve remains in the specified zones. Using multiple partitions, the digital code of the zones traversed by the Lissajous curve with the time interval spent by the Lissajous curve to traverse the zone becomes the digital signature of the circuit.

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Straight lines are implemented in the X-Y plane using weighted adders and comparators. Several monitors have been proposed in the past for this purpose [13], [14]. In these approaches, Lissajous curves were previously studied to select the best X-Y partitions delimited by such lines. In order to simplify the monitors, non-straight boundaries have recently been proposed for the X-Y zones [15]. This method takes advantage of the nonlinear dependence of the nMOS transistor drain current I_{D} as a function of its gate-source voltage V_{GS}. The benefits are circuit simplification and significant reduction in monitor size.

In this work we present an efficient method for digital signature generation and a metric for analog parameter verification.

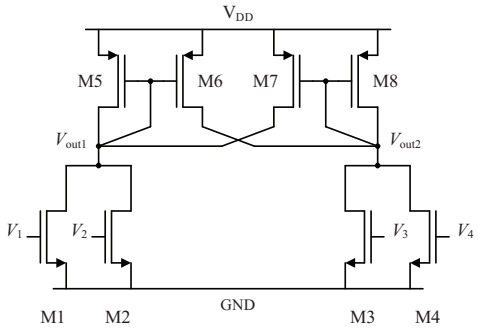

Fig. 2. Monitor circuit based on current comparison.

III. Monitor for Digital Signature Generation

Current comparison is a straightforward way to implement control curves by composing two or more voltage signals. In contrast with voltage comparison, addition and substraction of currents (Kirchhoff's law) allows the use of very simple structures. Furthermore, in CMOS applications, the quasi-quadratic current-voltage characteristic of MOS transistors in saturation enables the implementation of nonlinear curves to delimit zones in the X-Y plane.

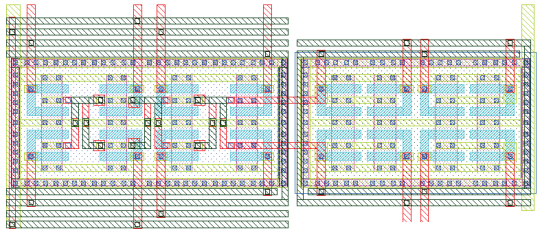

Fig. 3. Layout of the monitor in Fig. 2. It is implemented in STMicroelectronics 65 nm CMOS technology. The occupied area is $53.54\,\mu\mathrm{m}^2$.

A. Circuit Design

In order to compare currents, we propose the differential input stage of Fig. 2. In this implementation, four input signals are used, even though the structure can be generalized by simply adding transistors in parallel.

This circuit with only two nMOS input transistors is the well-known "Source grounded differential pair" or "Pseudo differential pair" [16]. For the pMOS, equal sized transistors M5 and M8 are used as active loads, while equal sized transistors M6 and M7 perform the required feedback to improve the gain of the stage.

As can be seen in Fig. 2, the input signals (V_1 to V_4) are directly connected to the gate of nMOS transistors (M1 to M4 respectively), which deliver the current to be added at each side of the differential input stage. Every transistor current is selected according to the required curve parameters by adequately sizing the input transistor dimensions (W/L).

The layout of the proposed monitor, implemented in STMicroelectronics 65 nm CMOS technology, is shown in Fig. 3. In this design, the transistors are split into four to balance the structure and thus satisfy two-dimension common-centroid strategies [17]. The area overhead is $53.54\,\mu\mathrm{m}^2$ ($11.64\,\mu\mathrm{m} \times 4.6\,\mu\mathrm{m}$). The design also includes a high gain output stage to digitalize the differential output of the monitor. The total area used per monitor is $116.1\,\mu\mathrm{m}^2$.

B. Control Curves

As can be observed in Table I, by interchanging positions of the four input voltages, curve shape and location are controlled. Fig. 4 shows the experimental curves for the configurations in Table I. Results lie in the predicted range for Monte Carlo simulations using the foundry technology statistical characterization.

Table I
Input configuration for the curves in Fig. 4

	Transistor widths (nm) ($L = 180$ nm)				Applied input voltages (V)			
	M1	**M2**	**M3**	**M4**	V_1	V_2	V_3	V_4
1	3000	600	600	3000	Y axis	0.2	X axis	0.6
2	3000	600	600	3000	0.6	Y axis	0.2	X axis
3	1800	1800	1800	1800	Y axis	X axis	0.55	0.55
4	1800	1800	1800	1800	Y axis	X axis	0.3	0.3
5	1800	1800	1800	1800	Y axis	X axis	0.75	0.75
6	1800	1800	1800	1800	Y axis	0	X axis	0

Comparing voltages V_1 and V_3 (one signal at each side of the differential pair) and setting V_2 and V_4 to a DC level, the resulting curves are segments of positive slope (curves 1 and 2 in Fig. 4). If both sides are symmetrical (transistor aspect ratio and constant voltages) we obtain a straight line cutting the plane at 45 degrees (curve 6). The distortion of curve 6 for small input voltages is caused by the subthreshold operation of the nMOS transistors.

When both voltages in one branch of the differential pair (V_3, V_4) are connected to DC levels, V_1 and V_2 are nonlinearly added, generating segments of negative slope as shown in curves 3 to 5. Boundary curves become a straight line for input voltages below the threshold voltage because the input transistors do not deliver current to the addition.

IV. Digital Signature

A. Signature Definition

The zones in the X-Y plane are codified so that every monitor delivers a digital "0" for the region containing the

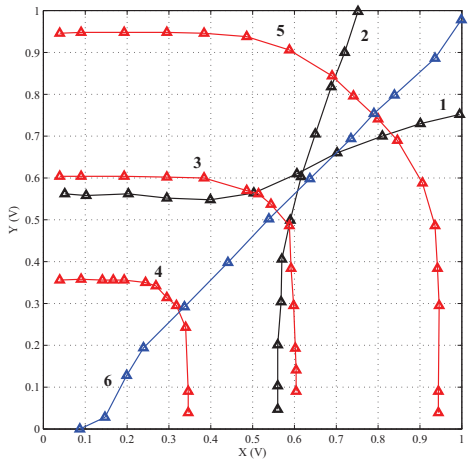

Fig. 4. Experimental control lines of TABLE I obtained for the monitor fabricated using STMicroelectronics 65 nm CMOS technology.

origin, and a digital "1" otherwise. The resulting zones and codes are shown in Fig. 4 and Fig. 6.

The signature of a CUT is defined as the sequence of pairs of zone code (Z_i) and time interval of permanence of the CUT's signals in the zone (Δ_i).

Formally, if the periodic Lissajous curve crosses k zones, $Z_1, Z_2, \ldots, Z_k$, and the time duration in each zone is denoted as Δ_i, $\forall i = 1, \ldots, k$, the CUT's signature is defined as,

$$\text{SIGNATURE} \equiv \{(Z_1, \Delta_1), (Z_2, \Delta_2), \ldots, (Z_k, \Delta_k)\}. \quad (1)$$

Monitor outputs are processed by an asynchronous capture which generates the digital signature. The implementation is illustrated in Fig. 5, where an m-bit counter holds the time between code captures.

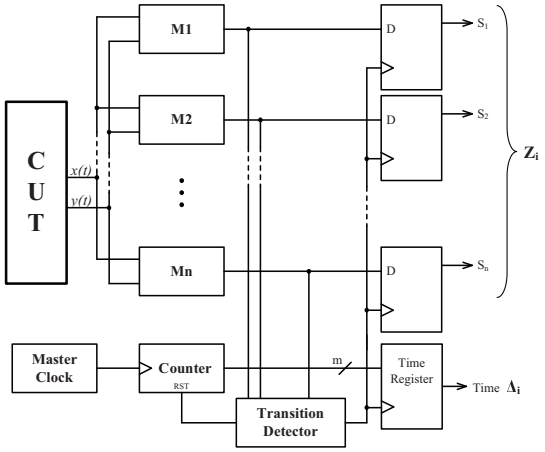

Fig. 5. Block diagram for asynchronous capture of digital signatures generating n-bit zone codes and m-bit time intervals.

In Fig. 6, the golden and +10% f_0 shift Lissajous curves evolve across the X-Y plane traversing different zones, delimited by nonlinear control curves, at different instants and thus generating different signatures.

Using the capture circuit of Fig. 5, the signatures of Fig. 7 are obtained for the defective and the defect-free curves. The chronogram in Fig. 7 shows the zone code for any time t within the period of the Lissajous curves.

B. Metric Definition

An indicator of signature discrepancies is required. We obtain it by defining the so-called normalized discrepancy factor as

$$\text{NDF} = \frac{1}{T}\int_0^T \mathrm{d_H}(S_O, S_G)\, dt, \quad (2)$$

where functions $S_O(t)$ and $S_G(t)$ respectively represent the observed defective and golden signatures defined within the period T of the Lissajous curves. Operator $\mathrm{d_H}()$ is the Hamming distance of the zone codes at each time instant. The NDF parameter indicates the discrepancy of the defective and golden instantaneous codes weighted by the duration of the time interval in which the Lissajous curve remains in the same zone.

The previous definition matches the average value of the Hamming distance chronogram over the interval $[0, T]$. For the example of Fig. 7, an NDF of 0.1021 is obtained.

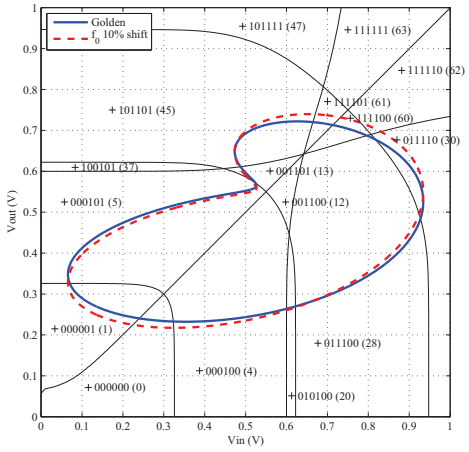

Fig. 6. Control curves with zone codification and Lissajous compositions: golden and +10% shift in f_0.

According to the zone codification criterion, neighbouring zones only differ in one bit. This is why the Hamming distance is suitable, as can be observed in the lower chronogram of Fig. 7, where the Hamming golden-defect distance is plotted over a period. Note a Hamming distance of 2 in the interval $[48, 50]\,\mu$s (see Fig. 6) resulting from the faulty trace which reaches zone $111110_2\,(62_{10})$ instead of the sequence $011110_2\,(30_{10})$, $011100_2\,(28_{10})$, $111100_2\,(60_{10})$, which defines a defect-free Lissajous.

C. Parameter Verification Process

The NDF is used to evaluate the amount of deviation of the parameters under verification. Circuits with parameters meeting specifications are expected to have small NDF values. To evaluate the NDF effectiveness, extensive software simulations were performed on a Biquad filter circuit with

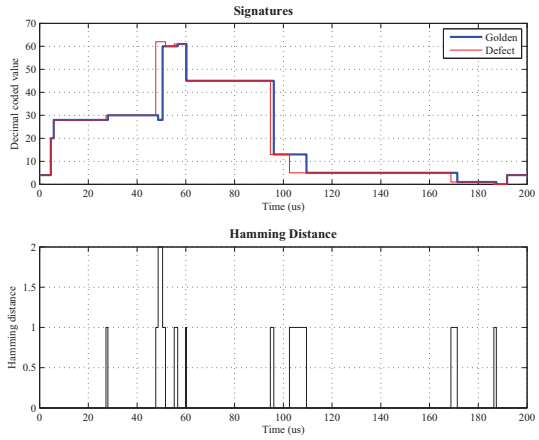

Fig. 7. Chronogram of digital signatures and Hamming distances for +10% shift in the f_0 parameter of a Biquad filter. NDF = 0.1021.

different degrees of deviation in the natural frequency of the filter. The discrepancy factor increases almost linearly with the amount of deviation and quite symmetrically with positive and negative f_0 parameter deviations, as can be seen in Fig. 8. The test decision is made by previously setting the desired level of tolerance and checking whether the NDF lies in the acceptance or rejection bands. Simulations conducted with high frequency white noise on the signals with null mean and a 3σ spread of $0.015\,\mathrm{V}$ show that deviations as low as 1% in the natural frequency of the filter are detected.

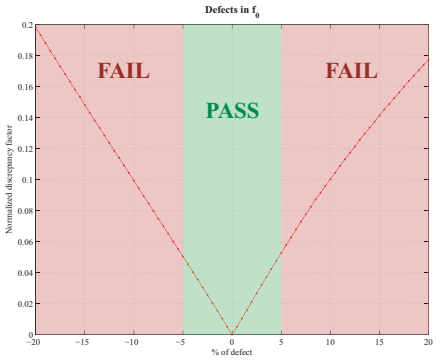

Fig. 8. Normalized discrepancy factor for defects in f_0.

V. Conclusions

In order to test analog circuits with two observable signals, we define a metric to compare digital signatures using the Hamming distance between the golden and CUT zone codes. A normalized discrepancy factor (NDF) characterizing the amount of parameter deviation is defined as the average value of the Hamming distance of the digital zone codes weighted by the time duration of each code. The test decision is made by mapping the discrepancy factor and the amount of deviation related to the acceptable band, as indicated in Fig. 8.

A low cost X-Y zoning monitor was designed and fabricated in STMicroelectronics 65 nm technology. The monitor is based on a four input current comparator followed by a high gain stage. The monitor divides the X-Y plane with nonlinear boundaries into zones to generate a digital output for each analog (x, y) location. Zone boundaries can be adjusted by changing the biasing voltages and/or the aspect ratio of the input transistors. Experimental measurements of the monitor zone boundaries were performed, yielding results in the range of the predicted Monte Carlo simulations values (process and mismatch) for STMicroelectronics 65 nm technology variability.

The method was applied on a Biquad Filter circuit to test the natural frequency parameter.

Acknowledgments

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