

A New Digital Predictive Predistorter for Behavioral Power Amplifier Linearization

G. Montoro, P. L. Gilibert, E. Bertran, *Senior Member, IEEE*, A. Cesari, and D. D. Silveira

Abstract—This letter presents a new digital adaptive predistorter (PD) for power amplifier (PA) linearization based on a nonlinear auto-regressive moving average (NARMA) structure. The distinctive characteristic of this PD is its straightforward deduction from the NARMA PA model, without the need of using an indirect learning approach to identify the PD function. The PD itself presents a NARMA structure, and hence it can be quickly implemented by means of lookup tables. Single and multicarrier modulated signals collected from a three-stage LDMOS class AB PA, with a maximum output power of 48-dBm CW have been used to validate the linearity performance of this new predictive predistorter.

Index Terms—Amplifier distortion, digital predistorter (PD), digital radio, direct learning approach, linearization, microwave power amplifiers (PAs), nonlinear auto-regressive moving average (NARMA), radio transmitters.

I. INTRODUCTION

CURRENT personal communication standards use spectrally efficient multilevel modulation formats which are very sensitive to the intermodulation distortion that results from nonlinearities in the radio frequency (RF) transmitter chain. Moreover, the need to support multi-user operation and/or multipath environments (spread spectrum or multicarrier modulations) results in RF signals at the power amplifier (PA) input exhibiting high peak to average power ratios (PAPR). This leads to a PA efficiency degradation since significant back-off levels are required in order to have linear amplification, unless a linearizer is deployed.

Among linearizers, digital predistortion (PD) takes advantage of the already existing digital signal processing (DSP) devices in transmitters (to cope with signal coding and protection required in modern standards), thus reducing the RF hardware adjustment problems. However, since modern communication standards present significant bandwidths (i.e., 20–28 MHz in WiMAX), memory effects have to be taken into account to avoid degradation in PD linearity performance.

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G. Montoro, P. L. Gilibert, and E. Bertran are with the Department of Signal Theory and Communications, Technical University of Catalonia (UPC), Barcelona 08860, Spain (e-mail: montoro@tsc.upc.edu; plgilibert@tsc.upc.edu; bertran@tsc.upc.edu).

A. Cesari is with the Department of Intégration de Systèmes de Gestion de l’Energie (LAAS-CNRS), Toulouse 31077, France (e-mail: acesari@laas.fr).

D. D. Silveira is with the Institute of Electrical Measurements and Circuit Design, Vienna University of Technology (TUW), Vienna A-1040, Austria (e-mail: daniel.silveira@tuwien.ac.at).

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Therefore, when designing digital PD, at least two significant issues have to be taken into account. The first one is to have accurate PA behavioral models capable to fit with current necessities (in terms of BW, PAPR, and memory effects reproduction). The second one regards the simplicity of these models, since they have to be invertible and finally implemented in digital processing devices (DSPs or FPGAs) without an excessive computational cost that permits more frequent updates of the predistortion function.

A general overview on the usual PA behavioral models used in literature is presented in [1]. Full Volterra series and Neural Networks are typically limited to PA behavioral modeling, because of their computational complexity in a digital PD application. The most usual models employed for digital PD are: memory polynomials or nonlinear moving average (MA) models [2], [3], Hammerstein [4], [5], and Wiener [6], [7] models with their cascade and parallel variants and using finite or infinite impulse response (FIR or IIR) filters to model the linear time invariant block.

The estimation of the predistorter function is commonly made by using the indirect learning approach or postdistortion and translation method (e.g., [3], [4], and [8]). However, this method assumes the commutative property for cascading nonlinear systems, which is not rigorous at all, despite the good results shown by this method regarding linearity improvement.

This letter presents a digital adaptive predistorter with a nonlinear auto-regressive moving average (NARMA) structure whose parameters can be easily obtained from a closely related NARMA model of the PA. This kind of model embeds both linear and nonlinear parts, thus avoiding a cascaded linear–nonlinear decomposition as in Hammerstein or Wiener models. In practice, the NARMA PD is well suited for being implemented by using simple lookup tables (LUTs). The adaptation process of the proposed PD relies just on the PA NARMA model, and its stability, despite its nonlinear feedback structure, may be assessed and ensured.

II. PREDICTIVE PREDISTORTION SYSTEM DESCRIPTION

The digital predictive predistortion system here presented follows the block diagram shown in Fig. 1, where digital predistortion linearization is carried out at baseband by adaptively forcing the PA to behave as a linear device. The functioning of the digital PD is quite simple and intuitive. First it is necessary to perform an identification of the low-pass complex envelope PA behavioral model, from which a first set of coefficients defining the PA behavior are calculated at baseband using the PA input (x_A) and output (y_A) discrete complex envelope data.

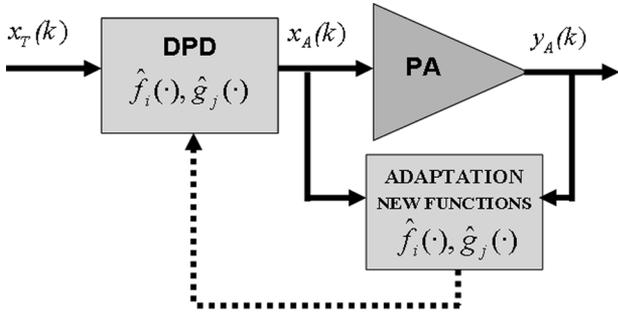


Fig. 1. Predistorter block scheme.

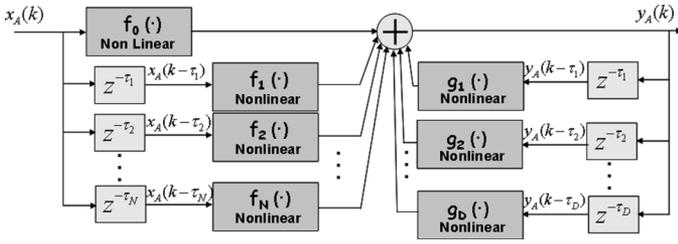


Fig. 2. General block diagram of a NARMA structure.

The first contribution developed in this letter is to consider a kind of NARMA structure (see Fig. 2) to identify the PA low-pass complex envelope behavioral model.

The output of this NARMA PA behavioral model is described in

$$y_A(k) = \hat{f}_0(x_A(k)) + \sum_{i=1}^N \hat{f}_i(x_A(k - \tau_i)) - \sum_{j=1}^D \hat{g}_j(y_A(k - \tau_j)) \quad (1)$$

where \hat{f}_i and \hat{g}_j are estimated nonlinear functions that can be implemented with power series or by using lookup tables (LUTs), as it will be discussed later in this letter. In addition, τ_i and τ_j ($\tau \subset N$) are the most significant delays of the input and the output, respectively, contributing at describing the PA memory effects. The process to extract these optimal delays is explained in [5], while a condition that ensures its inherent stability is presented in [8]. It is important to identify the PA behavior model attending the tradeoff between computational complexity and model accuracy.

Once we have identified the \hat{f}_i and \hat{g}_j nonlinear functions describing the PA behavioral model, we now consider y_D as the desired linearised PA output. It is defined as the signal to be transmitted (x_T) multiplied by a linear gain (G_{linear})

$$y_D(k) = x_T(k) \cdot G_{\text{linear}}. \quad (2)$$

As shown in Fig. 1, $x_A(k) = x_T(k)$ if no baseband predistorter is considered. From (1) it is possible to derive

$$\hat{f}_0(x_A(k)) = y_A(k) - \sum_{i=1}^N \hat{f}_i(x_A(k - \tau_i)) + \sum_{j=1}^D \hat{g}_j(y_A(k - \tau_j)) \quad (3)$$

and solving (3) it is possible to obtain the necessary amplifier input $x_A(k)$ in order to achieve a certain output $y_A(k)$. Since the

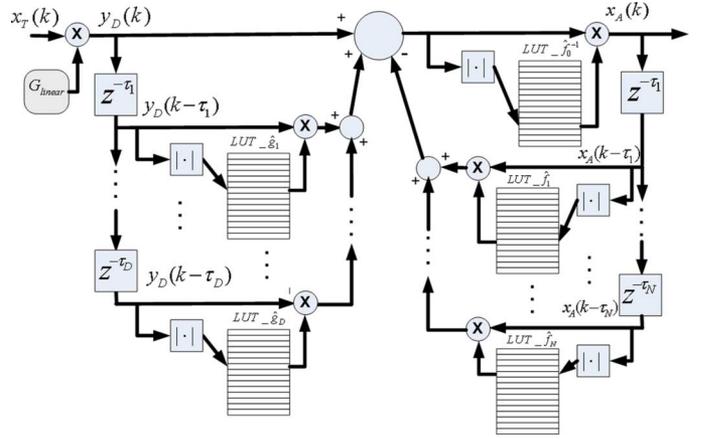


Fig. 3. Predictive (PD) implementation with LUTs.

desired output $y_D(k)$ is evaluated *a priori* [see (2)], then in (3) we can replace y_A by y_D (and the same for all delayed output samples). In other words, we consider $y_D(k)$ (desired output) as a prediction of the future value of $y_A(k)$ (current output) and consequently, we calculate the input value of the PA $x_A(k)$ that permits achieving the desired output, $y_A(k) = y_D(k)$. Finally, the digital PD output $x_A(k)$ (and PA input) can be expressed as

$$x_A(k) = \hat{f}_0^{-1} \left(y_D(k) - \sum_{i=1}^N \hat{f}_i(x_A(k - \tau_i)) + \sum_{j=1}^D \hat{g}_j(y_D(k - \tau_j)) \right). \quad (4)$$

Then, the adaptive process followed by this digital adaptive predistorter in order to perform the PA linearization consists in the following.

- 1) In a first step, identifying new \hat{f}_i and \hat{g}_j nonlinear functions, as described in (1)—see also Fig. 2—by monitoring current PA input (x_A) and output (y_A) samples, as it is shown in Fig. 1.
- 2) Second step: test the stability of both PA and digital PD NARMA models (bounds given by the small-gain theory [8]).
- 3) The third step consists in inverting the \hat{f}_0 nonlinear function since it is necessary to find the digital PD output as it is shown in (4).
- 4) The last step consists in generating all necessary LUTs contents to implement the predistorter function described in (4). And then back to step 1.

III. LOOKUP TABLE PREDISTORTION IMPLEMENTATION

The LUT based implementation of the predictive digital predistorter described in this letter is shown in Fig. 3. Each nonlinear function (\hat{f}_i , \hat{g}_j , \hat{f}_0^{-1}) is implemented with a LUT.

This configuration permits a FPGA implementation relaxing the computational effort related to the nonlinear functions implementation and, in addition, permits scalability, that is, adding or reducing the number of delays considered in the predistorter structure.

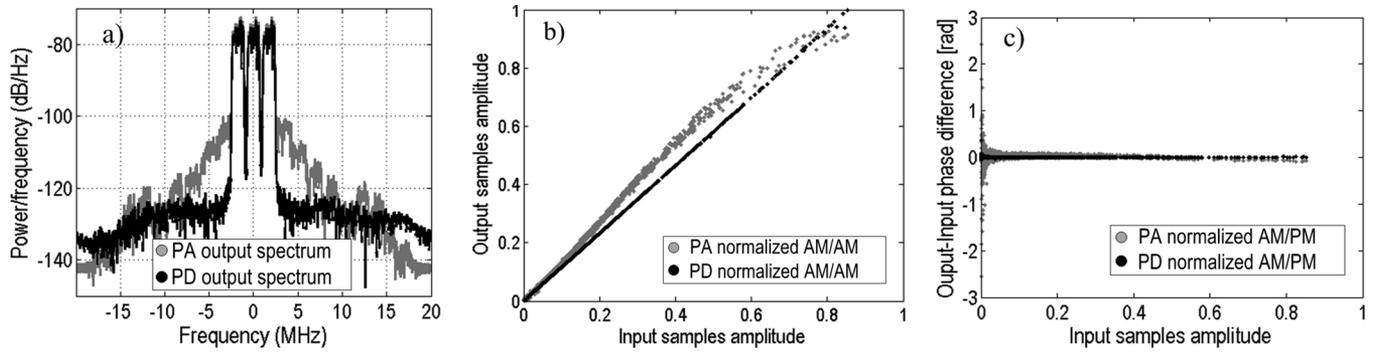


Fig. 4. PA and linearized: (a) output spectra; (b) AM/AM characterization; and (c) AM/PM characterization; for a 3xIS95 signal.

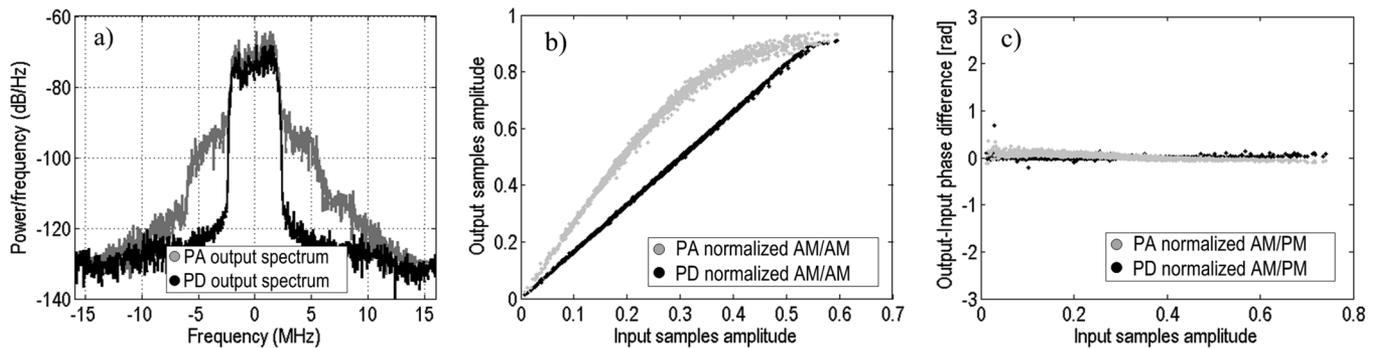


Fig. 5. PA and linearized: (a) output spectra; (b) AM/AM characterization; and (c) AM/PM characterization; for a WCDMA signal.

IV. PREDISTORTION RESULTS

In order to test the predictive predistorter we have assessed the predistortion adaptive function in Matlab, using measured data to identify the PA and later validate the adaptive predistorter. The PA used is a LDMOS three-stage class AB main amplifier (final stage transistor Motorola MRF 18090B), 36 dB of gain, 1-dB compression point at 48 dBm and $IP_3 = 53$ dBm. The data were measured at a central frequency of 1.96 GHz. The two kinds of data considered are:

- 3xIS95 channels, 4.8-MHz bandwidth (9-dB IBO);
- WCDMA channel, 5-MHz bandwidth (0-dB IBO).

In order to check its adaptability 50 bursts of modulated data with 2048 samples per burst were considered. Figs. 4 and 5 show the PA and PD normalized output power spectra, the normalized AM/AM and the AM/PM curves for both 3xIS95 and WCDMA data. The predistorter specifications for both kinds of data are:

- 3xIS95 PD: four input delays and one output delay, total number of LUTs = 6. ACPR reduction of 20 dB;
- WCDMA PD: four input delays and one output delay, total number of LUTs = 6. ACPR reduction of 20 dB.

V. CONCLUSION

This new digital PD configuration is easy to implement, more robust than the ones using indirect learning approach, and presents better ACPR reduction. Moreover, data blurring in AM/AM and AM/PM due to short term memory effects are

compensated (long term memory effects are not of concern in adaptive systems). The LUT configuration reduces complexity in the implementation and permits scalability in order to meet the tradeoff between complexity and PD accuracy.

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