Effect of the interfacial dipole layer based on cysteine on the electrical characteristics of organic Thin-Film Transistors*

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The chosen amino acid was cysteine, whose presence have been shown to improve the hole injection. Pentacene, a p-type semiconductor, was used as the active semiconductor layer. Results show that the cysteine layer affects the performance of manufactured devices, although the magnitude of the change requires of a deeper discussion. A 0.93 V shift in threshold voltage has been observed when a 10 nm cysteine layer was evaporated in an BGTC organic transistor. Changes in mobility and intensity have also been observed.

I. INTRODUCTION

A transistor is a three-terminal electronic device in which electric current flows within a channel between two terminals (source and drain) and is regulated by a third terminal (gate). Threshold voltage is defined as the voltage that must be applied on the gate so that the conducting channel is formed. In such a case, current will flow if voltage difference between source and drain is applied.

Thin-film transistors (TFTs) are transistors which have been fabricated by placing thin films of an active semiconductor layer, a dielectric layer and metallic contacts over a suitable conducting substrate. For instance, they are widely used in flat panel displays. In addition, organic thin-film transistors (OTFTs) are TFTs that use organic semiconductors as active layers and have many advantages such as biocompatibility and flexibility, leading to promising applications for bendable displays and chemical and biological sensing.

Each TFT has its own Threshold Voltage, depending on the materials used and fabrication. The Threshold Voltage may be modified by the adding of layers between the dielectric and the semiconductor. It has been achieved through the adding of SAM [1, 2].In this project we have taken a different approach, adding a dipole. There are many different layers that display a dipolar behavior, and we chose to use a layer based on the amino acid cysteine.
The usage of amino acids as layers between the dielectric and the semiconductor can also be used to characterize the dipole moment of the amino acid from the threshold voltage shift from the TFT without that added layer, and the carrier mobility shift.

Cysteine has been considered because it has shown to improve hole injection. Pentacene-based OTFTs have been manufactured and characterized in order to study differences in performance when a cysteine layer is present in the transistor's gate and otherwise. To the best of our knowledge, amino acids have been tested in solar cells but not in OTFTs, so, these results being positive, this first step could lead to a new line of research.

Two sets of devices were manufactured, one device of each pair containing both a cysteine layer with a pentacene one on top, and the other with just the pentacene as the semiconductor. We manufactured the devices following the Bottom Gate - Top Contacts (BGTC) configuration, instead of the Bottom - Gate - Bottom Contacts (BGBC) one. The BGTC configuration was expected to show better results as charge carriers do not have to cross a cysteine layer to go from the contacts to the semiconductor. Thus 2 sets of devices with BGTC configuration were manufactured: one with a cysteine layer of 10 nm thickness and the other without that cysteine layer, and just pentacene as the active semiconductor layer, again with 50 nm thickness. All devices were constructed over a crystal silicon (c-Si) flat substrate, with a thermally-grown silicon dioxide (SiO2) layer at the lab, also using pentacene -an organic p-type semiconductor-, as the active semiconductor layer.

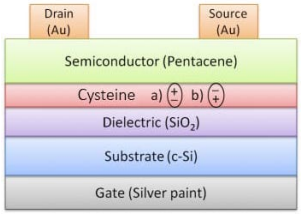

FIG. 1. Diagram of an OTFT with a cysteine layer. BGTC configuration.

II. EXPERIMENTAL PROCEDURE

Organic materials were deposited onto the crystalline silicon substrate by thermal sublimation under high vacuum conditions (10^{-6} mbar). The desired thickness layer was obtained by choosing the right exposition time (de-

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position rate was kept constant by temperature regulation). Metallic contacts were deposited in another vacuum chamber, where gold was also sublimated. This procedure was done to obtain both drain and source electrodes, which were defined by placing a metallic shadow mask over the sample. Resulting sizes of the channel are length (L) and width (W) of 80 μm and 2 mm, respectively. In relation to the gate electrode, it has been added manually afterwards using silver paint. The fabricated

OTFTs were characterized in a cryostat. Characterization was done in the dark and under vacuum conditions (10^{-1} mbar). Electric current was measured by using a Keithley 2636A source meter. The **output** (drain current (I_{D}) versus drain voltage (V_{DS})), **transfer** (drain current (I_{D}) versus gate voltage (V_{GS})) and **saturation** (drain current (I_{D}) versus gate voltage (V_{GS})) were obtained for every transistor. The last one is measured when V_{GS} it is set equal to V_{DS}, which guarantees that the transistor is working in saturation regime.

III. RESULTS AND DISCUSSION

The effects of the cysteine layer in OTFTs are studied by comparing the characteristics of every pair of transistors manufactured. FIG. 2, FIG. 4,5 and FIG. 6 stand for **output**, **transfer** and **saturation** characteristics of the 10 nm cysteine layer in a BGTC configuration, respectively. When comparing the output characteristics

of both transistors (with and without the cysteine layer) in FIG. 2 and FIG. 3, it is clear that the OTFT with the cysteine layer added shows both a similar current and a similar tendency towards saturation as the OTFT without. It may be argued that the current has been lowered by a factor of two, yet as the order or magnitude is of $10^{-7}A$, it is not a relevant result. Both sets of transistors present a clear linear and saturation regime for low and high drain voltages respectively, and cross the x axis at almost $V_{\mathrm{DS}} = 0$ V.

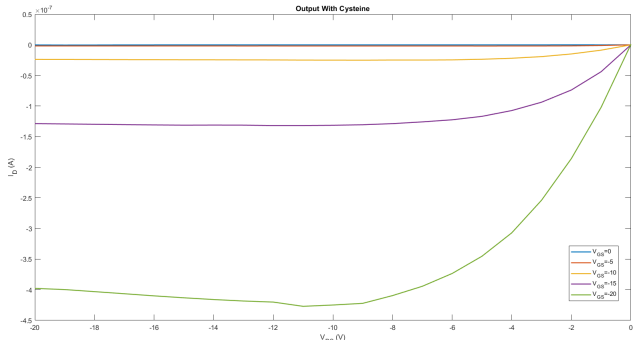

FIG. 2. Output characteristics: OTFT with cysteine layer.

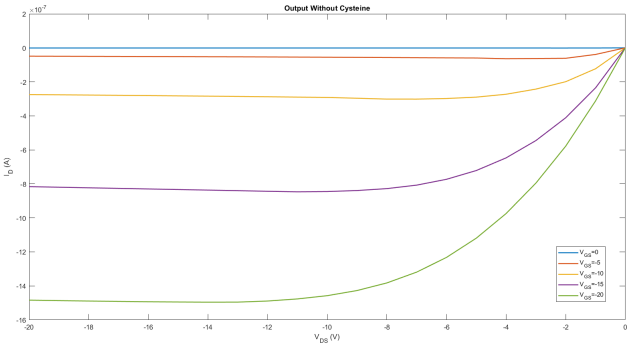

FIG. 3. Output characteristics: OTFT without cysteine layer.

Regarding transfer characteristics presented in FIG. 4 and FIG. 5, it is important to point out that current intensities for the same V_{GS} voltage for the transistor with cysteine do not present a considerable displacement towards more negative gate voltages V_{GS} with respect to the one without the amino acid layer. This indicates that both sets of transistors require a similar voltage between gate and source to form a channel in the OTFT semiconductor layer and, thus, the threshold voltage will be similar for the OTFT with cysteine and that without it. Moreover, both transfer characteristics show clearly an OFF and ON state, with an $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio of around 10^7 in both cases, although for the OTFT with cysteine is a bit higher.
Comparing both graphs (one with V_{DS}=-1V and the other with V_{DS}=-5V) we clearly see a difference in the transistor without cysteine, since it is placed more on the left in the case of V_{DS}=-5V. However, the transistor with cysteine is more robust to changes in voltage V_{DS}.

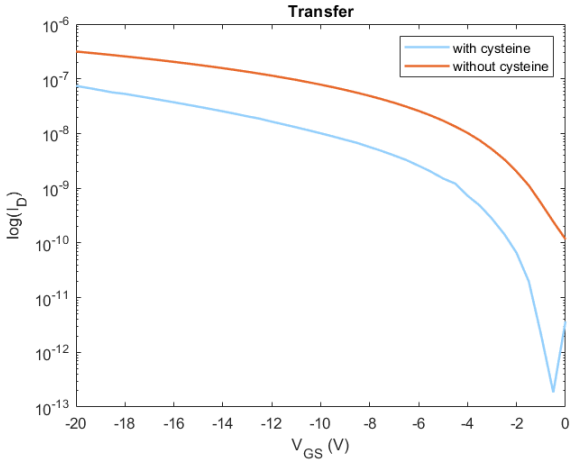

FIG. 4. Transfer characteristics ($V_{\mathrm{DS}} = -1V$) of the OTFTs without and with a 10 nm cysteine layer.

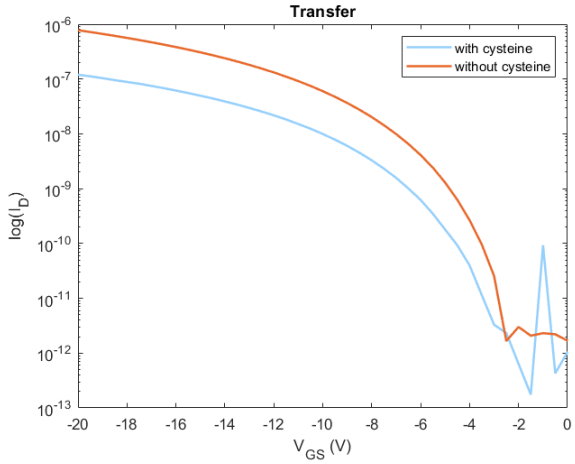

FIG. 5. Transfer characteristics ($V_{\mathrm{DS}} = -5V$) of the OTFTs without and with a 10 nm cysteine layer.

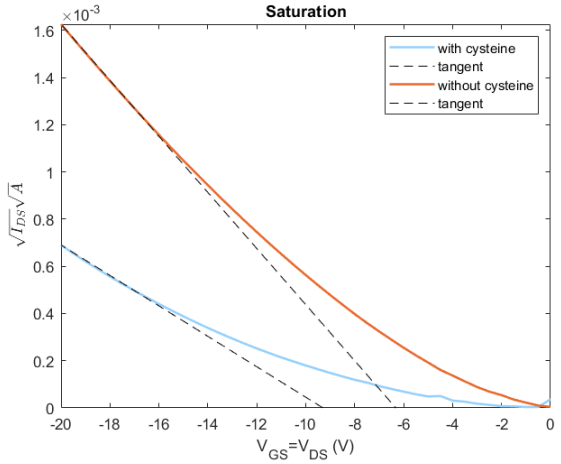

FIG. 6. Saturation characteristics of the OTFTs with and without a 10 nm cysteine layer.

FIG. 6 shows the square root of the absolute value for the drain current as a function of V_{GS}. The drain current (I_{D}) for a TFT (as well as an OTFT), in saturation regime, is analytically modeled as:

$$I_{\mathrm{D}} = \frac{1}{2}\mu C_{\mathrm{ox}}\frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2 \tag{1}$$

Where C_{ox} is the silicon dioxide capacitance and W and L are the width and length of the channel, respectively. Cox can be calculated from $C_{\mathrm{ox}} = \frac{\epsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}}$, where $\epsilon_{\mathrm{ox}} = 3.9\epsilon_0$ and t_{ox} is the thickness of the oxid layer.

Mobility (μ) and threshold voltage (V_{TH}) can be obtained from 1 as follows:

$$\mu = 2\frac{1}{C_{\mathrm{ox}}}\frac{L}{W}\left(\frac{\partial\sqrt{I_{\mathrm{D}}}}{\partial V_{\mathrm{GS}}}\right)^2 \tag{2}$$

$$V_{\mathrm{TH}} = -\left.\sqrt{I_{\mathrm{D}}}\right|_{V_{\mathrm{GS}}=0}\left(\frac{\partial\sqrt{I_{\mathrm{D}}}}{\partial V_{\mathrm{GS}}}\right)^{-1} \tag{3}$$

It is convenient to mention that, taking into account these expressions, one would expect just a single slope in the saturation characteristic. However, devices show a non-ideal behaviour as reflected by the existence of a double slope, one for high values of voltage and other for smaller ones. The existence of a double slope has been reported several times [3, 4]. In order to compute the mobility and the threshold voltage, only the slope for high voltages plotted in FIG. 6 has been considered.

The transistor without cysteine presented a mobility of $\mu = 3.6 \cdot 10^{-2}\frac{cm^2}{Vs}$ and a threshold voltage of V_{TH} = -6.32 V, while the transistor with a 10 nm cysteine layer showed a mobility of $\mu = 1.06 \cdot 10^{-2}\frac{cm^2}{Vs}$ and a threshold voltage of V_{TH} = -9.3 V. It is clear from these results that the addition of the cysteine layer affect the threshold voltage, with a difference of approximately 3 V), but lowers carrier mobility to about a third, that may be caused by the alleged improvement in the hole injection in the channel in the presence of cysteine.

Results for 10 nm of cysteine show a small shift to the left in the threshold voltage of the transistors, about 3V. When a cysteine layer is present, threshold voltage is very similar, so a similar voltage difference must be applied on the gate. A possible explanation for this phenomenon would be that, unlike other amino acids, cysteine does not have a strong dipole moment, whose weak electric field cannot change the band diagram in an appreciable manner, resulting is a similar threshold voltage to that of transistors made with nonpolar molecules, such as pentacene.

The effect of this dipole layer can also be studied from an alternative point of view, proposed by professor Supriyo Datta [5]. According to his model, current flows due to an electrochemical potential difference between drain and source electrodes and due to available electronic states in the semiconductor. The electrochemical potential might also be referred as to the Fermi level or the work function, and it is defined as the minimum energy to extract an electron at zero Kelvin.

Drain and source contacts are made of the same material (gold) so in absence of an externally applied voltage, their electrochemical potential will remain the same and no current will flow. If a voltage difference V_{DS} between drain and source is applied, the energy of the positive terminal is lowered by V_{DS} with respect to the other one and a current does appear. It should be noted that holes flow from a lower potential to a higher potential. If $V_{\mathrm{DS}} < 0$ then $I_{\mathrm{D}} < 0$, which fits with experimental results.

Nevertheless, current can only occur if there are available states in the semiconductor, so that density of states and Fermi distribution must be taken into account. In order to make easier the comprehension of how V_{GS} affects the channel and of the physical meaning of the threshold voltage, the following figure is shown:

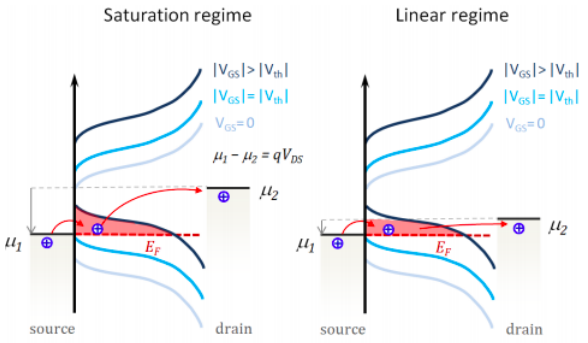

FIG. 7. Schematic diagram of the model proposed by Supriyo Datta. Horizontal axis: number of electronic states available. Vertical axis: energy. (Right: Linear regime model. Left: Saturation regime model.)

In FIG. 7 the vertical axis represents the energy and the horizontal axis is the number of states, which is the product between the Fermi distribution and the density of states. Notice that available states are those which reside between the drain energy ($\mu 2$) and the source energy ($\mu 1$), painted in red in the figure. As V_{DS} and V_{GS} are measured with respect to the source, $\mu 1$ is taken as the reference level.

The function of V_{GS} is to shift the curves of the available states up and down. Firstly, consider that V_{GS} is zero, in this case, as shown in the figure, there are no available states, as the source and drain energy interval falls in the energy gap of the semiconductor. If a negative V_{GS} is applied, the curve is shifted upwards. While making V_{GS} more negative, there is a point at which the higher point of the curve of the valence band coincides with $\mu 1$; that is, at this point available states start to appear. The V_{GS} needed to get to this point is the threshold voltage, V_{TH}: as there are available states in the semiconductor, the channel is formed and holes can flow through it. If V_{DS} remains fixed and V_{GS} continues being more negative, more states are available and the current becomes higher.

Given a V_{GS} more negative than V_{TH}, if V_{DS} is varied $\mu 2$ changes and, consequently, the number of states also changes. It is interesting to point out that two different cases can be considered: linear and saturation regime. In linear regime, if V_{DS} is more negative, $\mu 2$ is higher and more states are available in the channel, increasing the current that flows through it. This does not happen in saturation regime. In saturation regime a V_{DS} is applied such that $\mu 2$ surpasses the maximum of the valence band curve. Even though $\mu 2$ continues to increase, the number of states remains equal, as now $\mu 2$ is on the gap energy region and no more states are added.

Taking into account the results obtained, the effect produced by the adding of a cysteine layer do not shift the threshold voltage in a remarkable way, which has already been argued to be due to it's low dipole moment. The decrease in carrier mobility can be justified by the higher injection of holes in the channel, compared to the OTFT's that do not have a cysteine layer below the active semiconductor one. That higher injection makes for a higher carrier density, which is known to be inversely proportional to the carrier mobility of such a device.

IV. CONCLUSIONS

The aim of this project was to study the effect of a cysteine layer on OTFTs. OTFTs with a cysteine layer have been successfully manufactured and characterized. Moreover, several effects due to the cysteine layer have been observed: The addition of a dipole layer results in a small but undirectional change in our threshold voltage, due to its low dipole moment. An even smaller difference has been noted in current, but a satisfactory explanation has not been found yet. The cysteine layer has been shown to lower the carrier mobility in the channel as it increased the carrier density of the device. These phenomenon are already being studied in the case of self-assembled monolayers (SAMs).

More measures should be done in order to confirm the apparent relation between the dipole layer thickness and the shift experienced in the electrons mobility. Also how cysteine bonds to pentacene and SiO_2 should be studied in detail. Knowing the nature of the bonding would give valuable information to complete the understanding of the observed phenomena.

Furthermore, other amino acids with different dipole moment could be implemented. It is expected that the higher the dipole moment, the larger the shift in the threshold voltage. If this correlation was to be true, it might be possible to determine which amino acid forms the dipole layer, thus allowing for a new characterization technique to be developed. A seamless explanation on the correlation between the cysteine molecule and the carrier mobility has not been found yet, although it could lead to a deeper understanding of both the OTFT inner workings and of the molecule's own characteristics.

In conclusion, the trend is that the incorporation of a 10nm layer of cysteine displaces the curve to the left,but because the dispersion of the data it paves the way for future research to be done on the topic, which might eventually lead towards future applications.

V. ACKNOWLEDGEMENTS

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