Modeling the Impact of Process Variations in Worst-Case Energy Consumption Estimation

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***Abstract*—The advent of autonomous power-limited systems poses a new challenge for system verification. Powerful processors needed to enable autonomous operation, are typically power-hungry, jeopardizing battery duration. Therefore, guaranteeing a given battery duration requires worst-case energy consumption (WCEC) estimation for tasks running on those systems. Unfortunately, processor energy and power can suffer significant variation across different units due to process variation (PV), i.e. variability in the electrical properties of transistors and wires due to imperfect manufacturing, which challenges existing WCEC estimation methods for applications. In this paper, we propose a statistical modeling approach to capture PV impact on applications energy and a methodology to compute their WCEC capturing PV, as required to deploy portable critical devices.**

I. Introduction

Autonomous systems, including drones and electric cars, become ubiquitous nowadays. These battery-powered systems perform critical real-time tasks, and hence, must undergo a rigorous Validation & Verification (V&V) process ensuring that their functional and non-functional requirements are met. In particular, energy consumption must be proven to be within specific bounds to guarantee safe operation and specific battery duration thresholds. Hence, the V&V process of autonomous systems needs solutions for reliable and tight worst-case energy consumption (WCEC) estimation.

Autonomous systems build upon complex software demanding high computing performance to execute timely. This is achieved by deploying complex hardware, e.g. based on multicores and accelerators, implemented with high integration level. Therefore, WCEC estimation must (1) scale to arbitrarily complex software-hardware systems and (2) account for the impact of process variation (PV) intrinsic to highly-integrated process technologies. PV is an inherent consequence of the processor's manufacturing process and makes transistors and wires that were initially designed to be identical, end up having significantly different electrical properties. As a result, energy consumption varies significantly across different instances of the same processor. This challenges WCEC estimation since the WCEC estimates obtained for a given chip unit are not valid for other chip units. Performing V&V activities on every deployed chip poses a serious issue for autonomous systems industry, because the number of units can be in the range of millions and the costs are simply unaffordable (e.g. due to the low cost of drones and high chip count in cars). Although industry carries out several tests to all deployed units, the full V&V process followed for certification is not repeated for each system unit. In this context, our contributions are:

① We analyze the difficulties in deriving tight WCEC estimates in the presence of PV, which emanate from the fact that PV causes energy consumption variations and, therefore, different WCEC across different nominally-identical processor units.
② From the previous analysis, we capture the impact of PV on energy and power with a statistical-based modeling approach. We show how the input parameters of the model can be directly provided by processor manufacturers and by using current processors' performance monitoring counters (PMCs).
③ Building on the previous model, we provide a well-defined methodology for WCEC estimation. Our methodology, performs the entire estimation on a single processor unit, while delivering WCEC estimates that hold for all processor units and simplify the V&V process of autonomous systems.

We evaluate our proposed model and methodology with a variety of experiments with state-of-the-art power and PV simulators. We apply our methodology to an embedded processor design resembling the LEON4 processor for autonomous space systems. Results collected on representative benchmarks and two space case studies show that the proposed statistical approaches are a natural fit for WCEC estimation.

II. Background on power estimation

Power consumption has two main contributors: static and dynamic power. Static power (P_{sta}) corresponds to transistor leakage currents and depends on the exact physical properties of the manufactured circuits and thus, is affected by process variations. Dynamic power (P_{dyn}) is a consequence of the charging and discharging process of transistor's gate capacitance, which depends on the exact electrical features of the processor unit that, in the presence of PV, can only be known once the device is manufactured.

Model-based power estimation. The confidence on the energy estimates derived with static (analytical) models lies on the ability of deriving accurate power models, which in turn, builds on a combination of the information in technology libraries, usually simulated using standard electronic simulation tools. Model-based techniques are slow in general, limiting the window of analysis to a few thousands of cycles at most. For instance, SPICE models to characterize a memory macrocell with synthetic stimuli last several days of simulation since a single CMOS transistor model may account for more than 40 parameters [25]. Even with highly detailed models of the hardware components, the fact that in reality these components suffer from manufacturing deviations (PV) makes it infeasible to estimate power at the desired accuracy if PV is not conveniently accounted for.

 DOI 10.1109/DSD.2019.00092

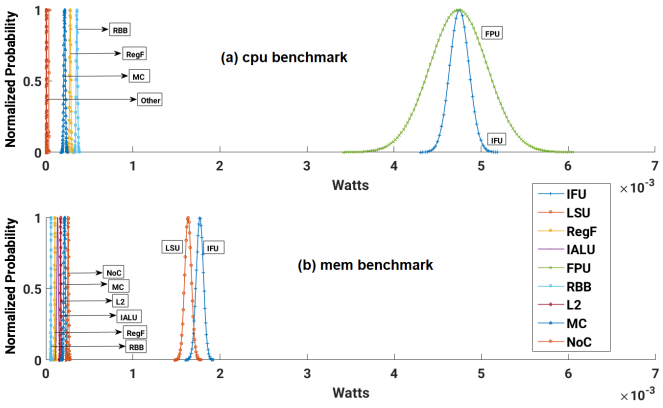

Fig. 1. Per-FUB power-variability for the CPU- and mem-intensive benchmarks

Measurement-based power estimation builds on the availability of power monitoring units. Several studies show how to achieve fine-grain power measurement of processors using existing activity power monitors [3]. Measurements are very useful for power verification since they provide real power consumption numbers of the processor. However, power measurements are only possible once the processor (or a test-chip) is manufactured, and hence they are used in the post-silicon validation step.

Deriving tight WCEC estimates builds on the ability to define representative scenarios. In general, maximum peak power numbers can be obtained empirically using kernels that generate the a-priori most stressing situations (power viruses [8]). However, this process does not allow estimating tightly the maximum energy a specific task can consume.

III. PV-related power variability

PV makes power consumption vary across different processor units (instances) and Functional Unit Blocks (FUBs), i.e. instances of functional units, on the same processor unit.

Within-chip PV, while less severe than chip-to-chip PV, makes the effects of manufacturing deviations be different across FUBs. Specific per-FUB PV creates an indirect dependence between the specific software executed and the observed PV related power variability. This dependence poses new difficulties in the WCEC estimation process since accounting for the impact of PV requires knowing the exact contribution to the power variability of each FUB. To illustrate this, we have performed an experiment using 2 synthetic software applications: a memory-intensive application and a compute-intensive one. The main features and FUBs of our reference processor include: instruction fetch unit (IFU), load-store Unit (LSU), register file (RegF), integer ALU (IALU), floating-point unit (FPU), result broadcast bus (RBB), L2, NoC, and memory controller (MC).

Intuitively, power variability caused by PV is not the same for all programs. For instance, the PV power variability in the FPU has no impact on the memory-intensive benchmark: Figure 1 shows the PV-related power consumption variability for each FUB obtained with McPAT-PVT [22]. Probability distribution functions are normalized to make their ***y-axis*** values match the same range for visualization reasons. We observe that

TABLE I
Summary of modeling distributions for PV features

Processor feature	Distribution
PV-induced power variability	Gaussian [23]
Manufacturing deviations	Gaussian fields [21]
Power and Delay due to Gate Length PV	Non-Gaussian [26]
Dynamic power per FUB	Multi-modal [9]

for the compute-intensive benchmark the FUBs with greater contribution to the power variability are the IFU and the FPU, whereas for the memory benchmark the FUBs with higher power variation are the IFU and LSU.

PV causes different impact on different FUBs, which makes the power probability distribution function vary across FUBs. For instance, some FUBs can follow a Gaussian distribution while others chi-square, log-logistic, or Weibull distributions [23][21][9][26]. The combination of these distributions can result in an arbitrary statistical distribution for the overall processor.

IV. PV-aware Energy Modeling

Next we propose a methodology for capturing the impact of PV through measurements. We describe our methodology, its parameters, and its fitness for certification. The proposed methodology builds on current industrial practice in CPU power modeling [10], which facilitates its potential adoption.

A. Random Nature of PV

PV impacts the physical characteristics of devices (transistors and wires), altering their nominal operation characteristics, including power and delay. PV is usually decomposed into systematic PV and random PV. The **systematic** component of PV is usually subject to strong spatial correlation across neighbor devices (transistors and wires). However, it has been shown that systematic PV impact on the different physical parameters can be accounted as an additive factor together with random PV, thus simplifying model complexity [21]. The **random** part of PV is a consequence of different uncontrolled phenomena like random dopant fluctuations. Random PV is modeled with probabilistic methods [11] that are applied either across processor units or across devices (transistors and wires). The particular implementation details of the circuits cause the impact of PV in energy distribution to vary across FUBs.

Due to the diverse nature of PV, the treatment of PV requires developing specific models to accurately capture its random impact. We list some specific methods to capture the PV impact of different parameters in Table I. It follows that the actual random distribution of PV may have any shape. Hence, our proposal needs to build on a non-parametric statistical method. Extreme value theory (EVT) [12] is such a method, since it is agnostic to the particular distribution of the phenomena whose extreme behavior is to be predicted. EVT may incur some pessimism due to the fact that it fits a tail model to the maxima, as if all the population behaves as the maxima. EVT *inflates* the expected probability of maxima in its application process, thus bringing some limited, but not null, pessimism as shown in Section VI. Yet, EVT ends up being a reliable and tight choice as we show in this paper.

B. The Model

Let E_{sta} and E_{dyn} be the static and dynamic energy consumption of a given task, respectively. Both can be further broken down into the individual contributions across FUBs (i.e. fetch unit, L2 cache, etc). Then, the static energy per FUB is roughly proportional to execution time and depends on the specific activity generated by each task in the case of dynamic energy. Commonly, models describe dynamic energy consumption per access type (e.g. read, write) per FUB and static energy consumption per time unit (static power) and FUB. Hence, energy consumption of a task can be described as shown in Equation 1, where τ_a is the task under analysis and t_a its execution time. Our processor has $\mathcal{F}$ FUBs, and each individual FUB, f, has f_y access types. Hence, P_f^{sta} stands for the static power of the FUB f and $E_{f,y}^{dyn}$ for the dynamic energy per access type y of FUB f. Finally, $Acc_a^{f,y}$ stands for the number of accesses of type y on FUB f performed by τ_a.

$$E_a = E_a^{sta} + E_a^{dyn} = \sum_{f\in\mathcal{F}} \left(P_f^{sta}\cdot t_a\right) + \sum_{f\in\mathcal{F}}\sum_{y\in f_y}\left(E_{f,y}^{dyn}\cdot Acc_a^{f,y}\right) \quad (1)$$

PV alters energy consumption, introducing random variations into P_f^{sta} and $E_{f,y}^{dyn}$. In particular, and based on the fact that dynamic and static energy consumption have a different nature, each component suffers a different relative dynamic and static energy variation. Still, all access types to a given component are subject to the same relative amount of variation.

Task energy accounting for PV can be derived as shown in Equation 2, where pv_f^{sta} and pv_f^{dyn} stand for the correction factors to account for the specific PV affecting static and dynamic energy of each FUB respectively.

$$Epv_a = \sum_{f\in\mathcal{F}} \left(P_f^{sta}\cdot pv_f^{sta}\cdot t_a\right) + \sum_{f\in\mathcal{F}}\sum_{y\in f_y}\left(E_{f,y}^{dyn}\cdot pv_f^{dyn}\cdot Acc_a^{f,y}\right) \quad (2)$$

The impact of PV on energy for each FUB depends on the different devices used for their implementation. Therefore, the impact of PV on energy can be modeled by means of specific probabilistic distributions across FUBs, where each FUB is subject to a relative power variation. This variation, though different across FUBs, is regarded as homogeneous for any given FUB, so it impacts all accesses to the FUB homogeneously and does not change over time since it relates to the particular effects of PV on the chip manufactured.

Hence, pv_f^{sta} and pv_f^{dyn} can be modeled according to the underlying distribution. For instance, if such distribution is Gaussian, they would be modeled as follows:

$$pv_f^{sta} \sim \mathcal{N}\left(1, \left(\sigma_f^{sta}\right)^2\right) \quad (3) \qquad pv_f^{dyn} \sim \mathcal{N}\left(1, \left(\sigma_f^{dyn}\right)^2\right) \quad (4)$$

where σ_f^{sta} and σ_f^{dyn} are the relative standard deviation for static and dynamic power (and energy) consumption of FUB f (e.g. 0.03 if the standard deviation for power variation is 3%).

Table II summarizes the inputs needed in our model and how they can be derived. **Processor related** parameters estimates are needed during the design and fabrication process to verify that power dissipation will not exceed the Thermal Design Point (TDP) before manufacturing the chip. Hence, chip vendors model those parameters from information obtained in process technology tests. Once power is verified to stay below affordable levels with the electrical power model, chips are fabricated and tested. Typically, chip manufacturers use in-field data to feed models back and correct discrepancies. Hence, chip vendors can estimate with high precision the power parameters needed in Equations 2, 3, and 4. **Software related** parameters can be measured during software tests by means of the performance monitoring unit (PMU).

TABLE II
PARAMETERS NEEDED FOR APPLYING THE METHODOLOGY

Processor related	P_f^{sta}	Static power per FUB
	$E_{f,y}^{dyn}$	Dynamic energy per FUB per access type
	σ_f^{sta}	Std deviat. for static energy per FUB
	σ_f^{dyn}	Std deviat. for dynamic energy per FUB
Software related	t_a	Task's execution time
	$Acc_a^{f,y}$	Per-type access count per component

V. WCEC ESTIMATION METHODOLOGY

WCEC estimation is useful to provide guarantees about software being compliant with strict energy consumption constraints for autonomous systems. Our WCEC estimation approach consists of two main steps: (1) collecting representative energy measurements of the task and (2) estimating the energy budget needed so that it cannot be exceeded with a relevant probability.

Measurement collection (sampling). Once the task has been executed and software-related parameters obtained through the PMU, our method produces energy measurements accounting for the impact of PV. To that end, we perform a Monte-Carlo experiment where pv_f^{sta} and pv_f^{dyn} in Equation 2 are sampled from their reference distributions. Each observation of the Monte-Carlo experiment, i.e., $o \in \mathcal{O}$, delivers specific $pv_{f,o}^{sta}$ and $pv_{f,o}^{dyn}$ values for each FUB $f \in \mathcal{F}$. These are used to produce a specific PV corrected energy sample (Epv_a^o) from the energy sample (E_a) of the task under analysis τ_a.

WCEC distribution. We regard EVT [12] as a convenient method for WCEC estimation as it is used to predict extreme (rare) events. EVT models the largest (tail) values measured from the phenomenon under analysis. EVT has already been used successfully in the context of WCET estimation, resulting in probabilistic WCET estimates [2][14][19].

In applying EVT to WCEC estimation we resort to the EVT application process in [2], which carries the following application requirements: it applies to independent data and processes and when an exponential tail is guaranteed to be a reliable upper-bound. Energy measurements in the sample correspond to independent and identically distributed observations of the same phenomenon (random variable) by construction of the process studied (energy consumption variation due to PV) and measurement protocol used (not carrying any state across measurements). From this observation, it follows that no dependence exists across input measurements, which we empirically assess with proper independence and identical distribution (i.i.d.) tests [4], which are a prerequisite for the reliable application of EVT.

The minimum sample size for a reliable application of EVT is only dictated by EVT itself. We start generating 1,000 energy measurements as initial sample size and increase the sample size whenever the method requests it. In this work in particular some of the experiments required 2,000 measurements, hence we used 2,000 measurements for the sake of homogeneity.

Accounting for multiple program inputs. Our methodology covers a specific set of input values for the program. However, test campaigns need to account for different operation conditions, which are modelled using multiple input sets for the program under analysis. The way to proceed resembles the approach followed for WCET (timing) estimation [16]. Hence, the methodology above needs to be applied independently for each set of input values, and EVT used in each individual set of measurements for a given input set. Then, the different WCEC distributions obtained need to be combined using the *max envelope* operator which, for each exceedance probability selects the highest energy value across all WCEC distributions, thus delivering the tightest WCEC distribution that upperbounds all those for each individual input set.

A. WCEC Interpretation and Safety Standards

Once we obtain the WCEC distribution, we can select as WCEC estimate the value whose exceedance probability is sufficiently low. Since the only source of variation is PV and it changes across chip units, a given exceedance probability relates to the probability of having a processor unit that may exceed such energy value systematically due to its specific PV.

In general, safety goals and safety requirements are defined with the aim of mitigating – rather than eliminating – the risk that hardware or software misbehavior causes a system failure. For instance in automotive, ISO-26262 stipulates the maximum allowable likelihood of occurrence of random hardware faults. In doing so, ISO-26262 acknowledges that safety techniques cannot achieve full coverage, allowing different diagnostic coverage. Overall, the interpretation of the energy exceedance probability matches that of defective hardware components (e.g. the probability of having a defective processor or a defective wheel). For instance, we can set the exceedance probability down to 10^{-9}, thus meaning that at most 1 every 10^9 processors may lead to exceeding the WCEC estimate for this task.

VI. Experimental Results

Architectural, power, and PV models. While processor vendors have the data needed by our model, this information is usually not released for commercial processors for autonomous systems. Hence, we build on SoCLib [15], a cycle accurate simulator, to model the timing behavior of a LEON4 processor We integrated McPAT-PVT [22] power estimation methodology into SoCLib to collect energy and power measurements. McPAT-PVT is an extended version of the McPAT tool [13] that allows accounting for the impact of PV in power measurements. For our experiments, we model a process technology of 22 nm, an operating voltage of 0.9 V, and an operating frequency of 700 MHz. Note that, the methodology is architecture and benchmark agnostic and our set-up just a representative example of the real-time domain.

Benchmarks and case studies. We evaluate two space case studies: DEBIE and OBDP. The former, manages an instrument for small space debris and micrometeoroids observation, that is part of the PROBA-1 satellite. The latter is part of the near infrared (NIR) HAWAII-2RG [1] detector, used in some real missions to process raw frames provided by the detector. We also use EEMBC automotive benchmarks [20] as reference benchmark suite, since they represent a number of critical real-time functions of some automotive systems. In particular we use cacheb, a2time, aifftr, aifirf, aiifft, basefp, bitmnp, canrdr, idctrn, iirflt, matrix, pntrch, puwmod, rspeed, tblook, ttsprk.

TABLE III
MAX OBSERVED ENERGY, AND PWCEC (IN μJ) WITH PV

bench	MAX	ΔE_{PV}	pWCEC EVT(10^{-7})	Δ^{EVT}_{pWCEC}	pWCEC Gauss	Δ^{Gauss}_{pWCEC}
cac	202.7	92.9 %	239.4	18.1 %	249.2	23.0 %
ma	8259.2	92.7 %	9716.5	17.6 %	10031.2	21.5 %
ai	2070.1	95.0 %	2520.3	21.7 %	2486.2	20.1 %
pn	51.4	98.2 %	58.2	13.2 %	62.2	21.1 %
rs	15.0	104.7 %	18.4	22.8 %	17.9	19.8 %
pu	54.4	101.2 %	67.0	23.1 %	65.4	20.2 %
aif	39.4	94.3 %	53.3	35.4 %	48.7	23.8 %
aii	1914.5	94.7 %	2051.9	7.2 %	2301.6	20.2 %
a2	25.6	98.8 %	33.1	29.3 %	31.5	23.1 %
id	348.2	92.2 %	437.9	25.7 %	429.0	23.2 %
ii	38.3	103.5 %	49.5	29.2 %	46.5	21.5 %
ba	59.7	106.5 %	64.5	8.0 %	70.7	18.4 %
bi	196.8	98.2 %	231.1	17.4 %	236.1	20.0 %
tb	17.1	100.9 %	21.6	26.3 %	20.8	21.5 %
can	36.6	99.8 %	46.8	27.8 %	44.3	21.1 %
tt	37.6	103.7 %	46.2	22.9 %	44.4	18.4 %
obd	143817.0	94.6 %	205486.1	42.9 %	176506.2	22.7 %
deb	228420.7	100.2 %	263980.0	15.6 %	269121.3	17.8 %

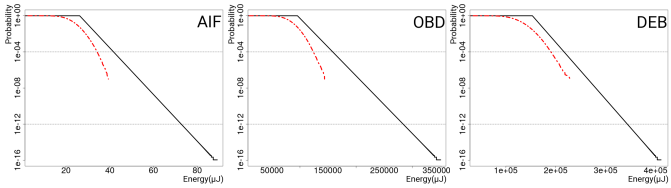

Fig. 2. pWCEC distribution in μJoules and empirical CCDF of the PV-adjusted energy measurement

Statistical Characterization of PV. We randomly generate a population of processor instances, N_p, whose FUB's PV behaves according to the specific distributions that would be provided by the processor manufacturer for real processors. In our setup used for illustration and evaluation purposes, we obtained those values from the McPAT-PVT power estimation tool due to the lack of this information from a real processor. However, in a practical case, such information would be provided by the chip vendor. Note, however, that our methodology holds regardless of the actual values used and hence, the representativeness of McPAT-PVT values, although it has already been discussed in [22], has no impact on the method proposed in this paper. This approach delivers N_p independent energy measurements per benchmark that resemble the chip-to-chip energy variations. Unless stated otherwise, we focus on Gaussian distributions in the remaining of the paper.

PV-generated power variability. In our setup, from the execution of each benchmark in the simulator we obtain the number of accesses to each FUB ($Acc_a^{f,u}$) and the task's execution time (t_a), which we fed into the power model of McPAT-PVT. McPAT-PVT provides static power per FUB

and cycle (P_f^{sta}) and dynamic energy per access type per component ($E_{f,y}^{dyn}$). Building on these parameters, we obtain the power dissipation per component as well as a power variation σ per component due to PV, as presented in Section IV.

The first two columns (after the benchmark names) in Table III show the absolute maximum energy consumption per benchmark, and the magnitude of the impact of variations, labelled as ΔE_{PV}. The latter is computed as $\frac{max-avg}{avg}$. We observe increments as high as 117% (the maximum is ≈2.2x the average), while average variations are of 100% (≈2x). This means that the maximum value observed is, on average, 2x times the average, thus further emphasizing the importance of accounting for PV in WCEC estimation.

Probabilistic WCEC Estimates. Starting from a set of measurements $o \in O$ of the energy for the modelled processor unit under analysis , E_a^o, we use specific statistical correction factors $pv_{f,o}^{sta}$ and $pv_{f,o}^{dyn}$ values for each FUB f to produce a PV corrected energy sample (Epv_a^o). This sample is passed as an input to EVT to generate a probabilistic WCEC (pWCEC) estimation that describes the probability of an arbitrary processor unit to exceed an energy consumption value.

Figure 2 shows 3 plots – 2 ESA applications, and the EEMBC with the highest pWCEC over-estimation (aif) – with their corresponding pWCEC distributions. Red dashed lines correspond to the empirical complementary cumulative distribution functions (empirical CCDF) of the measurements, whereas straight black lines stand for the pWCEC distributions.

To provide evidence on the confidence in deriving WCEC estimates, we collected 10^7 measurements for each benchmark. Note that performing such an experiment is not needed (and it is infeasible in the general case). We use it for comparison purposes and hence, pWCEC is estimated with 2,000 measurements. For the lowest probability for which we measured the actual distribution, 10^{-7}, pWCEC curves are 22.6% higher than observations on average.

We observe that pWCEC distributions upper-bound observed energy consumption for all benchmarks, and gently follow the observed distributions. We also observe that the slope (the vertical variation) of the observed distribution is also gentle. This shows that the impact of PV is high and emphasizes the importance of properly accounting for PV in the process of WCEC estimation, as PV can produce large energy variations.

VII. Related Work

Powerful tools exist to measure power at electrical level (e.g. SPICE [6]). Other tools estimate power at higher abstraction levels by modeling resistances and capacitances of memory structures (e.g. CACTI [24]). McPAT [13] and WATTCH [5], among other tools, estimate the power of full processors at system level building upon CACTI. Some authors analyze the dependence between WCEC and input values of different components [18]. Others [17] assess the validity of current WCEC methods, showing that WCEC cannot be estimated with models that work at an instruction level. The use of EVT has also been proposed to estimate circuits peak power [7]. However, unlike our approach where the exercised workload is known, this approach relies on the ability of the user to define representative testing scenarios and thus, faces the same problems of state-of-the-art power verification approaches.

VIII. Conclusions

We analyzed PV impact on the processor energy consumption, and presented a methodology based on statistical-modeling that deals with PV during the WCEC estimation process of autonomous systems. This enables the estimation of WCEC by accounting for the probabilistic nature of PV and using probabilistic approaches for WCEC estimation, such as EVT. Our results show that the impact on energy of PV is large, and can be appropriately bounded with probabilistic means.

Acknowledgments

This work has been partially supported by the Spanish Ministry of Economy and Competitiveness (MINECO) under grant TIN2015-65316-P and the European Research Council (ERC) under the European Union's Horizon 2020 research and innovation programme (grant agreement No. 772773). MINECO partially supported Jaume Abella under Ramon y Cajal fellowship RYC-2013-14717.

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