Electronic Systems
Notebook of Lab Activities

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Contents:

Lab Activity nº 1: Lab Instrumentation

Main Goal: To learn how to use the different instruments of the lab for measuring electrical signal parameters, both in continuous (DC) and alternate current (AC), and to get used to the basics of bread-board prototyping. These skills are considered CRUCIAL for the forthcoming lab activities of this course and development of technical skills during your current degree program.

As such, students are encouraged to observe and experiment with the different buttons and controls that instruments have, and to follow mounting instructions carefully. The machines of the lab can be grouped in the following two main groups:

- **Stimulus** (or Signal) **generation**: The *Power supply* for generating continuous (or DC) current and *Waveform Function Generators* for generating time-varying signals.
- **Measurement Instrumentation**: The *Multi-meter*, which contains an ohmmeter, a voltmeter and an ammeter, all of which are aimed for measuring steady-state electrical variables; and the *Oscilloscope* for visualizing and measuring parameters in time-varying signals.

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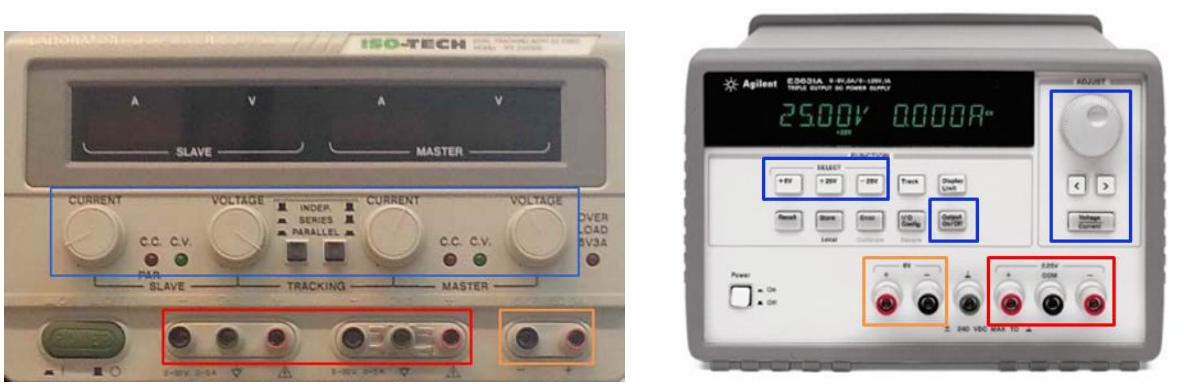
1 DC Power Supply

This device fixes its output to a constant voltage and delivers energy to the circuit in the form of DC current. Two models are available in the labs: 1) The **IPS2303DD** from ISO-TECH (Fig. 1a) at L-104; and 2) The **E3631A** from Agilent (Fig.1b) at L-106. Both consist of two identical outputs (red boxes) with adjustable voltage from 0 to 30V/3A and from 0 to 25V/2A, respectively. Another auxiliary high-power output (orange boxes) provides a fixed voltage of 5V for a maximum 5A DC current (The auxiliary output of the E3631A is variable and of 6V/5A).

When the outputs are connected, the display shows both fixed voltage and injected current to the user's circuit. The maximum voltage and current admitted to the circuit is programmed through the control functions in the front panel (rollers and buttons inside the blue boxes). However, the procedure varies depending on the machine model.



(a) (b)

***Figure* 1.** Power supplies at the labs: **a)** IPS 2303DD from ISOTECH (L-104); b) E3631from Agilent (L-106).

Task LAB1: Configure one of the outputs from the DC power supply to operate at **5V** with a maximum current of **0.25A**. Proceed as indicated depending on the machine model available at your workstation (see below).

DC current limiter:

- **IPS2303DD:** With the device turned OFF, **1)** Connect a cord between the positive and negative terminal at the output you're going to use; **2)** Turn the power ON and observe the current value in the display; **3)** Use the roller labelled as CURRENT to set the limit to 0.25A; **4)** Disconnect the output cord.
- **E3631A:** In this model you can configure the current limiter without connecting a cord at the output terminals. **1)** Turn the power ON; **2)** Select the CURRENT option from the ADJUST menu in the front panel on the right (a digit from the display blinks); **3)** Use the '<' and' >' buttons to move along the digits and set the value with the roller until the value 0.25A is shown on the display.

DC Voltage configuration:

- **IPS2303DD: 1)** Turn the instrument ON leaving output terminals unconnected; **2)** Use the VOLTAGE roller to set the output to 5V.
- **E3631A: 1)** Select VOLTAGE from the ADJUST button (the display shows the current voltage and one digit blinks); **3)** Use the buttons to move along the digits and set 10V.

At this point, the machine is ready to operate with the configured options. However, for safety reasons, it is preferable to develop connections with unpowered outputs. In the **E3631A** model, an OUTPUT ON/OFF button allows these operations to be made while the machine is turned ON. In this case, a message appears indicating whether the output is deactivated; then, the user can connect the cords safety and push the button again to reactivate the output. In the **IPS2303DD** model, however, these operations may be made with the machine turned OFF.

> **REMARK:** You must **WRITE DOWN** your answers in the form provided at the end of this document (See Annex 1) and deliver it to the lab teacher at the end of the session.

2 The Digital Multi-meter

A *digital multi-meter* (Fig. 2) integrates an ohmmeter, a voltmeter and an ammeter in one device and, as such, it can measure electric resistance, voltage and electric current; as well as other auxiliary parameters of stationary behavior.

From the different terminals on the right of the front panel (red box), the ***VΩ*** terminal is intended for measuring electric voltage and resistance, whereas the terminal labelled as '***Fuse on Rear Pannel***' is the point of electric current measurement. The red color (as well as the 'HI' label) indicates the POSITIVE connection (+), and the black terminal in the middle (also labelled as LO) is the NEGATIVE (-) one, which is "common" to all three measure variables.

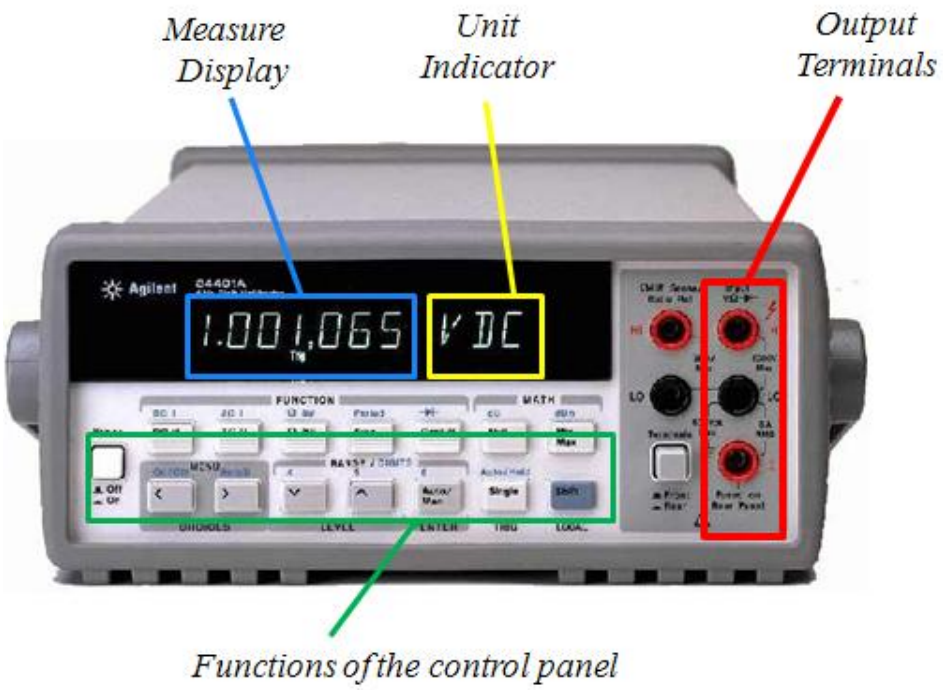


***Figure* 2.** Digital multi-meter 34401A at the L-104 and L-106, courtesy from Agilent Technologies

The device function is configured through the keypad in the front panel (green box). The blue function above is selected by means of the SHIFT button. As such, for measuring resistance, DC voltage and electric current; the options are **Ω**, **DC V** or **DC I** (SHIFT > DC V) respectively.

Generally, the multi-meter is intended for viewing stationary parameters, which are refreshed over the time, as information can only be provided through the display. Nevertheless when time-varying signals are sensed through the output terminals, in DC mode (DC V as well as DC I) the display shows the **average value**, whereas in AC mode (**AC V** and **AC I**) it shows the true[1] **root-mean-square value** (or *rms*). Strictly speaking, the average value of any signal $x(t)$ is obtained as

$$\langle x \rangle = \frac{1}{T}\int_T x(t)dt, \tag{1}$$

where T corresponds to the measuring interval[2] used by the device, and the true *rms* value is obtained as

$$x_{rms} = \sqrt{\frac{1}{T}\int_T x^2(t)dt}. \tag{2}$$

[1] Some multi-meters only provide the 'rms' value of sinusoids, since this value is easily obtained correcting the output peak by a factor of 0.707, which requires less resources. Hence, manufactures refer to the "true rms" implementation when their instrument contains the required circuitry to develop (2). It has to be mentioned, however, that the usefulness of this value relies on the basis of repetitive signals, which is a necessary condition in order to give a steady value of this measure through the display.

[2] T is automatically fixed by the device. In DC mode, this value corresponds to a time interval of fixed width along which the average value is estimated. As such, it can be seen as the refreshment time of the display. In AC mode, the multi-meter uses a sophisticated system to detect the periodicity of signals and, then, it configures T accordingly. See the manufacturer user's guide for more information on this topic.

Task LAB2: Get acquainted with the multi-meter functions by carrying out the following measurements:

Electric resistance:

- **1)** Identify each one of the five different resistors included in the kit. **2)** Use the ohmmeter to measure the resistors. **3)** Turn the multi-meter ON and select **Ω** in the control panel button (the digital display shows the message MOHM). **4)** Finally connect the cords and the resistor as shown in Fig. 3.
- Determine the deviation of each resistor from its nominal value according to the following equation. Check whether the values are within tolerances.

$$ERROR(\%) = \frac{\left| R_{Óhmetre} - R_{No\,min\,al} \right|}{R_{No\,min\,al}} \times 100 \qquad (3)$$

REMARK: The TERMINALS button must be turned OFF in order to activate the front panel.

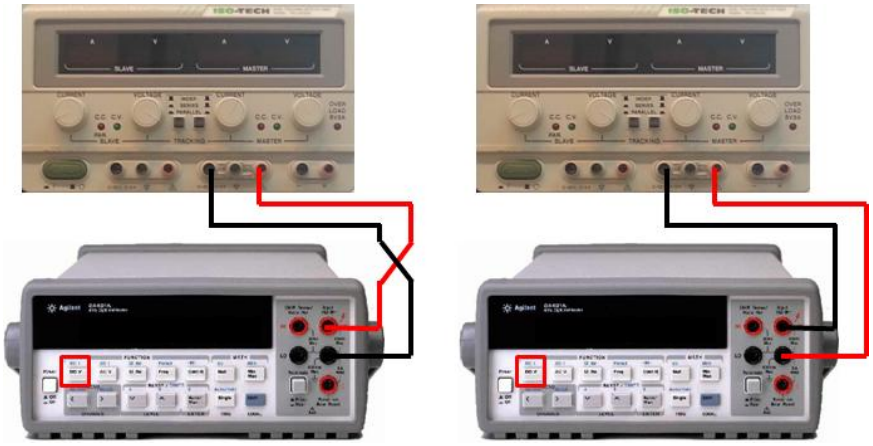
Electric DC voltage:

- Measure the 5V DC voltage configured in task **LAB1** with the *voltmeter*. Configure the instrument by following these steps: **1)** Turn both devices OFF; **2)** Connect them as indicated in Fig. 4a; **3)** Turn the multi-meter ON and press **DC V** in order to configure it as DC voltmeter (the display shows the message "VDC"); **4)** Finally, turn the DC power supply ON.
- Repeat measurements by reversing output connections at the voltmeter (Fig. 4b)

Electric DC current:

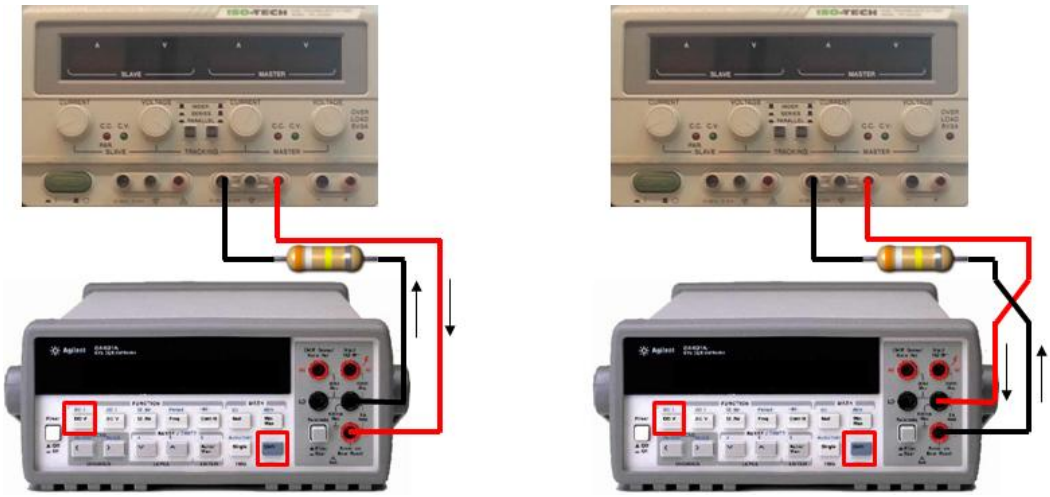
- Keep this 5V DC voltage and connect a **1 Kohm** resistor to measure the electric DC current flow with the *ammeter*. As previously, **1)** Turn both devices OFF. Make the connections of Fig. 5a; **2)** Turn the multi-meter ON and select **DC I** (**SHIFT** > **DC V**) to configure it as an ammeter (the display shows the "ADC" message); and **3)** Turn the DC power supply ON.
- Repeat measurements by reversing output connections at the ammeter (Fig. 5b)

***Figure* 3.** Output connection and multi-meter configuration for measurement of electric resistance.



(a) (b)

***Figure* 4.** Measuring electric DC voltage from the supply with the voltmeter; a) Forward; b) Reverse.



(a) (b)

***Figure* 5.** Measuring electric DC current flow. Arrows indicate flow direction a) Forward; b) Reverse.

3 From the electric diagram to the Bread-board prototype

At this point, it becomes necessary to define symbols for representing the instruments, electronic components and their electrical connections. This will not only be used jut to drawing the schematics of electronic systems but also for understanding their behavior, which is essential in signal analysis and electronic design.

Fig. 6 shows basic symbology and common standard conventions used in wire connectivity. In general, each element is a *dipole* and its terminals are connected to other dipoles. The positive pole of instruments is represented by "+" (Fig. 6a and 6b), and the resistor symbol is depicted in Fig. 6c. More than three connections between wires and/or terminals are indicated by a "point", whereas a "bridge" (or the omission of points) means a crossing of unconnected wires (NC). Finally, the GROUND terminal (Fig. 6e) is a common reference used in electrical variables.

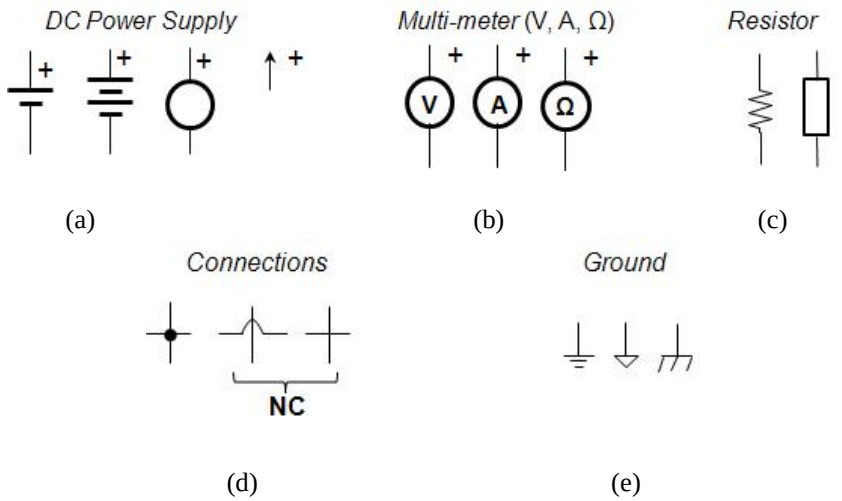


***Figure* 6.** Basic symbols of the elements shown in this document.

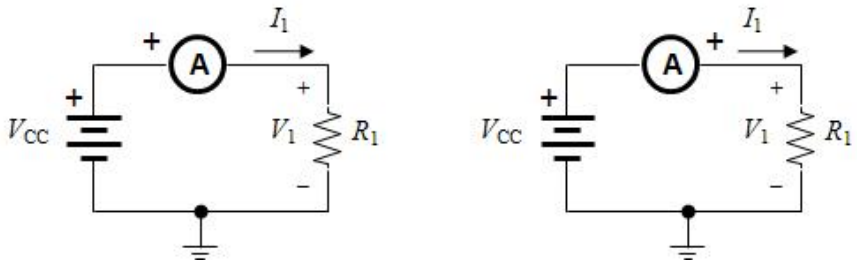
In this sense, a schematic diagram for the current measurement layout of Fig. 5 is depicted in Fig. 7. An arrow represents the direction of I_1, which flows from the positive to the negative pole of the power supply. By convention, the entrance point at the resistor sets the positive sign of its voltage drop (V_1). Finally, the supply V_{CC}, the ammeter (A) and the resistor (R_1) form a *closed path* (or *mesh*), whereas a *node* is any connecting point between two (or more) terminals.

This convention is similar to that used by the multi-meter. By default, electric currents ENTERING the red terminal are read positive[3] by the multi-meter. So in the first situation of Fig. 7a, the value showed in the display matches to I_1, both in value and sign, whereas in the second one the sign is reversed $-I_1$.

Another element, not considered an instrument, but essential when experimenting with electronics, is the test board (Fig.8). This board is known as the *bread-board* and it is where an electronic design is previously mounted and tested before their commercial implementation on a printed circuit board (PCB).

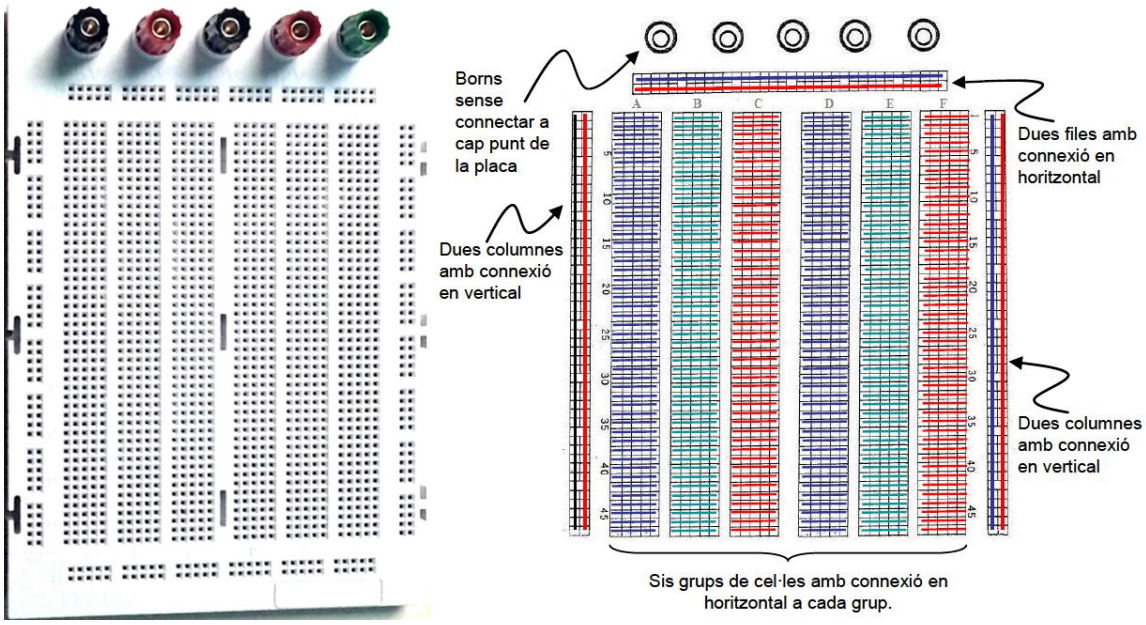
The breadboard have **five unconnected terminals**, **two columns, each vertically connected** (left and right); and **two rows, each horizontally connected** (top and bottom). In addition, the central part have **six groups of cells** (from A to F), each with 47 x 5 holes horizontally connected but vertically unconnected. Knowing this layout is important to develop the circuit connections previously designed on a schematic. Mainly, it is important to place the components according to the schematic and ensure that terminals and wires are connected properly. Using terminals for common connections, such as the GROUND, developing as fewer connections as possible in the breadboard and using colors for assigning groups of connections (i.e: black for ground connection, red for + or grey for -); is important to avoid possible problems and to allow errors to be detected quickly and easily.

[3] A similar criterion applies to the voltmeter, which takes as positive all drops caused by electric currents ENTERING the red terminal, and negative otherwise.



(a) (b)

***Figure* 7** Electric diagrams and variable conventions using the DC current measurement layout in Fig. 5.



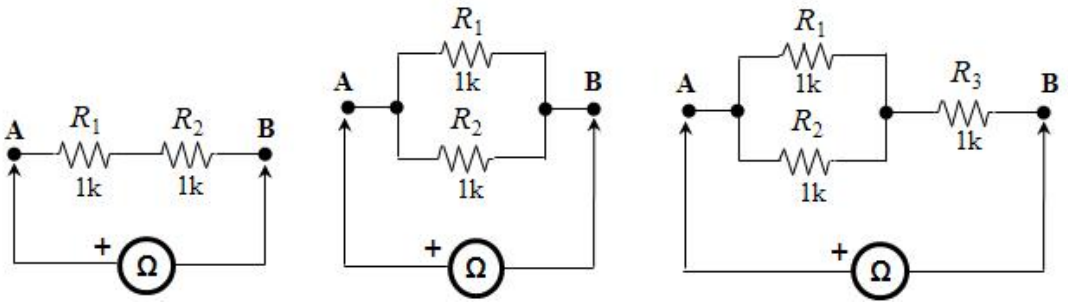
(a) (b)

***Figure* 8.** Overview of the breadboard: a) Aerial view; b) Internal connections of holes.

Task LAB3: Build the simple circuits of Fig. 9 on the breadboard and obtain experimentally their electric resistance:

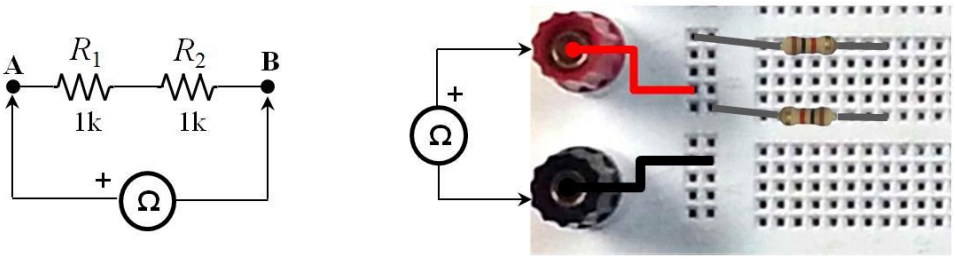
- In the first schematic; **1)** Follow the breadboard distribution in Fig. 10; **2)** Determine the theoretical value between A and B; and finally; **3)** compare with experimental results.
- In the remaining circuits (Fig. 9b and 9c), **1)** Use the information in Fig. 8 to guess the connections you need to make and; **2)** Proceed with the calculations and measurements.

REMARK: The electric resistance between two points, A and B, is measured by **DISCONNETING ALL SOURCES** and connecting the ohmmeter **IN PARALEL**. **NEVER** touch the terminals with your own hands while carrying out this measurement.



(a) (b) (c)

***Figure* 9.** Electric diagram of the circuits in Task LAB3: a) Series association; b) Parallel association; c) Series-parallel connection.



(a) (b)

***Figure* 10.** Mounting example of the series circuit. a) Electric diagram; b) Breadboard layout

Task LAB4: Using a V_{CC} = **5V** at the input of the series circuit (Fig. 11a) determine the DC current flow in the close path *I* and the voltage drop at all resistors V_1 and V_2.

Measurement of *I*:

- **1)** Set the output supply to **5V**, if not set already; **2)** Make sure the multi-meter is configured as ammeter (**DC I**) and turn OFF both devices for the moment. **3)** Mount the series circuit again and connect the instruments (Fig. 11b), (use the breadboard layout in Fig. 12a if you need it). Make sure you use the FUSE ON REAR PANEL terminal as positive of the ammeter; **4)** Turn both devices ON and annotate the value in the display. **5)** Compare with its theoretical value.

Measurement of V_1 and V_2:

- **1)** Turn OFF the DC power supply and disconnect the ammeter; **2)** Change to the voltmeter **(DC V**); **3)** Place the connections as in Fig. 11c (or Fig. 12b) and make sure you use the ***V*Ω** terminal as positive of the voltmeter; **3)** Turn the supply ON and annotate the value V_1.
- **1)** Without turning the devices OFF, disconnect the voltmeter and connect it in parallel with R_2 (Fig. 11d); **2)** Annotate the measure V_2 3) Finally compare both V_1. And V_2 with their theoretical values.

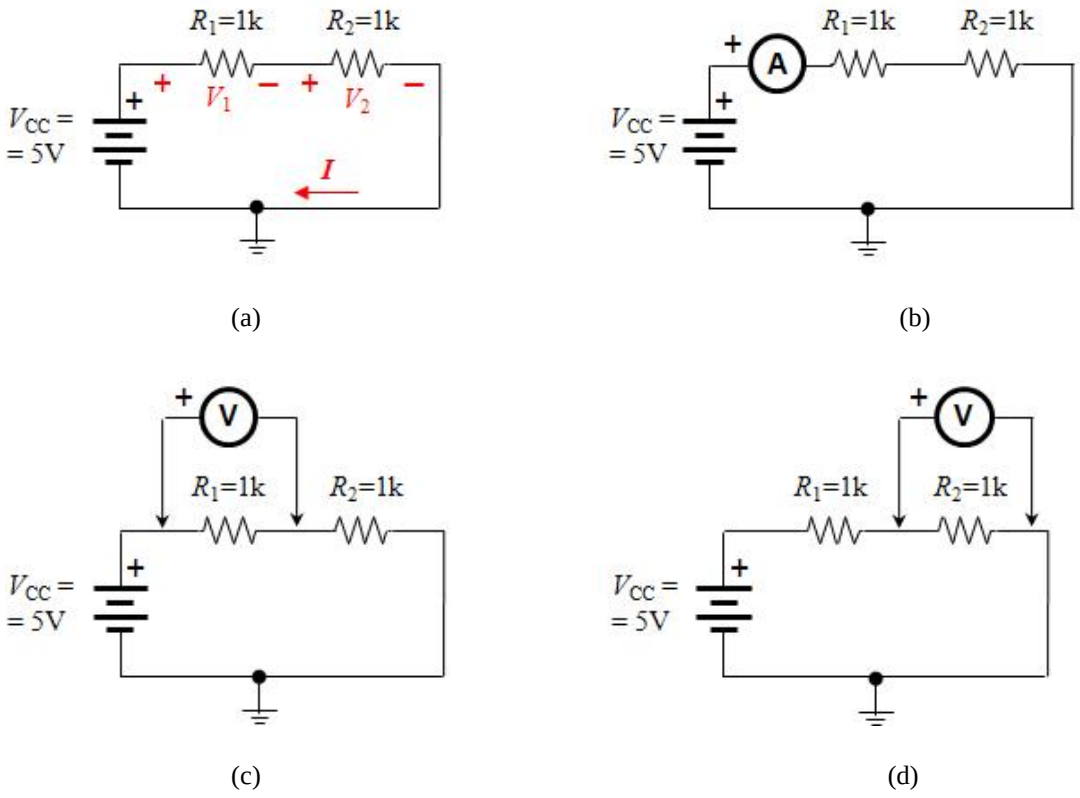


***Figure* 11.** Electric diagrams of Task LAB4. a) General diagram and electrical variables of interest; b) Measuring I; c) Measuring V_1; d) Measuring V_2.

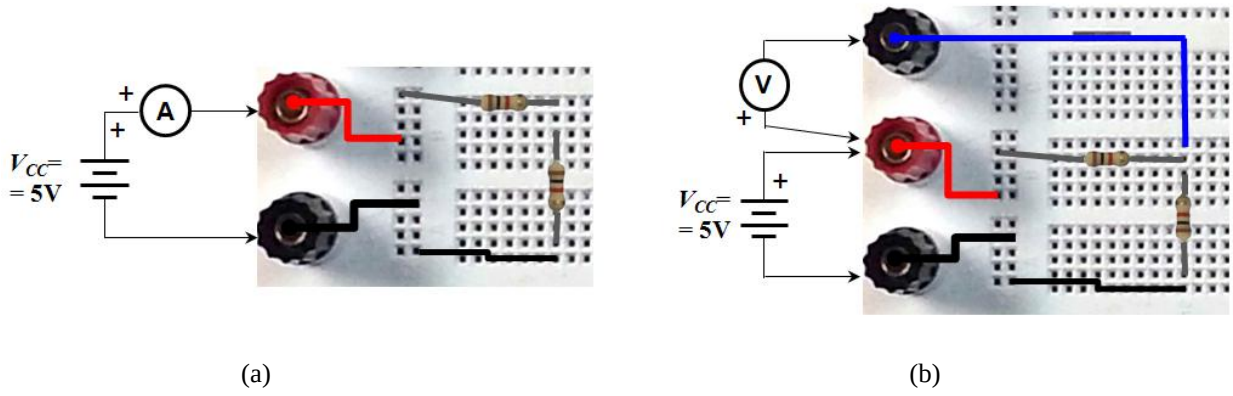


***Figure* 12.** Two possible breadboard layouts for measuring; a) DC current I; b) and V_1.

1st REMARK: For measuring electric current flow, you must **OPEN** at the branch point of measurement and close the circuit by connecting the ammeter **IN SERIES**. Electric voltage drop, on the other hand, must be measured by connecting the voltmeter **IN PARALLEL**.

2nd REMARK: DO NOT DISMOUNT the circuit. You'll use it again in the following sections.

4. The Waveform function generator

The *waveform function generator* is a device for generating time-varying periodical[4] signals. In this school there are three models available depending on the lab and workstation (Fig. 13): a) the **33220A** from Agilent; b) the **GF-855** from Promax; and c) the **HM8130** from Hameg.

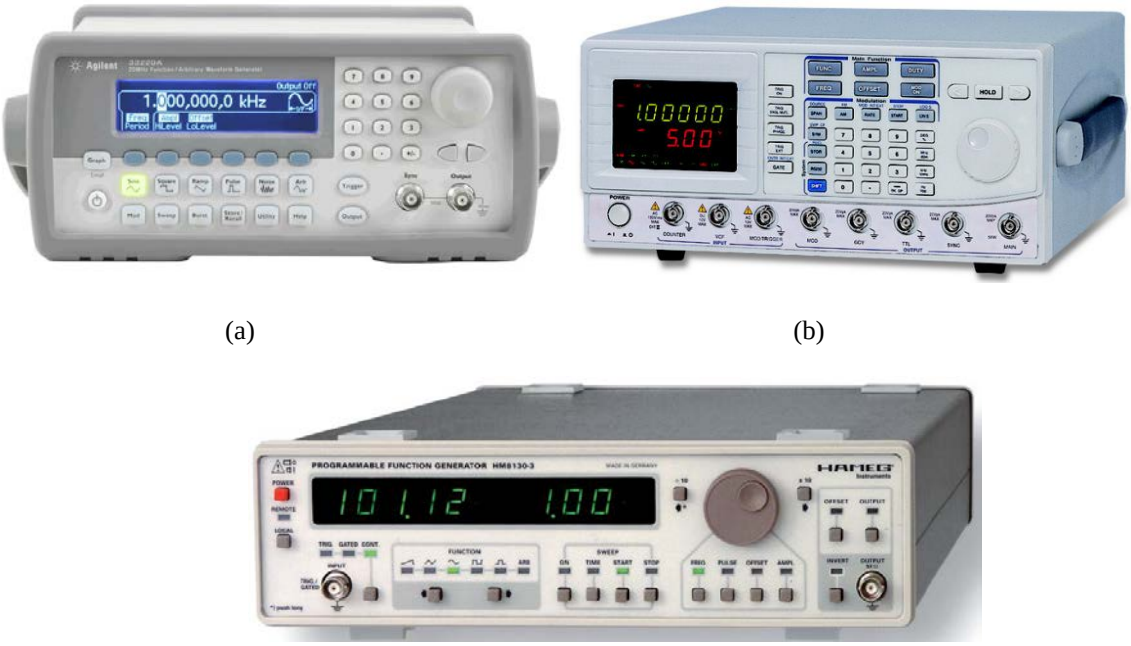
Different symbols may be used depending on the waveform type at the output (Fig. 14a). In this case, a minimum of four parameters need to be set (Fig. 14b): 1) the *shape* (FUNC: **saw tooth, square, sinusoid or pulse**[5]); 2) the *magnitude* (AMP: voltage variation range); 3) the *frequency* (FREQ: number of repeated patterns within a second); and 4) the *offset level* (OFF: DC voltage added to the zero-reference level). This devices sources the output through a type of terminal known as BNC[6] connector, which is labelled with a **50Ω** value (or 60Ω in certain models) indicating its output resistance.

Task LAB5: Learn to use the waveform function generator and get acquainted with the controls and configuration process. Set a **5V-peak sinusoid without offset and a frequency of 100Hz**. Make the following steps to measure its "rms" value with the voltmeter (Fig. 15). The process may be slightly different in other generator model:

- **1)** Turn the generator on with the POWER button. **2)** Select the sinusoid waveform **FUNC**(**TION**) option (red box), or select the **SINE** option if you use the 33220A model. **3)** With the **FREQ** option, configure the 100Hz value with the keypad (blue box), or move along the digits (orange box) with the buttons in the green box and set the frequency value with the roller. **4)** Repeat the preceding step with the **AMP(L)** option, and set a 10V peak-to-peak voltage, or a 5V-peak voltage depending on the device model. **5)** Repeat again in order to set a 0V offset (**OFF** button). **6)** Connect the BNC cord between generator and multi-meter. Make sure you use the **50Ω** and the ***VΩ*** terminals of both devices. **7)** Select the **AC V** option in the multi-meter. **8)** Finally, enable the generator output by means of the OUTPUT **ON/OFF** option if you're not using the GF-855 model and annotate the measure.

> **REMARK:** Many students in this school pass through the lab every day and they alter instrument configurations constantly, including this device. For this reason, the preceding procedure may not be exactly. If that's your case, a good solution may be to load initial manufacturer configurations (except for the HM1380 model which does not have this built-in function) following these instructions:
>
> **33220A:** *Store/Recall* > *Set to default* (from the keypad in the blue box).
> **GF-855:** *Shift* (blue bottom) > *Defau*

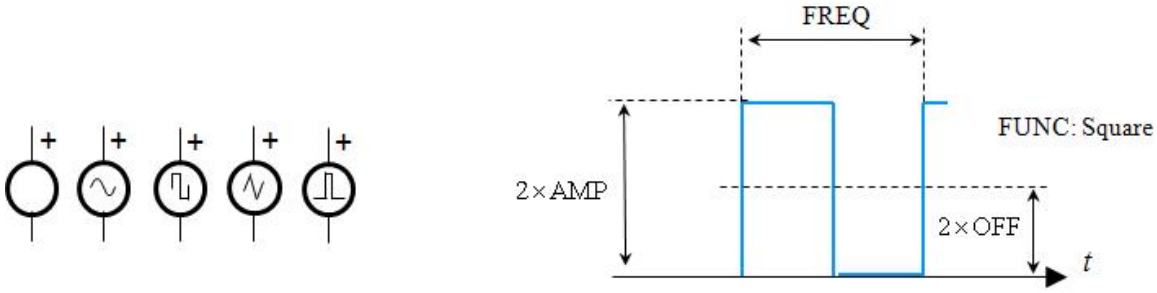
[4] For "periodical" we mean signals with a constant repetitive pattern along the time.
[5] For simplicity, this type is not considered in this activity since it deals with other parameters corresponding to the TTL output, and which are out of the scope of this tutorial.
[6] BNC stands for *Bayonet Neill-Concelman* after its inventors. This is a very popular closing mechanism (similar to a *bayonet*) characterized for being of fast connection and having great noise immunity.



(a) (b)

(c)

***Figure* 13.** Waveform generators at the labs of the EPSEVG: a) 33220A from Agilent (L-106); b) GF-855 from Promax (L-104); c) HM8130 from Hameg (L-104).



(a) (b)

***Figure* 14.** a) Basic symbols for representing the sources of time-varying signals in schematics (from left to right: *generic*, *sinusoid*, *square*, *saw tooth*, *pulse*); b) Basic voltage and time parameters which configured by means of the function generator.

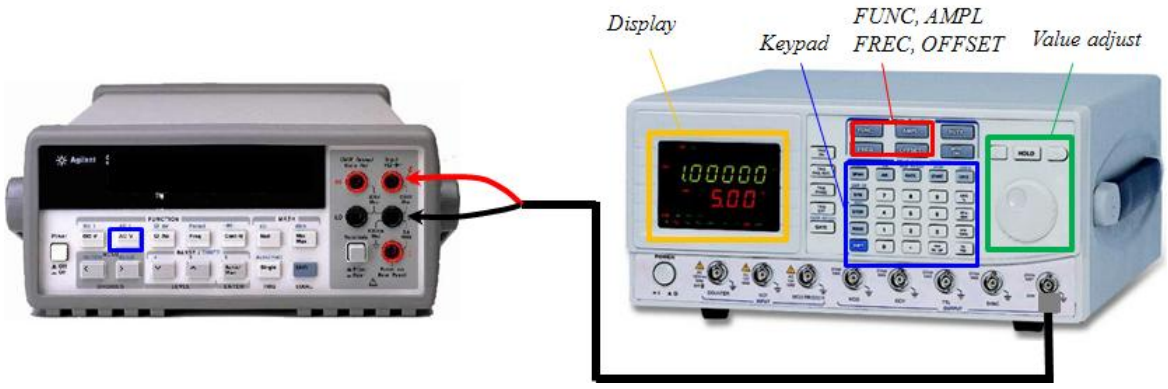


***Figure* 15.** Connection between generator and multi-meter for measuring rms (AC) voltage.

Task LAB6: Replace the DC power supply from Fig. 11 by the waveform generator and repeat the voltage measures in the resistors, in rms or AC mode. Maintain the settings of the previous task.

REMARK: The theoretical expression of a sinusoid is:

$$v(t) = V_{OFF} + V_{\max} \sin(2\pi ft) = \frac{OFF}{2} + \frac{AMP}{2} \times \sin(2 \times \pi \times FREQ \times t) \quad (4)$$

5. The oscilloscope

Perhaps, the *oscilloscope* is the most sophisticated device of the laboratory because of the huge number of control buttons and rollers; specifically necessary to observe time-varying signals on screen.

Two models can be found in the labs (Fig. 16). The **DSO3062A** from Agilent and the **HP54603B** from Hewlett Packard. Both are digital instruments which own a wide variety of functions. However, in this tutorial only the first model is considered in detail, since it is common at the lab, even though settings can be adapted easily to the second model.

In the frontal panel of the **DSO3062A** model, two separated sections can be found: the *screen* and the *control panel* (Fig. 17). TWO signals can be viewed at a time from the input terminals, **channels CH1** and **CH2** respectively, both located at the bottom part of the control panel (red box). Connecting a BNC probe is necessary to sense the signals and watch them on screen.

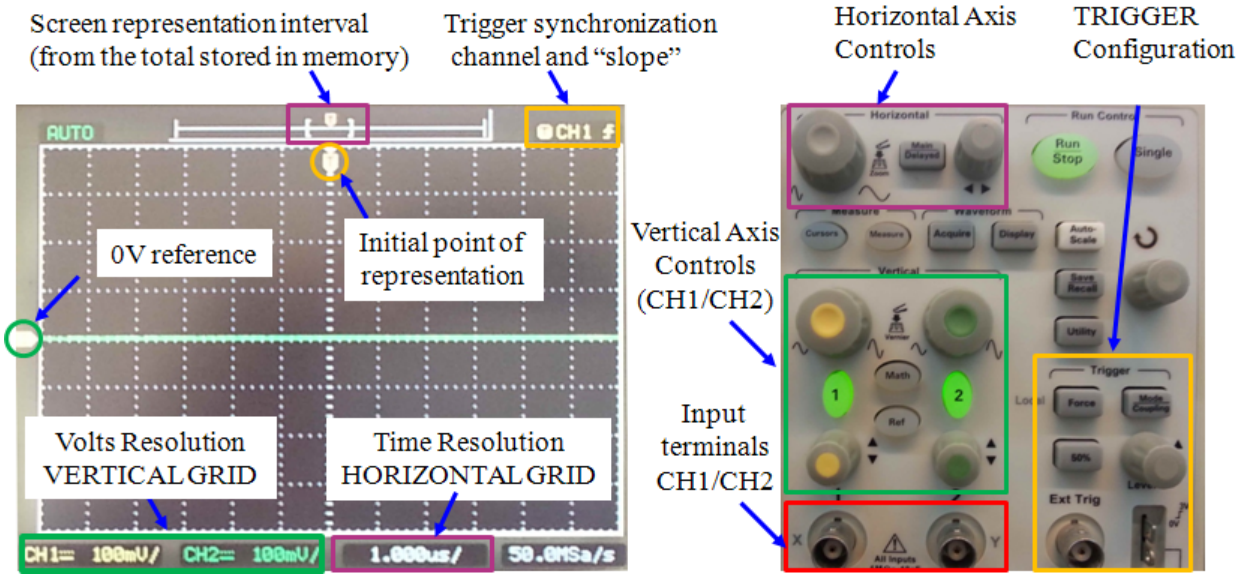
Configuring the instrument correctly not only is important for viewing the signals but also to understand the meaning of symbols, values and messages on screen[7]. The two values from the left bottom part, **100mV/,** (Fig. 17a) correspond to the grid resolution of the vertical axis of both channels (yellow and green for CH1 and CH2, respectively), whereas the white value just on the right, **1µs/**, is the time resolution of the horizontal axis. On the other hand, the numbered arrows left central part of the screen place the ZERO-voltage reference of both channels, whereas the arrow on the top part of the screen (labelled with a "T" concerning to the TRIGGER mechanism) establishes the signal reference[8] and the time point in order to allow signals to be fixed on the screen.

As an example, If the sensibility is set to 100mv-per-division (or equivalently 100mV/) the voltage range on screen (8 vertical squares; 8/) is **800mV-peak-to-peak** (or **400mV-peak**), whereas on the horizontal axis, the screen time width is **12µsegons** for a 1µs/ sensibility (12 squares).

[7] For simplicity, not all the oscilloscope functions will be explained either. See the oscilloscope manual available on the Atenea Campus.
[8] The digital oscilloscope works in REAL-TIME. This means that voltage data is sampled CONTINUOUSLY from the input terminals. Since the buffer memory is finite, and the screen is not wide enough either, the user must specify the INITIAL portion of representation. This is, precisely, the goal of the TRIGGER mechanism, which also attempt to stabilize the periodic signals on screen.

(a) (b)

***Figure* 16.** Oscilloscope models available at the EPSEVG labs. a) DSO3602A from Agilent; b) HP54603B from HP



(a) (b)

***Figura* 17.** DSO3602A's front panel. a) Screen; (b) Configuration and control knobs. Each color references to a group of controls specified within boxes. *Green* – Voltage sensibility; *purple* – Time sensibility; and *orange* – Trigger controls, among others.

Voltage parameters are configured with the control functions in the VERTICAL panel (Green box in Fig. 17b). Activation of CH1 and/or CH2 is carried out through the push buttons 1 and 2, respectively. The zero-voltage reference is set by means of the bottom rollers in this panel, whereas the voltage sensibility of the vertical grid is modified through the selectors located over the activation knobs.

On the other hand, time control is carried out through the HORIZONTAL menu (purple box). The window width is modified through the selector on the left, whereas moving along the waveform stored in the buffer is carried out by means of the roller on the right.

Task LAB7: Learn how to use the oscilloscope for viewing signals on screen, by the following instructions:

Basic configuration:

- **1)** Turn the waveform generator ON and configure the previous settings (5V-peak sinusoid and 100Hz-frequency) if they are not set already. **2)** Connect a BNC-BNC probe between the 50Ω generator's output and the channel CH1 (Fig. 18). **3)** Turn the oscilloscope ON and, follow these steps to observe the signal, once the grid appears (Fig. 17a):

  A) ***Vertical Panel*** > **"1-knob"** > *Coupling* > GND: The input signal disappear from the screen and a horizontal line shows the zero-voltage reference of CH1. Use the yellow roller to place this line at the center of the screen.
  B) ***Vertical panel*** > **"1-knob"** > *Coupling* > DC: The screen shows the waveform trace again.
  C) ***Vertical panel*** > **VOLTS/** (yellow selector): Change the voltage resolution to **2V/**
  D) ***Horizontal panel*** > **TIME/** (left selector from the horizontal menu): Set the time resolution to **1mseg**/

  REMARK: At this point, you should see a sinus of **10 grid positions** (or squares) wide in the horizontal axis, due to the fact that T = 1/FREQ = 10mseg. Likewise, the vertical range is **5 grid positions** wide (2.5 band-to-band beyond the zero-reference voltage) in the vertical axis.

- **2)** Access the TRIGGER menu by pressing the "**Mode/Coupling"** knob at the right in the control panel (orange box). Configure the following options:

  Mode (1) = "Edge". **Source** = "CH1". **Slope** = "Ascending". **Mode** (2) = "Auto". **Coupling** = "DC".

  3) Move the **LEVEL** roller (a discontinuous line appears and the text shows the activation threshold DC level on screen. **3)** Move this line up to "2V" and observe how the signal shifts slightly along the time axis to set the 2V-level reference at the center of the screen.

Coupling configuration:

- **1)** In the waveform generator, change the offset settings of the sinusoid to ***OFF* = 2V**. **2)** Use the Trigger to fix the signal on screen. **3)** Adapt the vertical axis to enclose the signal as **LARGE** as possible on the screen, and the horizontal axis to observe **4 CYCLES**.
- Configure the oscilloscope in AC mode (***Vertical Panel*** > **"1-knob"** > *Coupling* > AC). Comment both results:

***Figure* 18.** Oscilloscope connection for visualizing time-varying signals from the waveform generator.

1st. REMARK: The coupling mechanism is generally used to **HIDE** (NOT TO REMOVE) the average (or DC) input component from a signal. As such, the signal is forced to have a symmetric representation on screen, despite the 2V-level offset. This is done when the AC mode is selected. This mechanism is extremely useful to observe small AC components overlapped in very high DC components, which sometimes are of interest in order to understand the behavior of certain electronic systems.

2nd. REMARK: All configurations explained in this task are considered ESSENTIAL for correct instrument usage so, most probably, you'll need to repeat them again during this course. Procedures also apply to CH2, which can be viewed with CH1 simultaneously. As the waveform generator, instrument configuration may be altered severely over students by the lab. In these situations, it may be wiser to upload the manufacturer initial configurations:

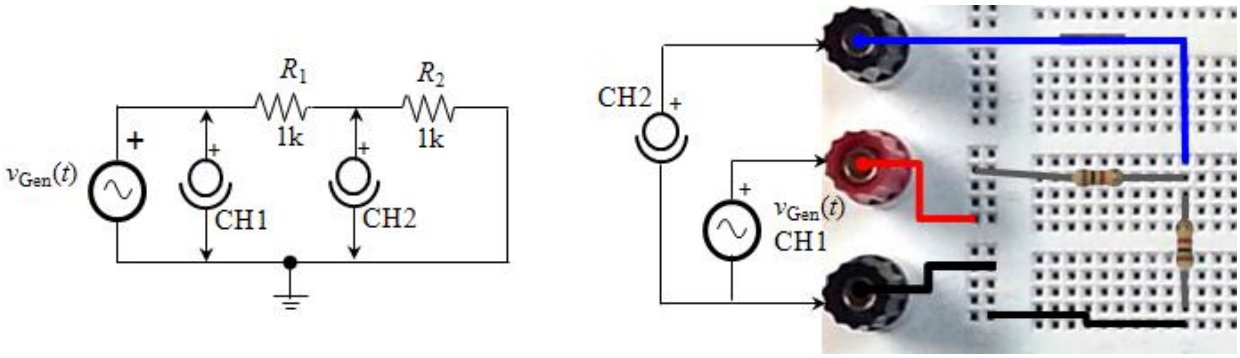
- In the menu: ***Save/Recall*** > *Storage* > *Set-up* > *Manuf.*

Other device utilities (**optional**):

- Take the time to review other interesting configuration options from the oscilloscope which could be of interest for you, such as **1)** the ***Measure*** button for displaying time and voltage measures automatically; **2)** the ***Cursor*** menu to narrow the measures; 3) or the ***Math*** menu for developing mathematical operations with both channels.

Task LAB8: Now connect the waveform generator at the input of the series circuit of Fig. 11, and the CH1 input channel in parallel. Represent the voltage waveform in each resistor (Fig. 19).

- **1)** Mount the circuit of Fig. 11a. if it's not mounted already. **2)** Use a "T" connector at the CH1 input of the oscilloscope and connect the generator output, $v_{Gen}(t)$, by means of a BNC-BNC probe (Thus, you'll to use an additional prove connected at the breadboard (Fig. 19b). Keep the previous sinusoid configuration (**5V**-peak; ***f* = 100Hz** and ***OFF* = 2**. **3)** Connect the other cannel, CH2, in parallel with the second resistor to measure $v_{R2}(t)$ and represent its waveform shape. Do not forget coupling both channels in DC mode.



(a) (b)

***Figure* 19.** Oscilloscope and waveform generator connection for measuring the voltage drop at $v_{Gen}(t)$, and, $v_{R2}(t)$. a) Connection diagram) Breadboard connection.

Differential mode (floating-point voltaje):

- Now, disconnect CH2 and connect this channel in parallel with the first resistor (all positive terminals from the generator, CH1 and CH2 must be TOGETHER. The negative pole of CH2 must be connected between R_1 and R_2). **3)** What is the problem?
- **1)** Undo the last change and connect back channel CH2 in R_2. **2)** Now configure the oscilloscope in *differential mode* (**MATH** *button* > *Operation* > **1 – 2**). This action will generate a new purple trace on screen corresponding to the point wise subtraction CH1-CH2, which is in fact $v_{R1}(t) = v_{Gen}(t) - v_{R2}(t)$

> **REMARK:** Both negative poles of CH1 and CH2 are **INTERNALLY CONNECTED**. As such, connecting them at different circuit points causes short-circuit and unpredicted circuit behavior may be of severe consequences.

Annex 1 – Results form

REMARK: Students must **PRINT OUT THIS FORM** and **BRING** it the day of the lab session.

UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH Escola Politècnica Superior d'Enginyeria de Vilanova i la Geltrú	EEL
Electronic Systems (SIEK) **Lab Activity 1**	
Students:	**Date:**

1 DC Power Supply

- **Task LAB1:**

I_{LIMIT} = _____ V_{FONT} = _____

2 Multi-meter

- **Task LAB2:**

2.1 Electric resistance measurement

	R_1	R_2	R_3	R_4	R_5
$R_{nominal}$ (Ω)					
$R_{Óhmetre}$ (Ω)					
Error (%)					

2.2 DC voltage measurement

$V_{SUPPLY(\text{Multi-meter})}$ = _____ $-V_{SUPPLY(\text{Multi-meter})}$ = _____

2.3 DC current measurement

$I_{R(1k\Omega)}$ = _____ $-I_{R(1k\Omega)}$ = _____

3 From the electric diagram to bread-board prototyping

- **Task LAB3:**

3.1 Series/parallel resistor association

	Series Circuit	***Parallel Circuit***	***Series-parallel Circuit***
$R_{Teòrica}$ (Ω)			
$R_{Òhmetre}$ (Ω)			

- **Task LAB4:**

3.2 Electric DC measures in the series circuit

	I	V_1	V_2
Theoretical			
Multi-meter			

4 Waveform generator

4.1 AC voltage measurement from the generator (rms value)

- **Task LAB5:**

$V_{AC(\text{Multi-meter})}$ = _____

4.2 Electric AC measures in the series circuit

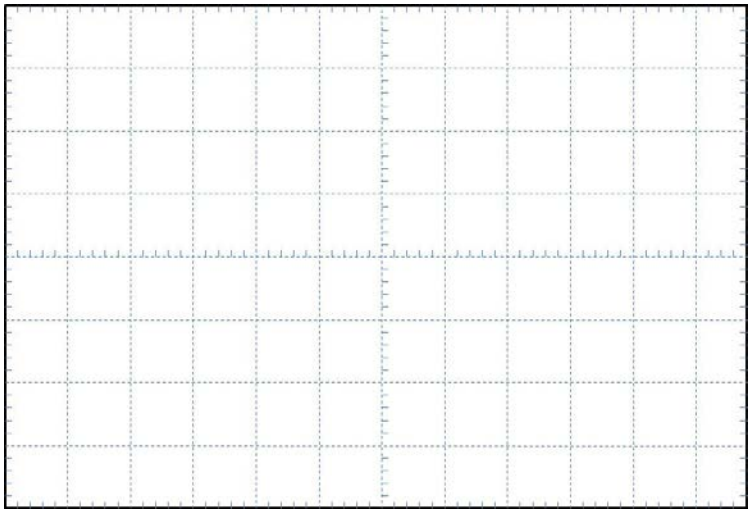
- **Task LAB6:**

	$V_{1(AC)}$	$V_{2(AC)}$
Theoretical		
Multi-meter		

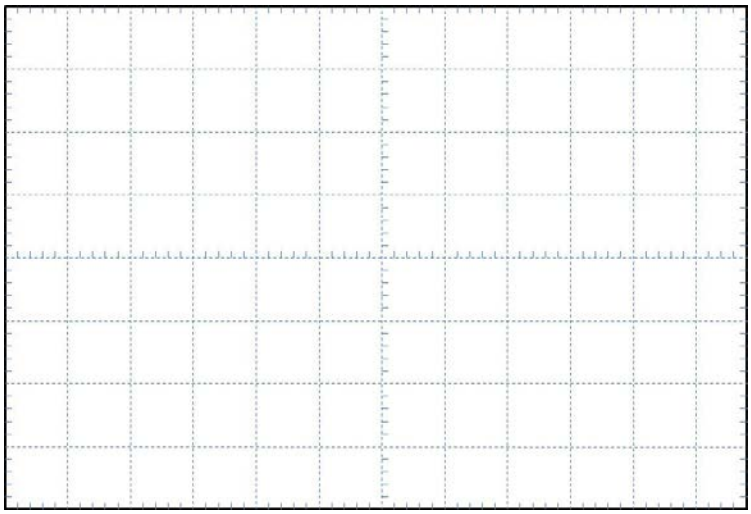
5 The Oscilloscope

- **Task LAB7:**

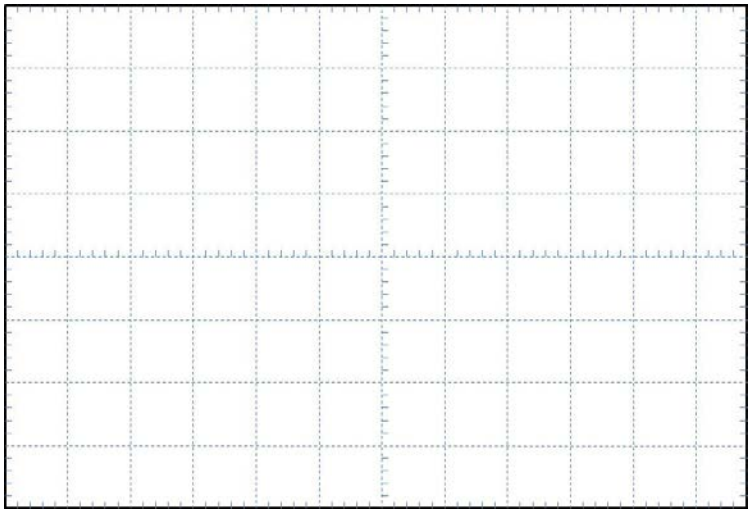
Basic oscilloscope configuration

	**CH1** VOLT/: **2V/** **CH2** VOLT/: **-----** **TIME**/: **1msec/** **Coup: DC** **Zero POS: 0V**

Coupling setting with OFF = 2V and DC mode

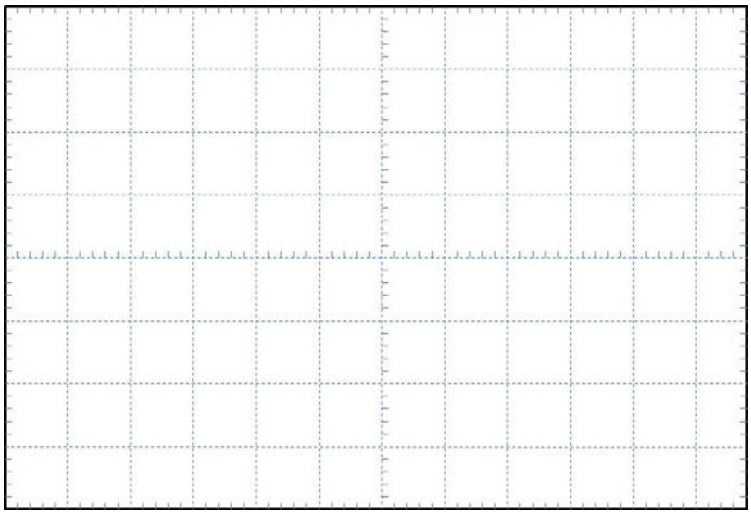
	**CH1** VOLT/: **CH2** VOLT/: **-----** **TIME**/: **Acob: DC** **Zero POS:**

Coupling setting with OFF = 2V and AC mode

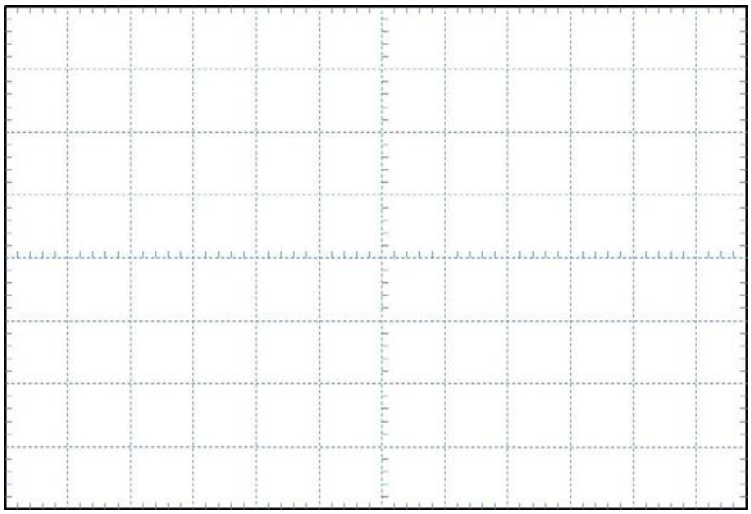
	**CH1** VOLT/: **CH2** VOLT/: ---- **TIME**/: **Acob:** AC **Zero POS:**

- **Task LAB8:**

Representation of $v_{Gen}(t)$ and $v_{R2}(t)$ in the series circuit

	**CH1** VOLT/: **CH2** VOLT/: **TIME**/: **Acob:** DC **Zero POS:**

Representation of $v_{Gen}(t)$ and $v_{R1}(t)$ with CH2 and R_1 in parallel

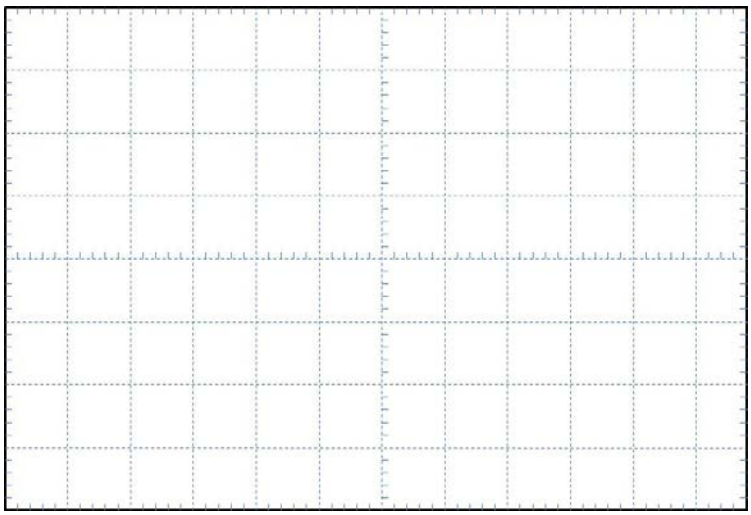
	**CH1** VOLT/: **CH2** VOLT/: **TIME**/: **Acob:** **DC** **Zero POS:**

Explain the problem

_____

_____

Representation of $v_{Gen}(t)$, $v_{R1}(t)$ and $v_{R2}(t)$ using the MATH option

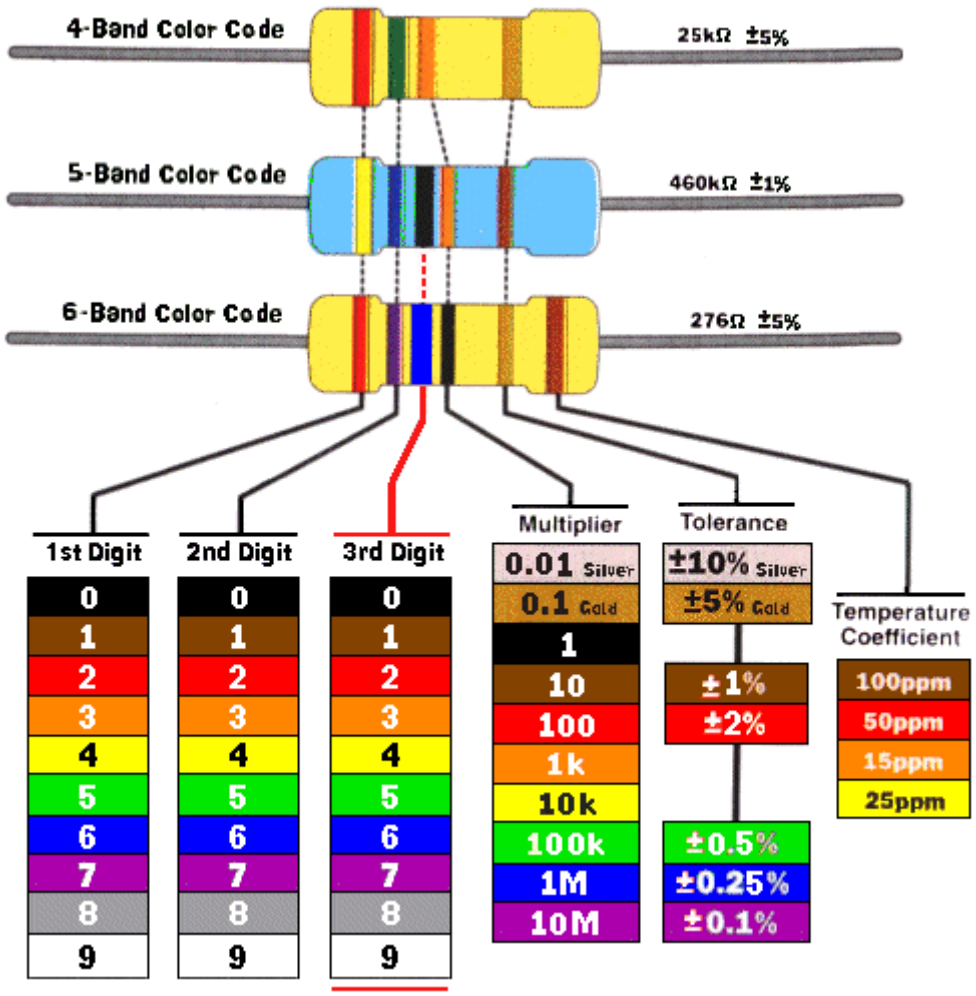
	**CH1** VOLT/: **CH2** VOLT/: **TIME**/: **Acob:** **DC** **Zero POS:**

Explain the configurations in the MATH menu here to view $v_{R1}(t)$ correctly

_____

_____

Annex 2 – Resistor value coding



Lab Activity nº 2. *Time* and *Frequency* domains

Main Goal: Learning how to determine the transient and frequency response of any *Linear Time invariant* system (LTI) in the form of a passive circuit, by means of the transfer function. This goal is not only restricted to a theoretical level but also considers technical development and extends to measurements in order to know such information in real electronic systems.

1. Capacitors and inductors

A capacitor consists of two electrodes separated by an insulating medium called the dielectric. The electric charge q on the electrodes is proportional to the voltage v_c across the capacitor,

$$q(t) = Cv_c(t) \tag{1}$$

where C is the capacitance. The unit is given in *farads* (abbreviated *F*): 1 farad equals 1 coulomb/volt, and habitual values are in the order of microfarads ($1\mu F=10^{-6}F$) or picofarads ($1pF=10^{-12}F$). On the other hand, its electric current is given by the rate of change of the electric charge, so its voltage/current relationship is,

$$i_c(t) = \frac{d\boldsymbol{q}}{dt} = \frac{d(C\boldsymbol{v_c})}{dt} = C\frac{dv_c(t)}{dt}. \tag{2}$$

Table 1 represents the mathematical model of this component both in time and frequency domain. More precisely, using the *Laplace* Transform allows time transitions to be expressed as,

$$\frac{dx(t)}{dt} \xrightarrow{L^{-1}} s \times x(s) \tag{3}$$

where $s \equiv d(\cdot)/dt$ is the *laplacian operator* containing the angular frequency ω,

$$s = j\omega \tag{4}$$

also related to the oscillation frequency $f = \omega/2\pi$ which is expressed in Hz. As such, and with the use of basic theoretical rules (*Ohm's law, Kirchoff law, etc*) it is easy to handle the behavior of reactive components, since knowing its electric impedance X_c is, most of the times, enough for carrying out calculations. This principle is also equivalent in the inductor, whose voltage drop varies with the magnetic field ϕ as,

$$v_L(t) = \frac{d\phi}{dt} = \frac{d(L\boldsymbol{i_L})}{dt} = L\frac{di_L(t)}{dt}, \tag{5}$$

where now L is the inductance, in *henris* (*H*). For this reason both components are considered *duals* (that is replacing i by v and v by i in one equation leads to the other) since their impedances are X_c and $X_{L,}$ respectively.

Task PRELAB0: Search through the Internet, or any manufacturer catalog (such as *RS Amidata*, *Farnell in One*, *Digi-key*, *Google*, etc) a **10nF** and a **10µF** capacitor.

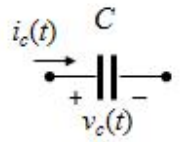
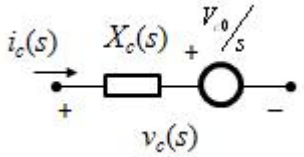
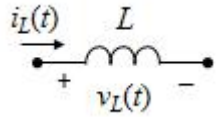
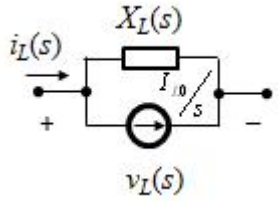
Symbols Capacitor/Inductor	**I-V Characteristics** (time domain)	**Impedance** (frequency domain)	**I-V relationship with initial conditions** (frequency domain)
	$i_c(t) = C\frac{dv_c(t)}{dt}$	$X_c(s) = \frac{v_c(s)}{i_c(s)} = \frac{1}{Cs}$	
	$v_L(t) = C\frac{di_L(t)}{dt}$	$X_L(s) = \frac{v_L(s)}{i_L(s)} = Ls$	

***Table* 1**. Symbols, conventions, and I-V model of the capacitor and the inductor in time/frequency domain.

- Draw their approximate contour outline in the box provided and explain how the capacitor value and tolerance are specified on the package. Indicate polarity if necessary.

2. ‘Step’ response (1st. Order system)

2.1 Definition of the ‘Step’ input signal

Consider a circuit in a black box, such as that of Fig. 1, to which a constant voltage source V_A is applied. The source begins to act thanks to a switch that shorts its terminals at time $t = 0$. Then, the input v_i jumps from 0 to V_A instantaneously as indicated in Fig. 1b. Such a function is called the *step function*. A *unit step function* (Fig. 1c) is defined in time (t) and frequency (s) domains, respectively, as,

$$u(t) = \begin{cases} 0, & t < 0 \\ 1, & t \geq 0 \end{cases} \xrightarrow{L} u(s) = \frac{1}{s}. \tag{5}$$

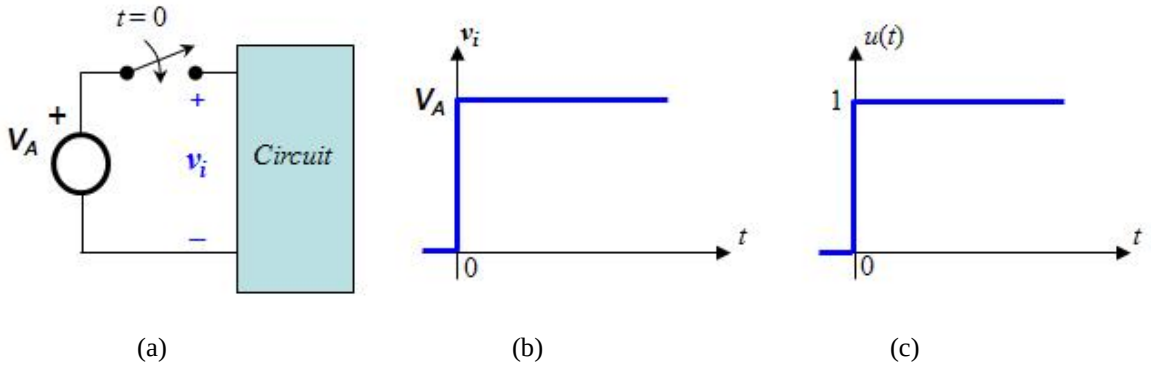
Therefore, a step function that is zero until $t = 0$ and rises up to V_A for $t \geq 0$ is written as $V_A u(t)$:

$$V_A u(t) = \begin{cases} 0, & t < 0 \\ V_A, & t \geq 0 \end{cases} \xrightarrow{L} u(s) = \frac{V_A}{s}. \tag{5}$$

2.2 Step response in 1st. order *RC* circuits

Let us consider the response of the *RC* series circuit in Fig. 2 to an input source of the form $V_A u(t)$ whose initial conditions are zero ($V_{c0} = 0$V). By using a *voltage divider*, the voltage across the capacitor is expressed as,

$$v_c(s) = \frac{X_C(s)}{R + X_C(s)} V_A(s) = \frac{1/Cs}{R + 1/Cs} \frac{V_A}{s} = \frac{1/RC}{s + 1/RC} \frac{V_A}{s}. \tag{6}$$



(a) (b) (c)

***Figure* 1**. Step function. a) Circuit with a constant input; b) Waveform shape of the step function; c) Unit step.

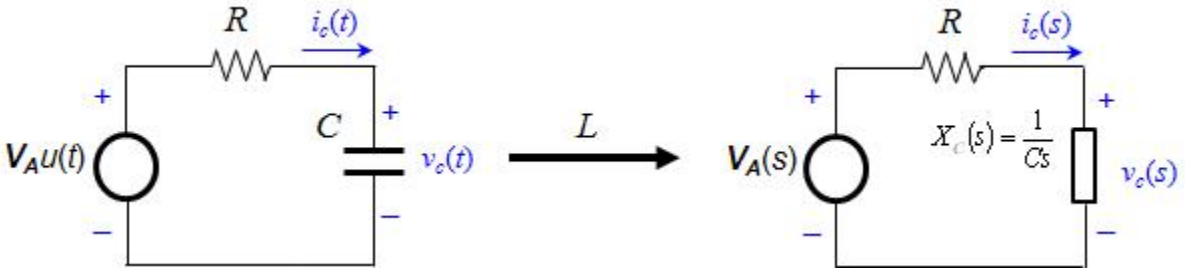


***Figure* 2**. The RC series circuit and its equivalent in *s* domain (zero initial conditions)

This expression has a known inverse transform (see the table in Annex 3), so the voltage across the capacitor is expressed in time domain as,

$$v_c(s) = \frac{1/RC}{s + 1/RC}\frac{V_A}{s} \quad \xrightarrow{L^{-1}} \quad v_c(t) = V_A\left(1 - e^{-t/RC}\right). \tag{7}$$

This signal has the exponential profile of Fig. 3. Since $V_A u(t) = V_A$, the current flow $i_c(t)$ can be determined by subtracting to the input $v_c(t)$ and then dividing by R.

Now we examine the behavior of the series RC circuit from a more physical point of view. Initially, we assume zero voltage across the capacitor for $t < 0$ and in $t = 0$ the source V_A is connected to the circuit. Since the continuity condition in the capacitor requires $\boldsymbol{v_c} = 0$ just after connecting the source, $t = 0+$ (otherwise $i_c \to \infty$ which would destroy the device. See Table 1), at this moment it holds that

$$\boldsymbol{v_R} = \boldsymbol{V_A} \qquad \text{i} \qquad \boldsymbol{i_c} = \boldsymbol{v_R}/R = \boldsymbol{V_A}/R \qquad \text{for} \quad t = 0+.$$

The electric current jumps instantaneously from 0 to $\boldsymbol{V_A}/R$ at $t = 0+$ (Note that an abrupt change in the capacitor's current is possible since this variable doesn't requires to accomplish with the continuity condition). Therefore, the current flows during this interval and the capacitor is charged.

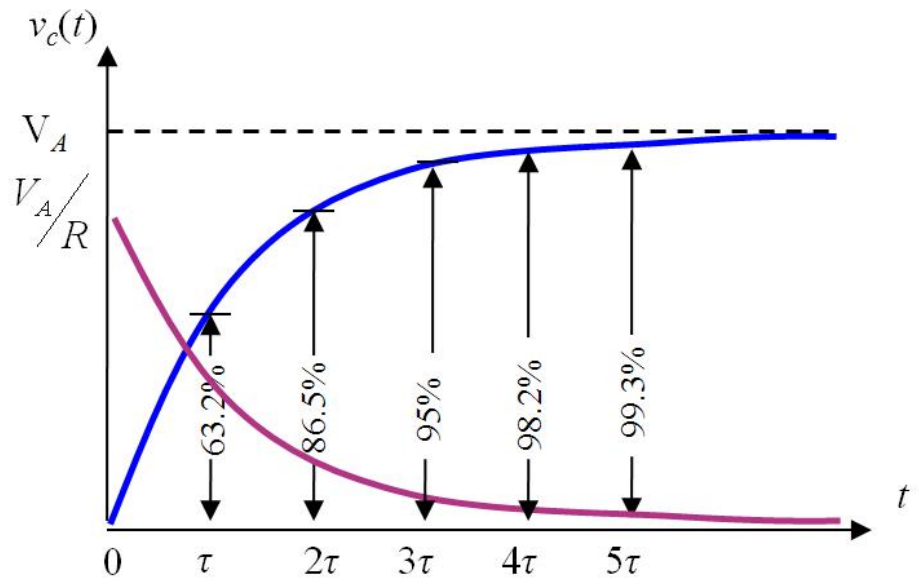


***Figure* 3**. RC series circuit. Output response: V_A (black discontinuous); $v_c(t)$ (blue); $i_c(t)$ (purple).

Since the resistor voltage is $v_R(t) = V_A - v_c(t)$, the current decreases at an exponential rate $e^{-t/\mathrm{RC}}$ until it gets to zero, and the voltage drop becomes $\boldsymbol{v_c} = V_A$. The state of affairs where no further change occurs (theoretically at $t = \infty$) is called the ***steady state*** of the circuit. From a practical point of view, however, the exponential term becomes negligibly small at $t = 5RC$ ($e^{-5} < 0.01$) and the steady state may therefore be assumed at this time.

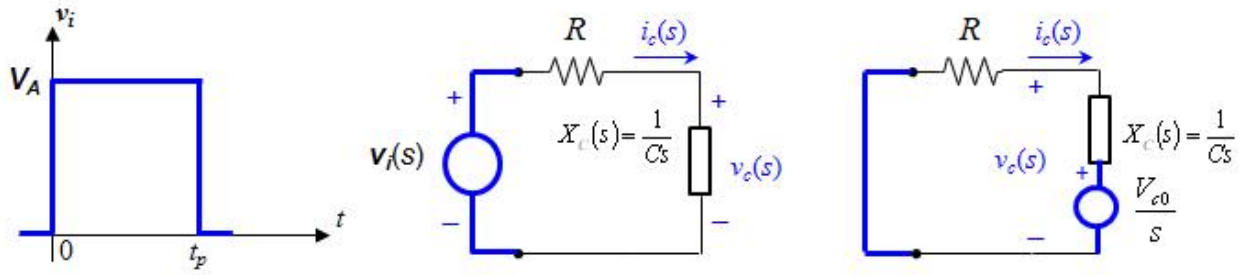
The transient component is also called the ***natural response*** of the circuit since it represents the manner in which passive components (R and C) would response when left to themselves. Additionally, the steady state is also known as the ***forced response*** imposed by the input source at the output. By expressing R and C in terms of the basic units, it is possible to show that the product RC has time dimensions (in seconds). Furthermore, if (6) is rewritten as,

$$H(s) = \frac{v_c(s)}{V_A(s)} = \frac{1/RC}{s + 1/RC} \quad \Leftrightarrow \quad H(s) = H_0 \frac{1/\tau}{s + 1/\tau} \tag{8}$$

the new expression characterizes uniquely the circuit behavior on the variable of interest $\boldsymbol{v_c}$ (the output) in relation to the source V_A (the input). Here, H_0 denotes signal amplification on the steady state ($H_0 = 1$ in this case), whereas $\tau = RC$ is the *time constant* of the circuit. For this reason, expression (8) is often referred to as the ***transfer function*** of the circuit.

2.3 Response to a rectangular pulse (General charge/discharge expression of the RC circuit)

The response of an RC circuit to a *rectangular pulse* (Fig. 4a) is important in electronics since a large number of signals in communication systems have similar shape. As initial conditions in the capacitor vary both at $t = 0$ and $t = t_p$, two time intervals must be considered: 1) $0 < t < t_p$ and 2) $t_p < t < \infty$.



(a) (b) (c)

***Figure* 4**. RC circuit schematics for a rectangular pulse (a). (b) Interval $0 < t < t_p$; c) Interval $t_p < t < \infty$.

Interval $0 < t < t_p$: This interval is equivalent to the situation shown in section 2.2 (Fig. 4b). H, the capacitor voltage at $t = t_p$ is not necessary V_A since it depends on the time constant τ. This voltage is given by (7) as,

$$v_c\left(t = t_p\,-\right) = V_A\left(1 - e^{-t_p/RC}\right) \tag{9}$$

Interval $t_p < t < \infty$: Unlike the previous interval, initial conditions are given by (9) as, $v_c(t_p\text{-}) = v_c(t_p\text{+}) = V_{c0}$. Thus, from Fig. 4.4c, the capacitor voltage is given by the *voltage divider*,

$$v_c(s) = \frac{R}{R + 1/Cs}\frac{V_{c0}}{s} = \frac{s}{s + 1/RC}\frac{V_{c0}}{s} = \frac{V_{c0}}{s + 1/RC} \xrightarrow{L^{-1}} v_c(t) = V_{c0}e^{-\frac{t-t_p}{RC}}. \tag{10}$$

Finally, by using (9) in (10) we obtain,

$$v_c(t) = \begin{cases} V_A\left(1 - e^{-t/RC}\right), & 0 < t < t_p \\ V_A\left(e^{t_p/RC} - 1\right)e^{-t/RC}, & t \geq t_p \end{cases} \tag{11}$$

2.4 Step-by-step procedure for the solution of *RC* circuits to rectangular pulses

The discussion provided in the previous section shows that when a series *RC* circuit is driven by rectangular pulses in different time intervals, the response may be obtained by an easy step-by-step procedure. This methodology avoids using differential equations or Laplace transformations and can be used in any *RC* circuit of just one capacitor. The procedure is the following:

1. Write an expression of the form,

$$v_c\left(t - t_n\right) = V_{c\infty} + \left[V_c\left(t_n\right) - V_{c\infty}\right]e^{-\frac{t-t_n}{\tau}} \tag{12}$$

for the time interval $t_n \leq t < t_{n+1}$, where $\tau = RC$ is the time constant of this interval and t_n is the initial time of the n-th interval, for $n = 1...N$.

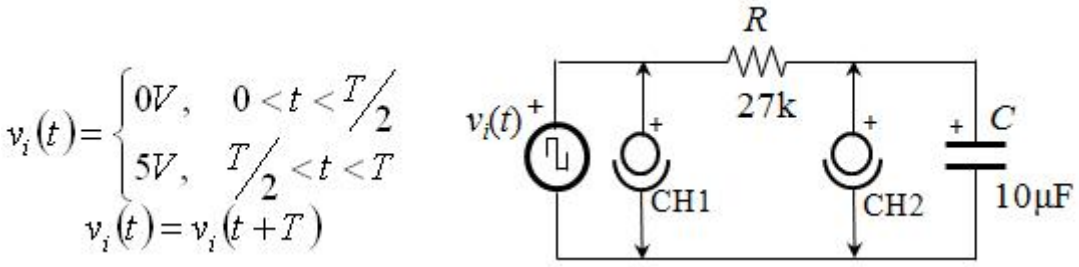
2. Evaluate the steady term $\boldsymbol{V_{c\infty}}$ by examining the circuit when the capacitor voltage has reached the maximum charge/discharge: $\boldsymbol{i_c(\infty) = 0}$ in any case.
3. Use the steady term $\boldsymbol{V_c}(t_n)$, already calculated by means of (12) in the previous interval $t = t_n$, and obtain the new voltage $v_c(t)$ by means of (12)
4. Proceed with interval $n = n+1$ by repeating the three previous steps. In the case of circuits containing a single capacitor, but not in the form of a series RC circuit, first obtain the *Thevenin* equivalent resistance, R_{th}, as seen from the capacitor terminals and repeat the steps described above, using $R=R_{th}$.

Task PRELAB1: In the template corresponding to the PRELAB activities provided at the end of this document (Annex 1), draw the connections corresponding to the series RC circuit in Fig. 5, and the signal waveforms you'll expect to see in the oscilloscope.

- Include the connections of both components and instruments of Fig. 5.5b and indicate the generator function configuration for providing a **SQUARE** signal between **0 and 5V**, with a frequency $\boldsymbol{f}$ **= 0.25Hz** ($\boldsymbol{T}$ **= 4seg**).
- As for the representation of signals, first determine the capacitor voltage expression, $v_c(t)$ using (11) and, then, with the oscilloscope configuration of CH1 and CH2 provided, use the grid to represent the waveforms you'll see on screen.

Task LAB1: Mount the circuit of Fig. 5 on the breadboard, connecting instruments as indicated, and obtain the value of τ experimentally:

- **1)** First, mount the circuit. **2)** Connect the TTL output from the waveform as the input of the circuit $v_i(t)$ (or configure a **SQUARE** signal between **0 and 5V** in the case you use the **50Ω** terminal) and set a frequency $\boldsymbol{f}$ **= 0.25Hz**. **3)** Use the settings of PRELAB1 to configure the oscilloscope and, observing the POSITIVE CYCLE, obtain the measurement for the time constant τ (*settling time* = 5τ). **5)** Compare with τ = *RC*.
- Use a capacitor of **10nF** and repeat the measurements by using the oscilloscope settings that best suits your needs. Draw the waveforms on the plot provided.



(a) (b)

***Figure* 5**. Schematics of the series *RC* circuit for TASK1. a) Expression of the square signal to be configured with the waveform generator. b) Electric diagram including instrument connections.

3. Frequency Response

3.1 Response to a sinusoid input

The mathematical expression for a sinusoid waveform (Fig. 6) and its equivalence in *s* domain are written generally as,

$$x(t) = A\cos(\omega t) \quad \xrightarrow{L^{-1}} \quad x(s) = A\frac{s}{s^2+\omega^2} = A\frac{s}{(s+j\omega)(s-j\omega)} \tag{13}$$

where A is the signal amplitude and $\omega = 2\pi f = 2\pi/T$ corresponds to the angular frequency, expressed in rad/seg. Finding the output response of the RC circuit for a sinusoid input (by means of the *Laplace* method) requires solving a 3rd. order expression of the form,

$$v_c(s) = \frac{1/Cs}{R+1/Cs}v_i(s) = A\frac{1/RC}{s+1/RC}\frac{s}{s^2+\omega^2} = \frac{B_1}{s+1/RC} + \frac{B_2}{s+j\omega} + \frac{B_2^*}{s-j\omega} \tag{14}$$

where B_1 and B_2 are the residues,

$$B_1 = A\frac{(1/RC)^2}{\omega^2+(1/RC)^2} \quad \text{and} \quad B_2 = \frac{A}{2}\frac{(1/RC)^2 - (j\omega/RC)}{\omega^2+(1/RC)^2}. \tag{15}$$

Respectively. So the inverse transform of (14) becomes,

$$v_c(t) = B_1 e^{-\frac{t}{RC}} + B_2 e^{j\omega t} + B_2^* e^{-j\omega t} \tag{16}$$

where B_1 corresponds to the *natural response* of the circuit disappearing with the time *t*, and B_2 is the term forced by $v_i(t)$. Neglecting B_1 and using the *Euler* theorem in (16) lead to

$$v_c(t) = A\frac{1/RC}{\sqrt{\omega^2+(1/RC)^2}}\cos\left[\omega t - \tan^{-1}(\omega RC)\right] = A\times\left|H(j\omega)\right|\times\cos\left[\omega t + \angle H(j\omega)\right] \tag{17}$$

where,

$$\left|H(j\omega)\right| = \frac{1/RC}{\sqrt{\omega^2+(1/RC)^2}} \quad \text{and} \quad \angle H(j\omega) = -\tan^{-1}(\omega RC), \tag{18}$$

are known as the ***module*** and ***phase*** response, respectively, of the transfer function $H(s)$ defined in (8). In other words, the output is another sinusoid of the same frequency ω, but delayed by $\angle H(j\omega)$ radians in relation to the input and corrected by the factor $|H(j\omega)|$.

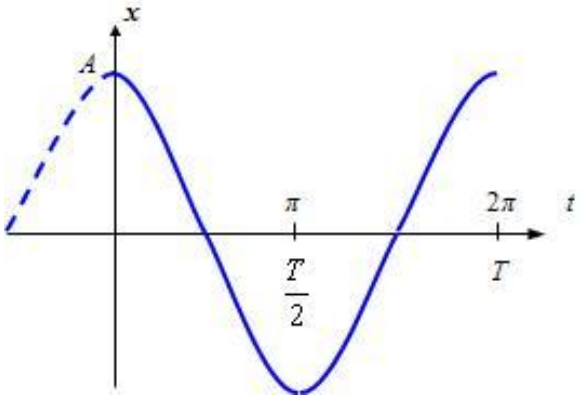


***Figure* 6**. Sinusoid of the form: $x(t) = A\cos(\omega t)$

These two parameters are crucial since they specify circuit behavior at any frequency. In fact, there is a method by which calculations can be extended easily to ANY *LTI* system provided that the focus is on knowing only the steady state of the circuit. This methodology is even valid regardless of the number of resistors, capacitors and inductors included in the network.

3.2 Frequency response in steady-state *LTI* systems

In general, given a *LTI-system* expressed in terms of its transfer function $H(s)$ (Fig. 7), its module $|H(s)|$ is obtained as,

$$\left|H\left(j\omega\right)\right| = \sqrt{H_R^2\left(j\omega\right) + H_I^2\left(j\omega\right)} \tag{19}$$

where "*R*" i "*I*" denote respectively the "real" and "imaginary" (complex) terms of $H(s)$, whereas the phase $\angle H(j\omega)$ is calculated as,

$$\angle H\left(j\omega\right) = \begin{cases} \tan^{-1}\left(\dfrac{H_I\left(j\omega\right)}{H_R\left(j\omega\right)}\right), & \text{si } H_R\left(j\omega\right) \geq 0 \\ \pi + \tan^{-1}\left(\dfrac{H_I\left(j\omega\right)}{H_R\left(j\omega\right)}\right), & \text{si } H_R\left(j\omega\right) < 0 \end{cases} \tag{20}$$

where the units of $\angle H(j\omega)$ are in radians. However, most of the times $H(s)$ has a numerator and a denominator, both containing real and complex terms. In this situations, one can use,

$$\left|H\left(j\omega\right)\right| = \frac{\sqrt{num\left[H_R^2\left(j\omega\right)\right] + num\left[H_I^2\left(j\omega\right)\right]}}{\sqrt{den\left[H_R^2\left(j\omega\right)\right] + den\left[H_I^2\left(j\omega\right)\right]}} \tag{21}$$

to evaluate the numerical value $|H(s)|$, where "*num*" and "*den*" denote numerator and denominator of $H(s)$, respectively. On the other hand, for evaluating $\angle H(j\omega)$ we use,

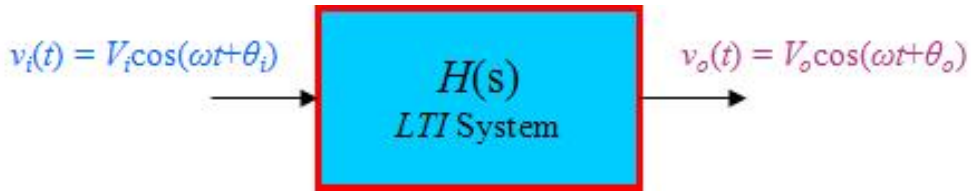


***Figure* 7**. General overview of the frequency response in a LTI-system.

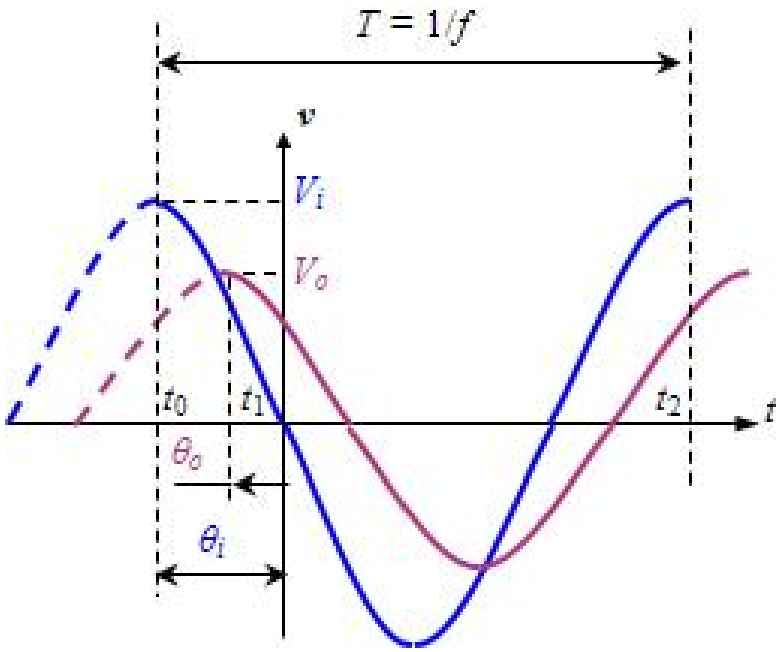


Figure 8. Voltage and time parameters used in the experimental estimation of |H(s)| and ∠*H*(*s*).

$$\angle H(j\omega) = \tan^{-1}\left(\frac{num\left[H_I(j\omega)\right]}{num\left[H_R(j\omega)\right]}\right) - \tan^{-1}\left(\frac{den\left[H_I(j\omega)\right]}{den\left[H_R(j\omega)\right]}\right). \qquad (22)$$

The reader can prove that using (21) and (22) in (8) leads to (18): the module and phase response of the series RC circuit. Furthermore, if we denote $V_i(\omega)$ and $\theta_i(\omega)$ as the input magnitude and phase, respectively, at frequency ω, the output response is given by,

$$V_o(\omega) = |H(j\omega)| \times V_i(\omega) \quad \text{and} \quad \theta_o(\omega) = \angle H(j\omega) + \theta_i. \qquad (23)$$

Fig. 8 shows the most representative points of both input and output signals of the LTI system. In other words, the module $|H(j\omega)|$ is just their output-input peak relation,

$$|H(j\omega)| = V_o / V_i. \qquad (24)$$

whereas the phase delay $\angle H(j\omega)$ is evaluated by measuring the reference points t_0, t_1 and t_2. Then, assuming that $\theta_i = 0$, and therefore $\angle H(j\omega) = \theta_o$, the phase is obtained from the signals as,

$$\angle H(j\omega) = \begin{cases} 2\pi \dfrac{t_2 - t_1}{T}, & \text{if } t_1 \geq t_2 \\ -2\pi \dfrac{t_1}{T}, & \text{if } t_1 < t_2 \end{cases} \quad (25)$$

Task PRELAB2: Using the capacitor value ***C* = 10nF**, represent the waveform signals of the RC series circuit (Fig. 5b) that would be observed on screen if, instead of the square signal input, we use a **sinusoid** with amplitude V_i **= 5V**, **zero offset**, and frequency ***f* = 1 kHz** ($\omega = 2\pi f$)

- Use (18) to obtain module and phase response, and then determine the reference points of Fig. 8 by means of (24) and (25) to carry out this task. Use θ_i **= 0** and fix on screen a random point for t_0 on the horizontal axis. Specify oscilloscope configuration in order to observe on screen **an entire cycle** of both signals in detail.

Task LAB2: Obtain the frequency response of the series RC circuit in the lab.

- **1)** Use a ***C* = 10nF** and connect the probe to the **50Ω** of the waveform function generator (instead of the TTL output) and configure an input **sinusoid** of amplitude V_i **= 5V, zero offset**, and frequency ***f*=1 kHz**. **2)** Draw the signals in the grip provided and annotate the parameters: V_i, V_o, t_0, t_1 i t_2. **3)** Use (24) and (25) to evaluate module and phase; and compare with (18).
- Repeat the previous steps for ***f* = 200Hz**.

4. 2nd. Order systems.

4.1 *LTI* system response to a step function

The standard notation of the 2nd. order *LTI* system is written as

$$H(s) = \frac{v_o(s)}{v_i(s)} = K \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}; \text{ o bé } \quad H(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} = K \frac{1}{1 - (\omega/\omega_n)^2 + j2\xi\omega/\omega_n} \quad . \quad (26)$$

The output of such a system to a step function $v_i(s)=V_i/s$ is,

$$v_o(t) = K \times V_i \left[1 + \frac{1}{2\sqrt{\varsigma^2 - 1}} \left(\frac{e^{-p_1 t}}{p_1} - \frac{e^{-p_2 t}}{p_2} \right) \right] \quad (27)$$

where,

$$p_{1,2} = \xi\omega_n \pm \omega_n \sqrt{\xi^2 - 1} \quad (28)$$

are the roots of the 2nd. order polynomial in the denominator of $H(s)$, known as the system poles.

Generally speaking, the behavior of $H(s)$ is best characterized by two parameters: the *damping factor* ξ and the *natural frequency* ω_n, respectively. Depending on the damping factor, there are three cases:

- *Underdamped behavior*: $0 < \xi < 1$

When $0 < \xi < 1$, p_1 and p_2 are **complex conjugate**. In this case, (27) can be rewritten as,

$$v_o(t) = K \times V_i \left\{ 1 - \frac{e^{-\xi\omega_n t}}{\sqrt{1-\xi^2}} \sin\left[\omega_d t + \tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\xi} \right) \right] \right\}. \tag{29}$$

and we obtain and underdamped behavior, which means that the output is characterized by an initial oscillating transient before it reaches its forced response (Fig. 9a). The parameter $\omega_d = \omega_n(1-\xi^2)^{1/2}$ is called the *natural-damped frequency* and is the frequency during the initial transient. The relevant points of this signal can be evaluated using the expressions in Table 1.

- *Critical damping*: $\xi = 1$

Here, the poles are **real** and **equal** ($p_1 = p_2 = \omega_n$), and the output has **the fastest possible response without overshot**,

$$v_o(t) = K \times V_i \left[1 - e^{-\omega_n t}(1 + \omega_n t) \right] \tag{30}$$

- *Over-damped*: $\xi > 1$

When $\xi > 1$, the poles are **real** but **different**. The output (27), which responds to an exponential law, increases slowly until it settles to its steady state. However, in this case we may distinguish two situations: one in which both poles are close each other and another where $p2$ **gets over** p_1 ($\xi >> 1 \rightarrow p_1 >> p_2$). In the last case, $H(s)$ can be approximated to a 1st. order system of the form,

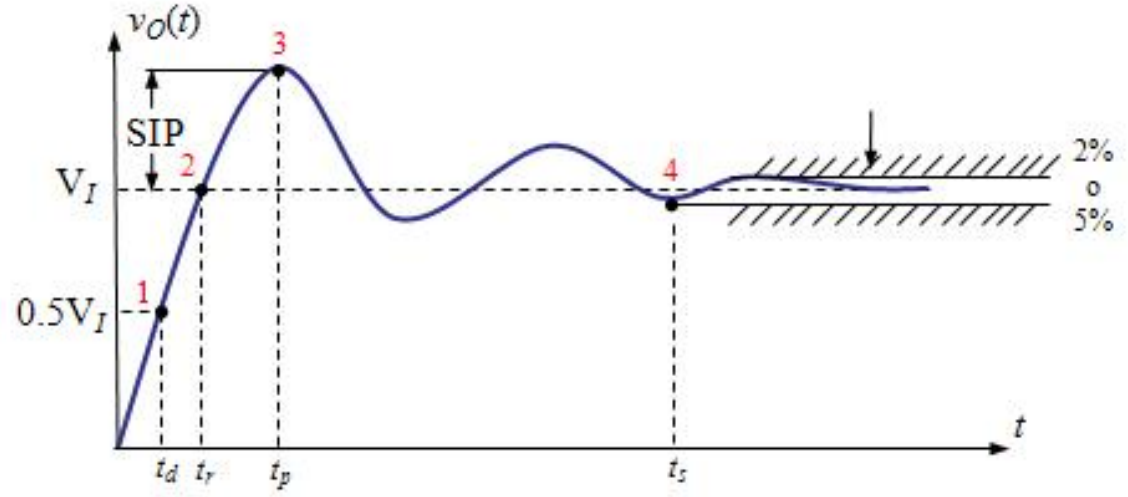
$$\hat{H}(s) \approx \lim_{p_1 \to \infty} \frac{v_o(s)}{v_i(s)} = K \frac{p_2}{s + p_2} \tag{31}$$

where,

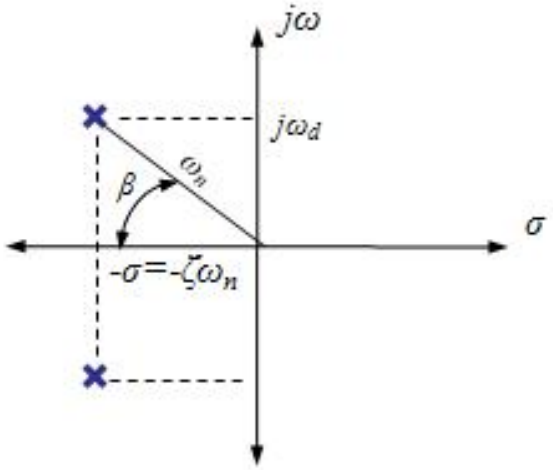
$$\hat{\tau} = \frac{1}{p_2} = \frac{1}{\xi\omega_n - \omega_n\sqrt{\xi^2 - 1}} \tag{32}$$

would correspond to the new time constant resulting from this estimation.

In general, the order of $H(s)$ depends on the degree in the denominator. Since the *laplacian* operator $s = d(\cdot)/dt$ also represents the derivative in the differential equation, the order is also established by the number of capacitors and inductors, provided that elements of the same type do not form series or parallel associations.



(a)



(b)

***Figure* 9**. Underdamped behavior in a 2nd. Order LTI system (K=1). a) Output waveform; b) Defining σ.

Parameter	Expression	Observations
1. Delay time (**t_d**)	------	It can only by evaluated by using (27) and imposing **$v_o(t) = 0.5V_i$**
2. Rise time (**t_r**)	$t_r = \frac{1}{\omega_d}\tan^{-1}\left(\frac{\omega_d}{-\sigma}\right) = \frac{\pi-\beta}{\omega_d}$	See Fig. 9b
3. Overshot time (**t_p**)	**$t_p = \pi/\omega_d$**	
3. Overshoot (***SIP***)	$SIP = \frac{v_o(t_p)-v_o(\infty)}{v_o(\infty)} = e^{-\frac{\xi}{\sqrt{1-\xi^2}}\pi}$	$v_o(t_p)$, $v_o(\infty)$ output value at t=t_p and steady state, respectively
4. Settling time (**t_s**) (* approximated value)	**$t_s = 3/(\xi\omega_n)$**	Error 5% of Vi
	$t_s = 4/(\xi\omega_n)$	Error 3% of Vi

***Table* 1**. Important parameters of the underdamped response to a step function.

4.2 Response of the series RLC circuit to a step input

One very popular and didactical example of a 2nd order LTI system is the series *RLC* circuit (Fig. 10) which consists of a resistor, a capacitor and an inductor. Using a voltage divider, the capacitor voltage (in *s* domain) is expressed as,

$$v_c(s) = \frac{X_c(s)}{R + X_L(s) + X_c(s)} v_i(s) \tag{33}$$

where, $X_c(s) = 1/(Cs)$ and $X_L(s) = Ls$ are the impedances of the capacitor and the inductor, respectively. After rearranging (33), the standard expression becomes,

$$H(s) = \frac{v_c(s)}{v_i(s)} = \frac{1/Cs}{R + Ls + 1/Cs} = \frac{1/LC}{s^2 + (R/L)s + 1/LC} \tag{34}$$

and, therefore, the gain factor, the natural frequency and the damping factor are,

$$K = 1; \qquad \omega_n = \frac{1}{\sqrt{LC}} \qquad \text{and} \qquad \xi = \frac{R}{2}\sqrt{\frac{C}{L}} \ . \tag{35}$$

Task PRELAB3: On the Bread-board template, represent the necessary component and instrument connections from Fig.11 you'll need to develop in order to measure the response to an input step of the series RLC circuit.

Task LAB3: Obtain the true response of the series *RLC* circuit and compare measurements with the theoretical values.

- **1)** Evaluate the theoretical value of $\boldsymbol{\xi}$ and ω_n by means of (35) and then evaluate the overshot (SIP) and the peak time (t_p) using the information in Table 1. **2)** Mount the *RLC* circuit. **3)** Connect the TTL output of the waveform generator and set a frequency ***f* = 100Hz**. Use the "T" connector. **4)** Configure the oscilloscope in order to observe the initial transient of CH2, in one of the ascending steps of CH1, in much detail. Draw the waveforms on the grid. **5)** Annotate the peak and rise time, $\boldsymbol{t_p}$ and $\boldsymbol{t_r}$; the damping factor ξ and the overshot ***SIP***, and compare with the theoretical ones.

- **1)** For ***R*=100k**, evaluate the new values of ξ and ω_n by means of (35) and estimate the theoretical time constant $\boldsymbol{\tau}$ using (32). **2)** Change the resistor in the circuit and draw the new signals. **3)** Measure the settling time ($\boldsymbol{t_s \rightarrow 5\tau}$ in half a cycle) and establish the experimental $\boldsymbol{\tau}$ of the circuit. Compare the values.

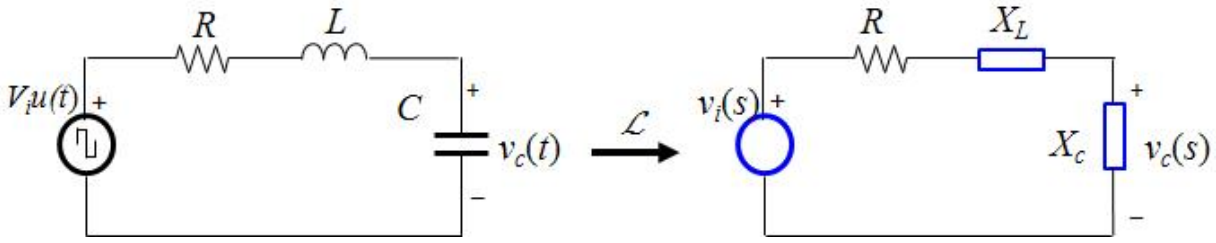


***Figure* 10**. Schematics of the series RLC circuit and its equivalence in *s* domain.

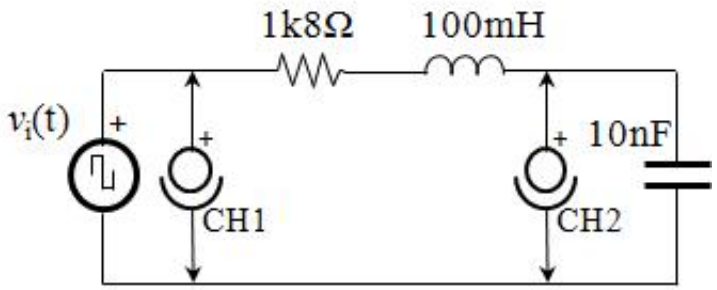


***Figure* 11**. Circuit and instrument connections for Task LAB3.

REMARK: The oscilloscope has a resistor $\boldsymbol{R_{CH2}}$ = **1MΩ** and a capacitor $\boldsymbol{C_{CH2}}$ = **13pF** in CH2 which connect in parallel with the circuit output (Fig. 12) when probes are plugged in. This connection has consequences in the true value of the parameters in (35). In fact, one can prove that the new transfer function considering these internal components becomes

$$H(s)=\frac{v_c(s)}{v_i(s)}=\frac{1}{K}\frac{K/LC_{EQ}}{s^2+\left(\frac{L+RR_{CH2}C_{EQ}}{LR_{CH2}C_{EQ}}\right)s+K/LC_{EQ}} \tag{36}$$

where

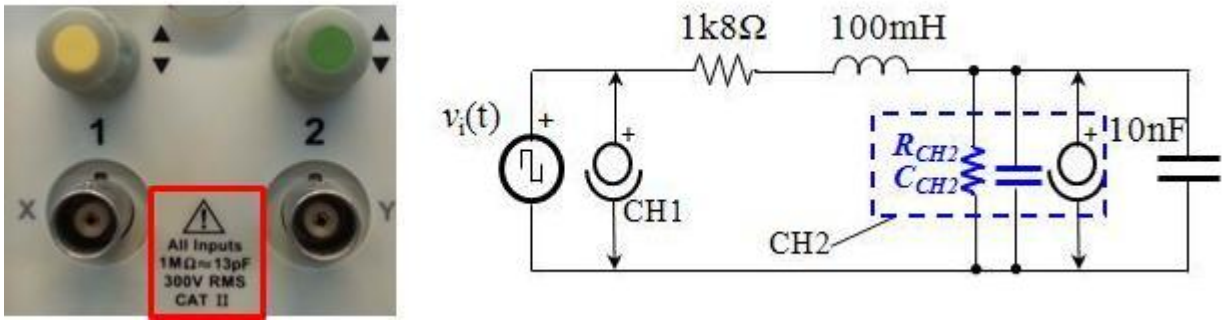
$$K=\left(1+\frac{R}{R_{CH2}}\right);\omega_n=\frac{K}{\sqrt{LC_{EQ}}};\xi=\frac{L+RR_{CH2}C_{EQ}}{2KR_{CH2}\sqrt{LC_{EQ}}}\ \text{ per } C_{EQ}=C+C_{CH2}. \tag{37}$$

For the same reason, when $\boldsymbol{R}$ = **100k** the settling value $\boldsymbol{v_c(\infty)}$ decreases to $\boldsymbol{V_i/K}$ = **4.5V**. This analysis could be even more complex if the internal components of CH1 are also considered.

4.3 The *electric resonance* phenomenon (the series *RLC* circuit case)

When *RLC* circuits are powered by sinusoids of the form $\boldsymbol{v_i(t) = V_i\sin(\omega t)}$ (Fig. 6) there is an interesting phenomenon called *electric resonance* which occurs at a certain frequency.

In the series *RLC* circuit, for example, let us define Z_T as the global impedance of the passive network. When $X_L(j\omega) = -X_c(j\omega) = +j/C\omega$, the resistor voltage is maximum. That is, when the



(a) (b)

***Figure* 12**. Effect of connecting CH2 at the output of the RLC circuit. a) Detail of CH1 and CH2 showing the input resistance R_{CH2} and the capacitor C_{CH2} which is added to the circuit when the probe is connected. b) Resulting schematics considering these two components.

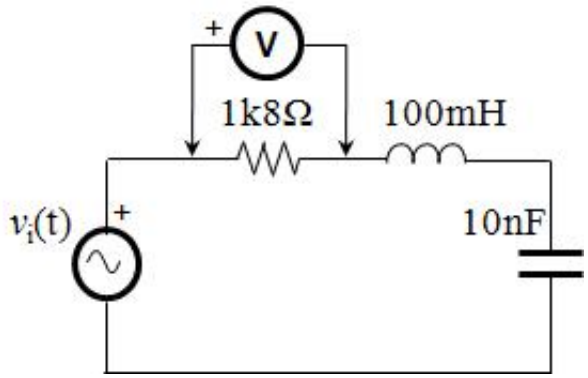


***Figure* 13**.Multi-meter connection for measuring the electric resonance.

$$Z_T(j\omega) = R + X_L(j\omega) + X_c(j\omega), \tag{38}$$

$$jL\omega_r = \frac{j}{\omega_r C} \longrightarrow \omega_r = \frac{1}{\sqrt{LC}}, \tag{39}$$

network produces its **minimum impedance $Z_T(j\omega_r) = R$**, so that the **maximum resistor current** becomes $v_R(j\omega_r) = V_i/R$. To this frequency $\omega = \omega_r$ we refer to as the *resonant frequency*.

Task LAB4: Using the multi-meter, determine the experimental resonant frequency ω_r of the RLC circuit (Fig. 13).

- **1)** Configure the waveform generator to the same **sinus** signal in task LAB2 (**5V-peak, zero offset**) but use a frequency ***f* = 100Hz** instead**. 2)** Connect the voltmeter with the resistor *R* in parallel. Use the AC measurement option (**ACV**). **3)** In the waveform generator, increase the frequency ***f*** until the resistor voltage v_R reaches its maximum value. **4)** Annotate the frequency ***fr*** the peak V_R and the rms value V_{Rrms}.

Annex 1 – Results form PRELAB

REMARK: You **MUST** do these activities **BEFORE THE LAB SESSION CORRESPONDING TO PRT2**

UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH Escola Politècnica Superior d'Enginyeria de Vilanova i la Geltrú	EEL
Electronic Systems (SIEK) **Activity 2:** Time and Frequency domain **PRELAB**	
Students:	**Date:**

PRELAB 0: Draw the contour package of a **10nF** and a **10µF** capacitor

How is the polarity indicated?

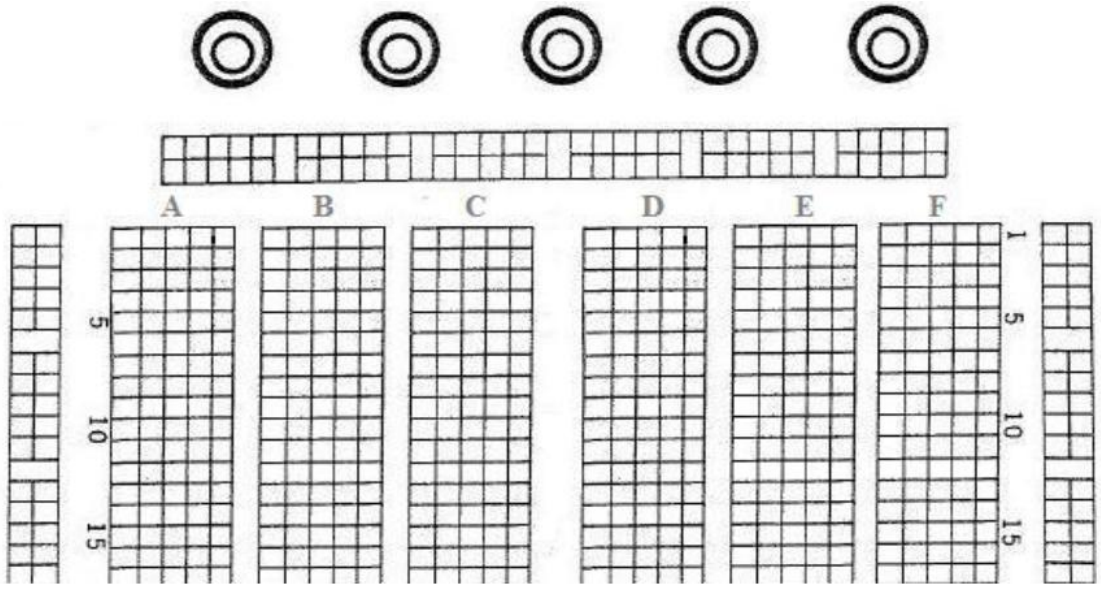
10nF:

10µF:

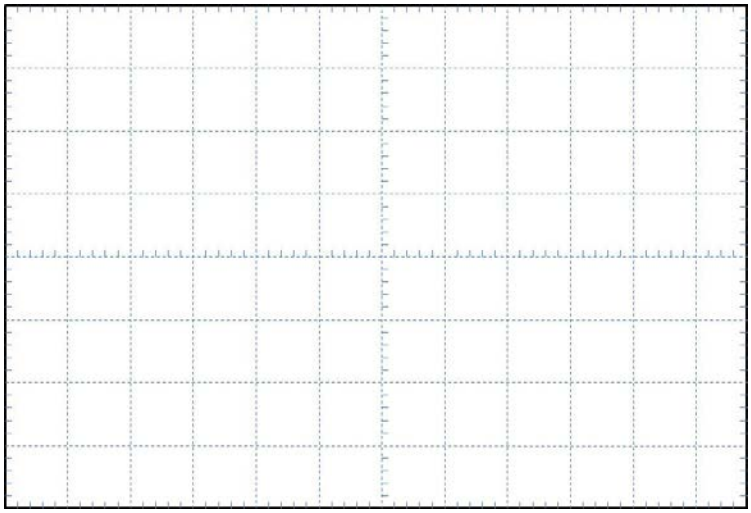
<u>PRELAB1</u>. Series *RC* circuit – Response to a step function. Waveform function generator configuration, mounting diagram, and waveform traces to be observed on the screen

Check the options you believe you need for the specified configuration

- ***OUTPUT:*** ☐ *TTL* ☐ 50Ω.
- ***FUNTION:*** ☐ Default ☐ *SQUARE* ☐ *SINUS* ☐ *TRIANGULAR*
- ***OFFSET:*** ☐ Default ☐ Value: _____
- ***AMPLITUDE:*** ☐ Defecte ☐ Vaue: _____
- ***FREQUENCY:*** _____



Representation of $v_i(t)$ and $v_c(t)$



CH1 VOLT/:
1V/
Zero POS: -2V

CH2 VOLT/:
1V/
Zero POS: -2V

TIME/: **500mseg/**

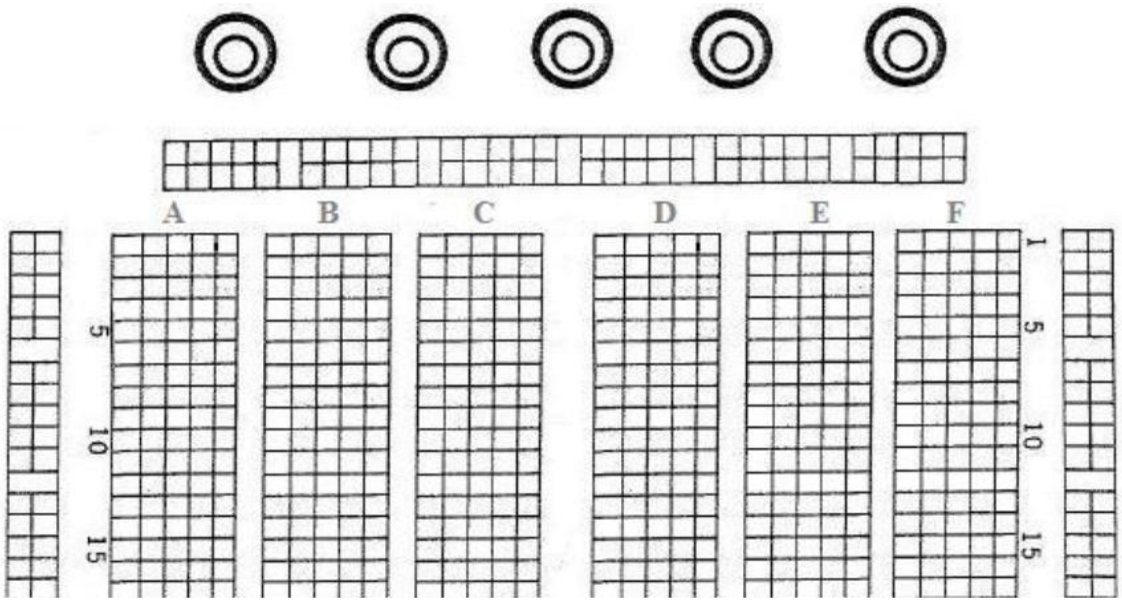
Coupling: DC

PRELAB 2. Series RC circuit – Frequency response.

Representation of $v_i(t)$ i $v_c(t)$

	CH1 VOLT/: **Zero POS:** **CH2** VOLT/: **Zero POS:** **TIME**/: **TRIGGER Possition:** **Coupling:**

PRELAB 3. Series *RLC* circuit – Response to a step function.



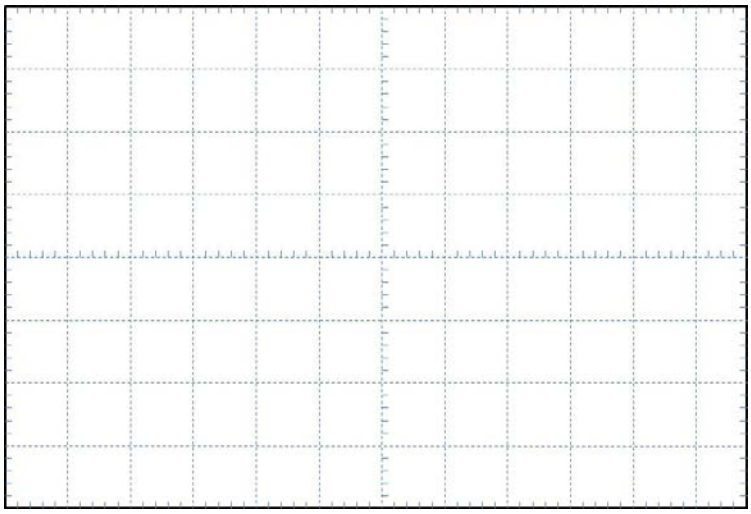
Annex 2 –Lab activities

REMARK: You **MUST PRINT OUT** this form and **TAKE IT WITH YOU** the day of the lab session

UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH Escola Politècnica Superior d'Enginyeria de Vilanova i la Geltrú	EEL
Electronic Systems (SIEK) **Activity 2:** Time and Frequency domain **RESULTS FORM**	
Students:	**Date:**

LAB 1: Series *RC* circuit – Response to a step function

Waveforms corresponding to $v_i(t)$ and $v_c(t)$ (**10µF**)



CH1 VOLT/:
1V/
Zero POS: -2V

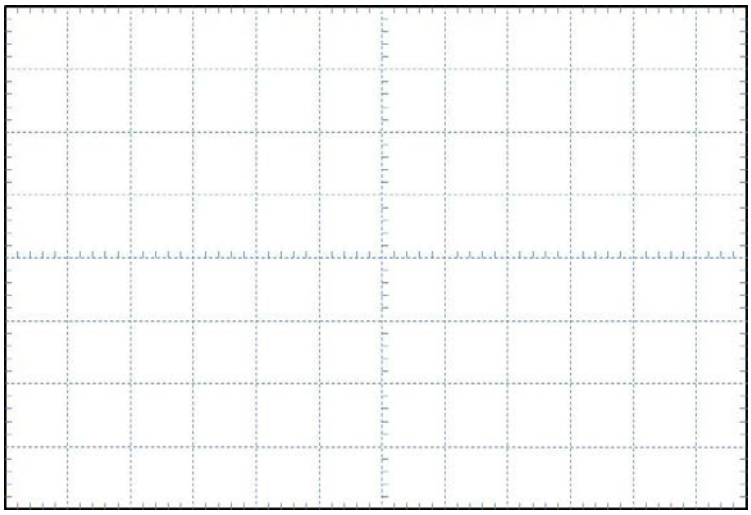
CH2 VOLT/:
1V/
Zero POS: -2V

TIME/: **500mseg/**

Coupling: DC

t_s (=5τ): _____ τ: _____

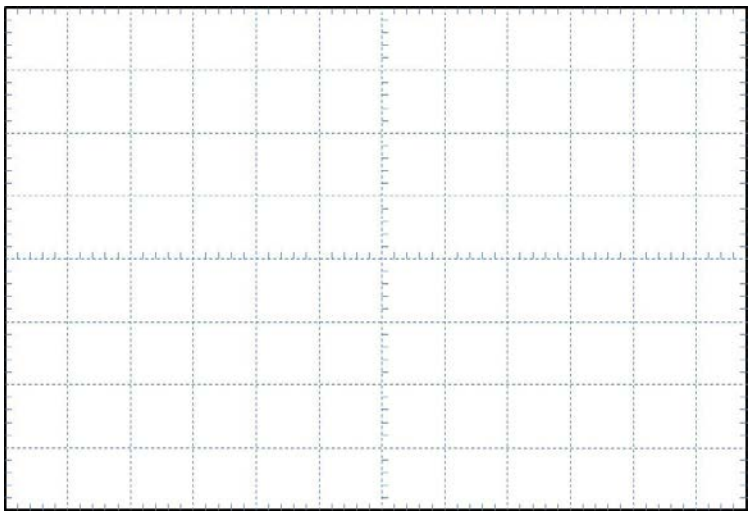
Waveforms corresponding to $v_i(t)$ and $v_c(t)$ (**10nF**)

	**CH1** VOLT/: **Zero POS:** **CH2** VOLT/: **Zero POS:** **TIME**/: **Coupling:**

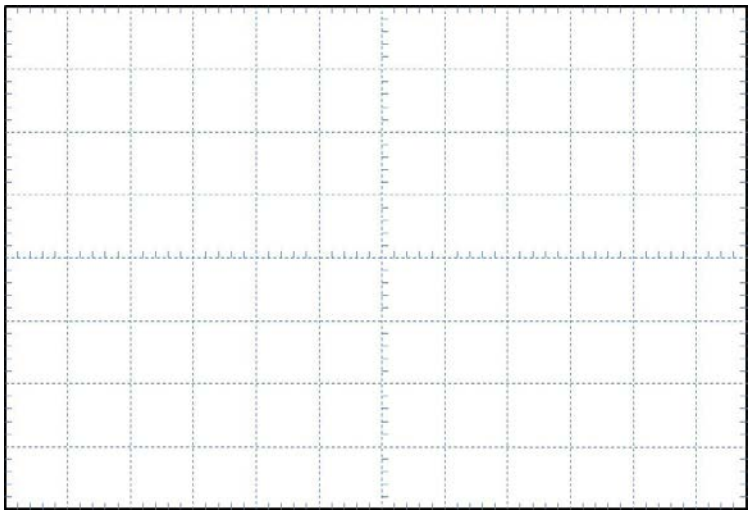
t_s (=5τ): _____ τ: _____

<u>LAB 2</u>: Series RC circuit – Frequency response.

Waveforms corresponding to $v_i(t)$ and $v_c(t)$ (***f*** **= 1KHz**)

	**CH1** VOLT/: **Zero POS:** **CH2** VOLT/: **Zero POS:** **TIME**/: **Coupling:**

Waveforms corresponding to $v_i(t)$ and $v_c(t)$ **(f = 100Hz)**

	**CH1** VOLT/: **Zero POS:** **CH2** VOLT/: **Zero POS:** **TIME**/: **Coupling:**

Module and *phase* of H(s) for ***f* = 1KHz** and ***f* = 100Hz** by using (18):

$|H(j2\pi 1\text{KHz})|$: _____ $\angle H(j2\pi 1\text{KHz})$: _____

$|H(j2\pi 100\text{Hz})|$: _____ $\angle H(j2\pi 100\text{Hz})$: _____

f	t_0	t_1	t_2	V_i	V_c
100Hz					
1kHz					

***Table* 3.** Signal parameters necessary to devaluate *modeule* and *phase* for f = 100Hz i f = 1KHz

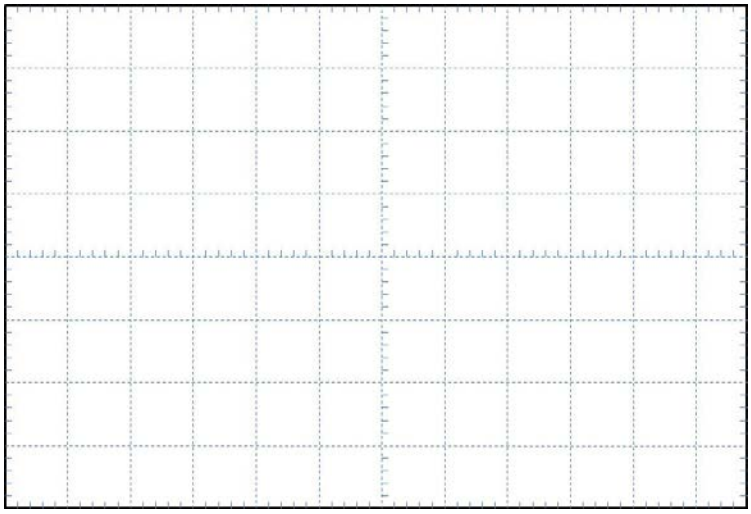
Experimental values obtained for ***f* = 1KHz** i ***f* = 100Hz**

$|H(j2\pi 1\text{KHz})|$: _____ $\angle H(j2\pi 1\text{KHz})$: _____

$|H(j2\pi 100\text{Hz})|$: _____ $\angle H(j2\pi 100\text{Hz})$: _____

<u>LAB 3</u>: Series *RLC* circuit – Response to a step function

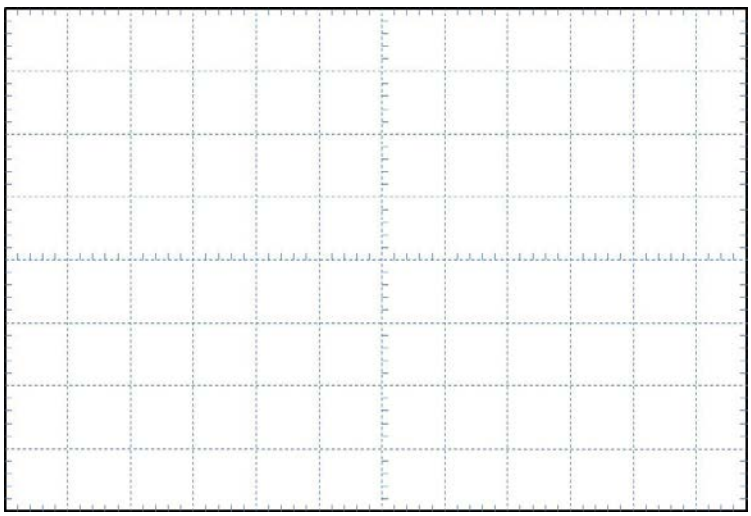
Waveforms corresponding to $v_i(t)$ and $v_c(t)$ (***R* = 1k8Ω**)

	**CH1** VOLT/: **Zero POS:** **CH2** VOLT/: **Zero POS:** **TIME**/: **Coupling:**

	t_p	t_r	*SIP*	ξ	ω_n
Theoret.					
Measured					

***Taula* 3.** Resultats de la resposta esgraó en el circuit *RLC* sèrie

Waveforms corresponding to $v_i(t)$ and $v_c(t)$ (***R* = 100kΩ**)

	**CH1** VOLT/: **Zero POS:** **CH2** VOLT/: **Zero POS:** **TIME**/: **Coupling:**

t_s (=5τ ***teòric***): _____ t_s (=5τ ***mesurat***): _____ $\hat{\tau}$: _____

<u>LAB 4</u>: Resonant frequency of the series *RLC* circuit.

	f_r (Hz)	ω_r ($2\pi f_r$) (rad/seg)	$V_R(j\omega_r)$ (peak)	$V_{Rrms}(j\omega_r)$ (rms)
Theoret.				
Mesaured				

***Table* 4.** Resonant frequency measurements

Annex 3 –Basic Laplace Transformations

***f*(*t*)**	***F*(*s*)**
Unit impulse	1
Step function $u(t)$	$1/s$
t	$1/s^2$
$\frac{t^{n-1}}{(n-1)!}$ $n = 1, 2, 3, ...$	$1/s^n$
t^{n-1} $n = 1, 2, 3, ...$	$n!/s^{n+1}$
e^{-at}	$\frac{1}{s+a}$
te^{-at}	$\frac{1}{(s+a)^2}$
$\frac{1}{(n-1)!}t^{n-1}e^{-at}$ $n = 1, 2, 3, ...$	$\frac{1}{(s+a)^n}$
$t^n e^{-at}$ $n = 1, 2, 3, ...$	$\frac{n!}{(s+a)^{n+1}}$
$\sin(\omega t)$	$\frac{\omega}{s^2+\omega^2}$
$\cos(\omega t)$	$\frac{s}{s^2+\omega^2}$
$\sinh(\omega t)$	$\frac{\omega}{s^2-\omega^2}$
$\cosh(\omega t)$	$\frac{s}{s^2-\omega^2}$
$\frac{1}{a}\left(1-e^{-at}\right)$	$\frac{1}{s(s+a)}$
$\frac{1}{b-a}\left(e^{-at}-e^{-bt}\right)$	$\frac{1}{(s+a)(s+b)}$
$\frac{1}{b-a}\left(be^{-bt}-ae^{-at}\right)$	$\frac{s}{(s+a)(s+b)}$
$\frac{1}{ab}\left[1+\frac{1}{a-b}\left(be^{-at}-ae^{-bt}\right)\right]$	$\frac{1}{s(s+a)(s+b)}$

$f(t)$	$F(s)$
$\frac{1}{a^2}\left(1-e^{-at}-ate^{-at}\right)$	$\frac{1}{s(s+a)^2}$
$\frac{1}{a^2}\left(at-1+e^{-at}\right)$	$\frac{1}{s^2(s+a)}$
$e^{-at}\sin(\omega t)$	$\frac{\omega}{(s+a)^2+\omega^2}$
$e^{-at}\cos(\omega t)$	$\frac{s+a}{(s+a)^2+\omega^2}$
$\frac{\omega_n}{\sqrt{1-\xi^2}}e^{-\xi\omega_n t}\sin\left(\omega_n\sqrt{1-\xi^2}t\right)$	$\frac{\omega_n^2}{s^2+2\xi\omega_n s+\omega_n^2}$
$-\frac{\omega_n}{\sqrt{1-\xi^2}}e^{-\xi\omega_n t}\sin\left(\omega_n\sqrt{1-\xi^2}t-\phi\right)$ $\phi=\tan^{-1}\left(\frac{\sqrt{1-\xi^2}}{\xi}\right)$	$\frac{s}{s^2+2\xi\omega_n s+\omega_n^2}$
$1-\frac{\omega_n}{\sqrt{1-\xi^2}}e^{-\xi\omega_n t}\sin\left(\omega_n\sqrt{1-\xi^2}t+\phi\right)$	$\frac{\omega_n^2}{s\left(s^2+2\xi\omega_n s+\omega_n^2\right)}$
$1\text{-}\cos(\omega t)$	$\frac{\omega^2}{s\left(s^2+\omega^2\right)}$
$\omega t\text{-}\sin(\omega t)$	$\frac{\omega^3}{s^2\left(s^2+\omega^2\right)}$
$\sin(\omega t)\text{-}\ \omega t\text{-}\cos(\omega t)$	$\frac{2\omega^3}{\left(s^2+\omega^2\right)^2}$
$\frac{1}{2\omega}t\sin(\omega t)$	$\frac{s}{\left(s^2+\omega^2\right)^2}$
$t\cos(\omega t)$	$\frac{s^2-\omega^2}{\left(s^2+\omega^2\right)^2}$
$\frac{1}{\omega_2^2-\omega_1^2}\left[\cos(\omega_1 t)-\cos(\omega_2 t)\right]\ (\omega_1\neq\omega_2)$	$\frac{s}{\left(s^2+\omega_1^2\right)\left(s^2+\omega_2^2\right)}$
$\frac{1}{2\omega}\left[\sin(\omega t)+\omega\cos(\omega t)\right]$	$\frac{s^2}{\left(s^2+\omega^2\right)^2}$

Properties of the Laplace Transformation

1	$\mathcal{L}[A\cdot F(t)] = A\cdot F(s)$
2	$\mathcal{L}[f_1(t)\pm f_2(t)] = F_1(s)\pm F_2(s)$
3	$\mathsf{L}_{\pm}\left[\frac{d^n}{dt^n} f(t)\right] = s^n F(s) - \sum_{k=1}^{n} s^{n-k} f^{k-1}(0\pm)$ on $f^{k-1}(t) = \frac{d^{k-1}}{dt^{k-1}} f(t)$
4	$\mathsf{L}_{\pm}\left[\int\ldots\int f(t)(dt)^n\right] = \frac{F(s)}{s^n} + \sum_{k=1}^{n} \frac{1}{s^{n-k+1}}\left[\int\ldots\int f(t)(dt)^k\right]_{t=0\pm}$
5	$\mathsf{L}\left[\int_0^t f(t)\,dt\right] = \frac{F(s)}{s}$
6	$\mathsf{L}\left[\int_0^{\infty} f(t)\,dt\right] = \lim_{s\to 0} F(s)$; si $\int_0^{\infty} f(t)\,dt$ existeix
7	$\mathsf{L}\left[e^{-at} f(t)\right] = F(s+a)$
8	$\mathsf{L}\left[f(t-a)1(t-a)\right] = e^{-as}F(s)$ per $a \geq 0$
9	$\mathsf{L}\left[t^n f(t)\right] = (-1)^n \frac{d^n}{ds^n} F(s)$ n = 1, 2, 3, ...
10	$\mathsf{L}\left[\frac{1}{t} f(t)\right] = \int_s^{\infty} F(s)$; si $\lim_{s\to 0} \frac{1}{t} f(t)$ existeix
11	$\mathsf{L}\left[f\left(\frac{t}{a}\right)\right] = aF(as)$
12	$\mathsf{L}\left[\int_0^t f_1(t-\tau)\, f_2(\tau)\,dt\right] = F_1(s)F_2(s)$
13	$\mathsf{L}\left[f(t)g(t)\right] = \frac{1}{2\pi j}\int_{c-j\infty}^{c+j\infty} F(p)G(s-p)\,dp$

Lab Activity 3. Linear DC Power Supplies

Main goal: Knowing the basic stages that make up a low-power DC supply (line transformation, voltage rectification, filtering and stabilization) and learn the function that basic semiconductors (diodes, bridge rectifiers, Zener and integrated circuits) develop within this electronic system.

1 Introduction

A DC power source provides a continuous DC voltage to a circuit. To make this possible, it is necessary to transform the high-power line voltage, which is in the form of a sinusoid of $220V \cdot \sqrt{2} = 311\text{V}$ peak and 50Hz, by means of several operations implemented in stages (Fig. 1):

- The *transformer* generates another voltage (v_S) of the same type as in the power line (v_{AC}) at the second winding, but of a much lower amplitude. This value depends on the number of turns of both windings (N_1 - primary and N_2 – secondary, where $N_1 >> N_2$) and is calculated as:

$$v_S = \frac{N_2}{N_1} v_{AC} \tag{1}$$

- The *rectifier* is implemented by means of diodes and converts the output from the transformer into a unipolar voltage of considerable ripple.
- The ripple at the rectifier output is reduced even more with a *filtering* stage, which is responsible of removing the components of higher frequency. The ripple obtained with this operation, however, depends on other factors belonging to the output load (such as impedance and load current), and cannot be removed completely.
- This is precisely the function of the last stage, the *voltage regulator*, which makes the DC output independent from the input line.

2 Rectifier circuits (rectifier diodes)

We'll start with the rectifier diode, the most common *nonlinear* semiconductor in electronics (Fig. 2a) which acts as a semi-controlled switch (Fig. 2c and 2d):

- When a negative voltage is applied to both terminals (according to the reference in Fig. 1b, $v < 0$), this device behaves as an *open circuit* (Fig. 2c). In this situation, its electric current, from anode to cathode,is zero and it is said that the diode is **reverse biased**, or it works in **OFF** mode.
- On the other hand, if the electric current is positive ($i > 0$) the device act as *shortcircuit* (Fig. 2d) and it is said that the diode is **forward biased**. It works in **ON** mode.

The true behavior, however, varies slightly. In ON mode, it turns out that the voltage from anode to cathode (v) is not quite zero, but has a small value close to 0.7V (the true value depends on diode the material used by the manufacturer). One way of representing this threshold consists in adding an additional source (V_D = 0.7V) in series with the ideal model (Fig. 3).

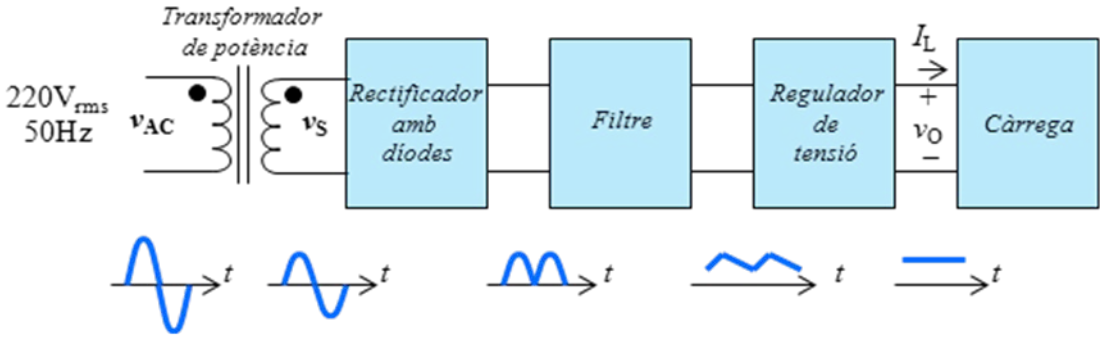


***Figure* 1**. Block diagram corresponding to the different stages of the DC power supply. These are the necessary steps for the AC-DC energy conversion of the power line v_{AC}.

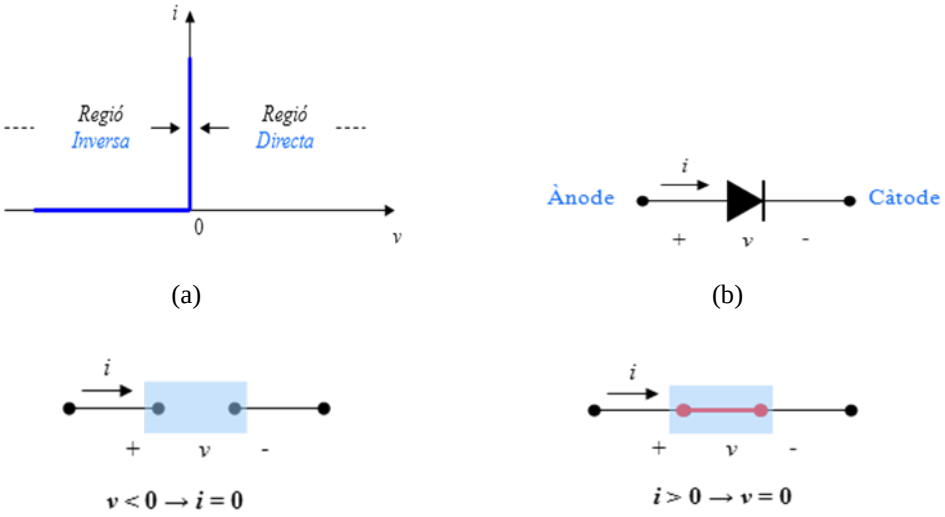


***Figure* 2**. The ideal diode model: a) Symbol; b) *i*-*v* characteristics; c) OFF operation; d) ON operation.

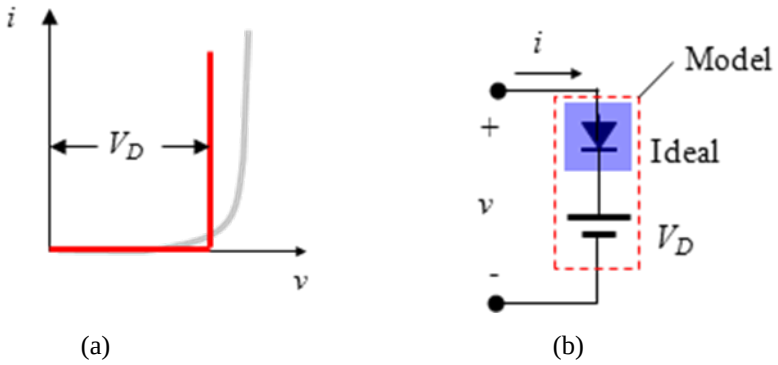
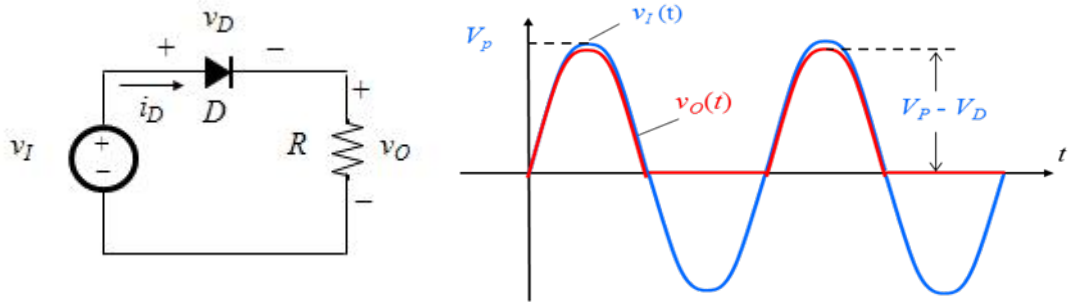


***Figure* 3**. a) True and linealized i-*v* characteristics; b) Equivalent linealized model.

One basic application which makes use of the diode characteristics is the *rectifier* (Fig. 4). This circuit consists of a diode *D* and a resistor *R* connected in series. When a sinusoid voltage $v_I = V_P \sin(2\pi ft)$ is introduced as input, the diode will be in ON mode whenever $v_I(t) \geq V_D$, and in OFF mode otherwise. Since in this mode i_D becomes zero, the output voltage in the resistor *R* is also zero.



(a) (b)

***Figure* 4**. a) Single-phase half-wave rectifier circuit. B) Voltage waveforms $v_I(t)$ – blue; and $v_O(t)$ - red.

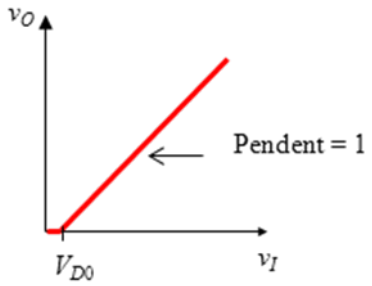


***Figure* 5**. $v_O - v_I$ transfer characteristics of the half-wave rectifier in Fig. 3a.

Thus, the circuit "rectifies" the negative cycle from the unique (or single-phased) input. During the positive cycle, the output will be the same as the input but removing the threshold V_D corresponding to the voltage drop on the diode (Fig. 5). Hence, the name of the circuit: the *single-phase half-wave rectifier*.

In practice, the average output voltage $V_{O(av)}$ is determined over an entire cycle as,

$$V_{O(av)} = \frac{1}{T}\int_0^T \left[v_I(t) - v_D(t)\right]dt \approx \frac{1}{2\pi}\int_0^{\pi} V_P \sin(\omega t)\, d\omega t - V_D \approx \frac{V_P}{\pi} - \frac{V_D}{2}, \quad (2)$$

where V_P corresponds to the input amplitude and depends on the transformer windings $\boldsymbol{v_I = v_S}$. As for the diode, the average and maximum value of electric current, $I_{D(av)}$ and $I_{D\max}$, respectively is obtained as

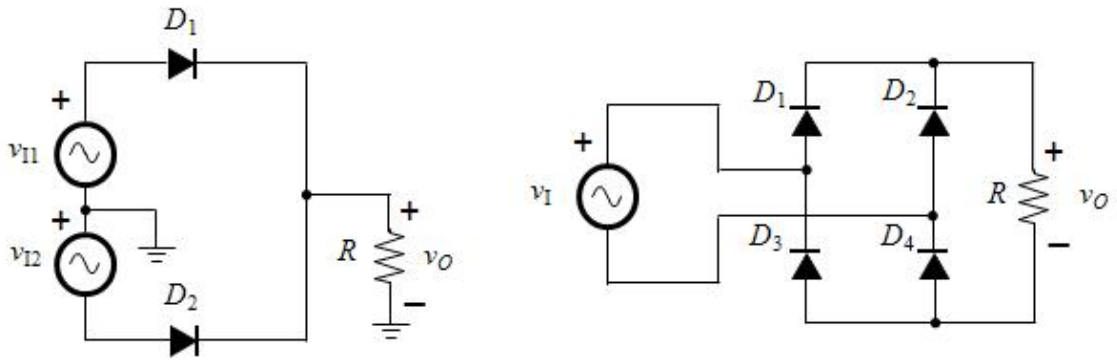
$$I_{D(av)} = \frac{V_{O(av)}}{R} \qquad \text{and} \qquad I_{D\max} = \frac{V_{O\max}}{R} = \frac{V_P - V_D}{R}, \quad (3)$$

whereas the maximum repetitive voltage drop in OFF mode , V_{RRM}[1] is,

$$V_{RRM} = \max\{-v_D(t)\} = V_P. \quad (4)$$

This information regarding the half-wave rectifier is important in practice, as it specifies which is the correct diode to use on one hand, and then it permits a first glance of the main DC power source parameters, such as the DC output or the power transferred by the source.

[1] V_{RRM} stands for *Maximum Repetitive Reverse Voltage* and is the maximum voltage the diode can take, from cathode to anode, when it is reverse biased. That is I_D = 0A.



(a) (b)

***Figure* 6**. (a) Two-phae haf-wave rectifier. (b) Single-phase full-wave rectifier (or bridge rtectifier).

Electrical variables	**Single-phase Rectifier** (half-wave)	**Two-phase Rectifier** (half-wave)	**Single-phase Rectifier** (full-wave)
$V_{O(av)}$	$\frac{V_P}{\pi} - \frac{V_D}{2}$	$\frac{2V_P}{\pi} - V_D$	$\frac{2V_P}{\pi} - 2V_D$
V_{RMM}	V_P	$2V_P$	V_P - V_D
I_{Dmax}	$\frac{V_P - V_D}{R}$	$\frac{V_P - V_D}{R}$	$\frac{V_P - 2V_D}{R}$
$I_{D(av)}$	$\frac{V_{O(av)}}{R}$		

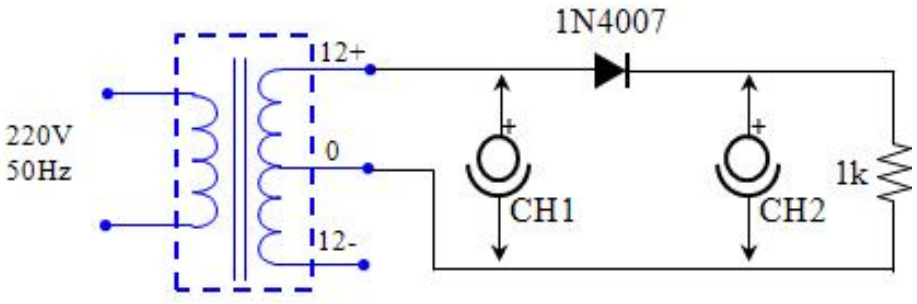
***Table* 1.** Summary of specifications corresponding to the different rectifier circuits.

The rectifier circuits in Fig. 6, improve the features of the half-wave rectifier. On one hand, the *two-phase half-wave rectifier* increases the capacity of output power transferred to the load because using two phases doubles the average DC value on the resistor v_O. On the contrary, however, the diodes must stand twice the input voltage when operating in OFF mode ($V_{RRM} \approx 2V_P$). The benefits of the *single-phase full-wave rectifier* (or *bridge rectifier*), on the other hand, are similar to the two-phase rectifier but with a reverse voltage $V_{RRM} \approx V_P$ (see Table 1).

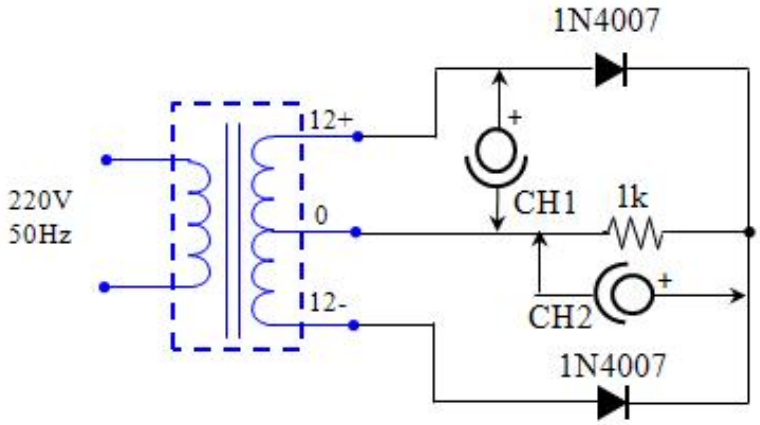
Task PRELAB1: In the Bread-Board template provided at the end of the document, draw the connections corresponding to the two rectifiers shown in Fig. 7, to be implemented in the lab on the 3rd. session. Include the connections from the transformer, components and oscilloscope.

Task LAB1: In each circuit in Fig. 7, obtain the waveform at the second winding in the transformer $v_I(t)$, the output $v_O(t)$ and the voltage in one diode $v_D(t)$.

- **1)** Mount the circuit in Fig. 7a. **2)** Turning both transformer and oscilloscope OFF, connect the probes and wires. When you finish, turn both devices ON. **3)** Configure CH1 and CH2 as indicated in order to observe both signals in detail. **4)** Select the **MATH** option and activate the SUBSTRACTION operation (purple trace: CH1 – CH2). **5)** Obtain the values of V_{RRM} and $V_{O(av)}$ by means of the MEASURE option of both channels.



(a)



(b)

***Figure* 7**. Diagram connections the two rectifiers necessary to obtain $v_I(t)$, $v_D(t)$ i $v_O(t)$ in the lab. a) Single-phase half-wave rectifier. b) Two-phase half-wave rectifier.

- Similarly, proceed with the second circuit (Fig. 7b) to obtain the waveform signals corresponding to the two-phase half-wave rectifier.

  REMARK: It is very important **NOT MANIPULATING OR NOT MODIFYING PROBE CONNECTIONS** while the transformer is on, in order to prevent the internal protection fuses of 0.5A from breaking. For the same reason, remember **NOT TO CONNECT** the negative terminal of the probes at different points in the circuit.

As the benefits of the *single-phase full-wave rectifier* are quite acceptable, its use is extended as part of many commercial DC low-power supplies[2]. Because of the four diodes, this circuit increases in complexity and volume. Fortunately, today there are many integrated circuits including the four diodes in a single package, such as the bridge rectifiers (Fig. 8), which eases connectivity and implementation.

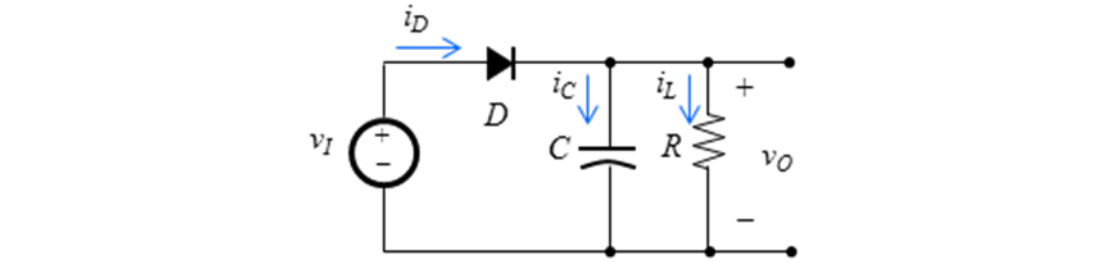
3 Filtering stage

The subsequent step to the rectification of the negative cycle in the input line consists in reducing the ripple. The easiest way consists in connecting a capacitor in parallel with the load (Fig. 9a) in order to cause a smooth transition between cycles (Fig. 9b), thus "filtering out" the high-frequency components of the input line. The full sequence of Fig. 9b develops as follows:

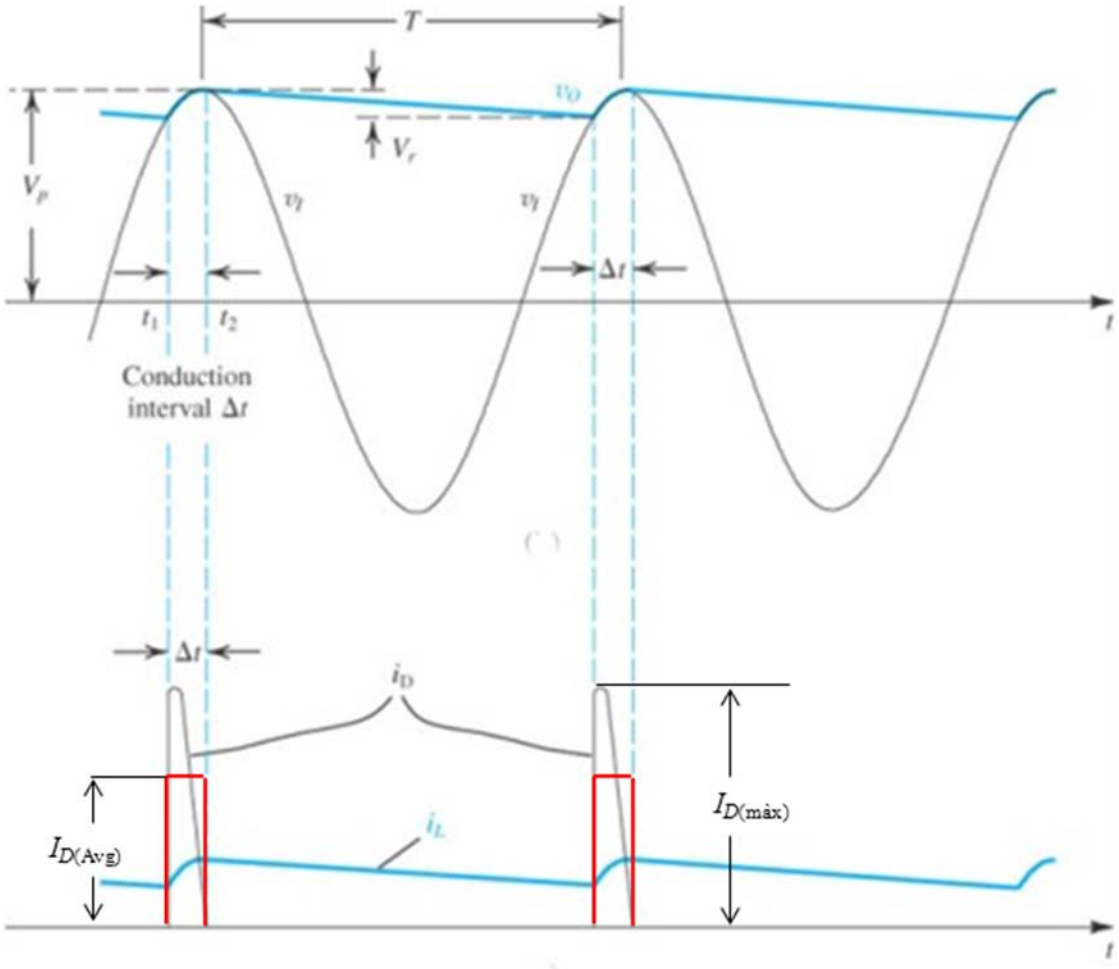
[2] In general, the low-power DC supplies are those providing a maximum output current $I_O = I_{D(av)} < \mathbf{2A}$.

(a) (b) (c)

***Figure* 8**. Three bridge rectifiers commonly used in DC power supplies: a) the **W10G-E4** from *Vishay*; b) the **KBPC5010** from *Fairchild Semiconductor;* c) the **DF06** from *International Rectifier*



(a)



(b)

***Figure.* 9**. Single-phase half-wave rectifier with filter. a) Schematics. b) Waveforms corresponding to voltages in v_O, v_I; and electric currents i_D, i_L. We assume $RC >> T$.

- The diode allows the electric current to flow for small period of time (say $\Delta t = t_2 - t_1$). The ON mode begins at $t = t_1$, at this moment the input reaches the output value, which was decaying as a result of the capacitor discharge during the previous interval.
- When v_I has just reached the maximum value (we use the approximation $V_P - V_D \approx V_P$ to simplify our comments), and assuming that the output transition is much slower in relation to that of the input because R and C are designed so that $\tau = RC >> T$, the diode stops conducting at t_2 and turns OFF.
- When the diode is OFF (in almost all the full cycle T), the capacitor C transfer its charge to the resistor R. The evolution of $v_O(t)$ is given by (5) where $t_2 = 0$ is assumed in order to simplify our comments:

$$v_O(t) = v_O(\infty) + \left[v_O(t_2) - v_O(\infty)\right] e^{-t/RC} = V_P e^{-t/RC} . \quad (5)$$

  Here, $v(\infty) = 0$ is the hypothetical voltage the capacitor would reach in an event of permanent discharge, $t = \infty$, and $v(t_2) \approx V_P$ correspond to the initial value of this interval. Assuming that $RC >> T$, a good approximation is:

$$e^{-t/RC} \approx 1 - \frac{t}{RC} \quad (6)$$

- Since $v_O(t_1) = V_P - V_r \approx V_P e^{-t/RC} \approx V_P\left(1 - t/RC\right)$, equating (6) and (5) allows the ripple to be estimated as:

$$V_r \approx V_P \frac{T}{RC} = \frac{V_P}{fRC} = \frac{I_L}{fC} \quad (7)$$

Knowing this parameter, the average value of the output voltage $V_{O(av)}$ is determined as

$$V_{O(av)} \approx V_P - \frac{V_r}{2} . \quad (8)$$

Finally, we obtain the average and maximum value of the electric current flowing through the diode, $I_{D(\text{av})}$ and $I_{D(\text{màx})}$ respectively. Once again, these parameters are crucial for selecting one diode from the different suppliers. Taking into account that the diode stops conducting when $v_I(t) \approx V_P$, the conduction interval Δt can be estimated by means of $V_P - V_r = V_P \cos(\omega \Delta t)$, where $\omega = 2\pi f. = 2\pi/T$ corresponds to the angular frequency of the input line. Assuming that $\omega\Delta t$ is too small, the term $\cos(\omega\Delta t)$ can be approximated as $\cos(\omega\Delta t) = 1 - \frac{1}{2}(\omega\Delta t)^2$. So, the conduction angle α becomes

$$\alpha = \omega\Delta t = \sqrt{2V_r/V_P} . \quad (9)$$

Then, for estimating the average current $i_{D(av)}$, we equate the capacitor charge supplied by the diode during the conduction interval Q_S and the charge lost during the OFF interval Q_P:

$$Q_S = i_{C(av)}\Delta t = \left(I_{D(av)} - I_L\right)\Delta t \qquad \text{and} \qquad Q_P = CV_r \tag{10}$$

Equating $I_{D(av)}$ from (10) and using (7) and (9) the average diode current is obtained as

$$I_{D(av)} = I_L\left(1+\pi\sqrt{2V_p/V_r}\right) \tag{11}$$

On the other hand, the expression for the maximum diode current I_{Dmax} is (the demonstration is far too long):

$$I_{D(av)} = I_L\left(1+2\pi\sqrt{2V_p/V_r}\right). \tag{11bis}$$

As such, in an event of a ripple $V_r << V_P$, it is approximately correct saying that $I_{D(màx)} \approx 2I_{D(av)}$.

Increasing C allows the ripple to be reduced (7), but has the disadvantage of increasing the average diode current significantly (11) and, therefore, it could be destroyed. This conditions are relaxed a little by using the two-phase rectifier as well as the bridge rectifier. In these cases the ripple and the electric currents become:

$$V_r \approx \frac{V_P}{2fRC} = \frac{I_L}{2fC} \tag{12}$$

$$I_{D(av)} = I_L\left(1+\pi\sqrt{V_p/2V_r}\right) \quad \text{and} \quad I_{D(av)} = I_L\left(1+2\pi\sqrt{V_p/2V_r}\right). \tag{13}$$

This makes the bridge rectifier the most adopted configuration in low-power DC supplies.

Task PRELAB2: In the Bread-Board template provided, draw the connections from the *bridge rectifier with filter* you need to mount the circuit the day of the lab session, including the DF06 integrated circuit (Fig. 10).

Task LAB2: Obtain the output waveform $v_O(t)$ for different values of the capacitor C.

- **1)** Mount the circuit using the integrated bridge rectifier DF06. First, use a capacitor ***C* = 100nF** and connect ONLY the probe of channel CH1 in parallel with the resistor. **2)** After observing the correct output waveform, obtain $\boldsymbol{V_{O(màx)}}$(=V_P) and $\boldsymbol{V_{O(min)}}$; and determine the ripple as $\boldsymbol{V_r = V_{O(max)} - V_{O(min)}}$). **3)** Then, use (8) in order to determine the average output value $\boldsymbol{V_{O(av)}}$.
- Repeat the preceding operations for different capacitors: ***C* = 10µF** and ***C* = 100µF**. Comment the differences between theoretical and experimental results, use (7) in case you need it.

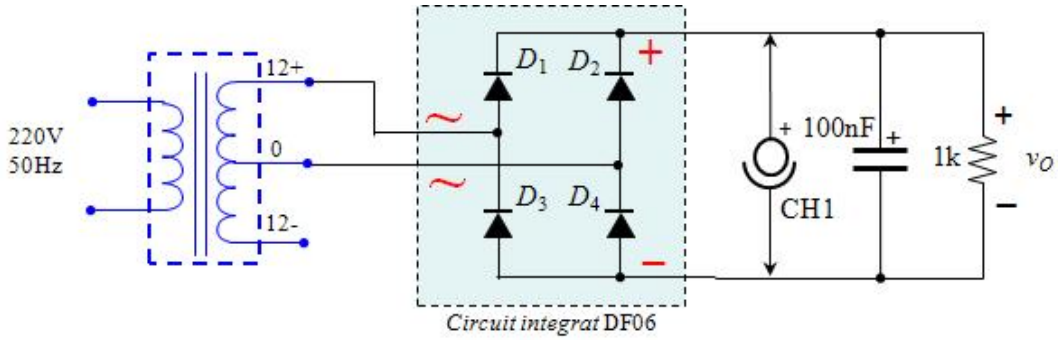


***Figure.* 10**.Schematics corresponding to the single-phase full-wave (or bridge) rectifier with filter, using the DF06 integrated circuit from *International Rectifier*.

4. Output voltage stabilization

We already mentioned (section 1) the functionality of the regulator in the last stage of the DC power supply, which is to provide a stable and independent voltage to the output. The simplest way of performing this operation consists in using a *Zener diode* (Fig. 11). The main difference in relation to the rectifier diode is that in the Zener the electric current can flow from cathode to anode. That is, $i = -i_Z < 0$ (or equivalently $i_Z > 0$). When this condition holds, it is normally said that the Zener is operating within the **breakdown region** (ON_{rev}), and the breakdown voltage is $v = -V_Z$ (the voltage from cathode to anode is V_Z).

In practice, however, the slope corresponding to the *i-v* characteristics at the breakdown region is finite (Fig. 12) and the breakdown voltage V_Z is not as constant as desired. Even so, in applications where a great stability is not required this tolerance is accepted and the zener is used for stabilization purposes. One example is the voltage regulator of Fig. 13. Its true output voltage considering the approximated model is:

$$v_O = V_{Z0} + r_Z I_Z \tag{12}$$

where r_Z represents the internal resistance of the zener.

In this circuit, the resistor value R cannot be any. As $v_R = v_S - R(I_L + I_Z)$, where I_L varies according to the output requirements ($0 > I_L > I_{L(màx)}$) and there are a minimum and maximum current where the Zener operates correctly (I_{Zmin}) and ($P_{Z(màx)} = V_Z \cdot I_{Z(màx)}$), meeting the following design condition is necessary:

$$\frac{v_{S(\min)} - v_{O(mín)}}{I_{L(màx)} + I_{Z(mín)}} \le R \le \frac{v_{S(màx)} - v_{O(màx)}}{I_{L(mín)} + I_{Z(màx)}} \tag{13}$$

Task PRELAB3: In the Bread-Board template provided, draw the connections for the full DC power supply, including the transformer, the bridge rectifier, the capacitor and the Zener-based voltage regulator (Fig. 14). Include the oscilloscope connections for measuring the ripple $\boldsymbol{V_r}$ (at $\boldsymbol{v_C}$ by means of CH1), the output $\boldsymbol{v_O}$ (with CH2) and the ammeter connection for measuring I_L.

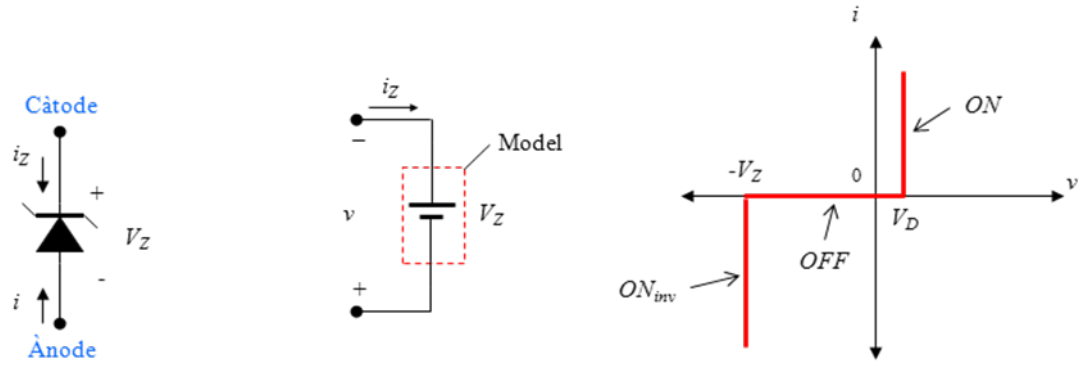


***Figure* 11.** Zener diode. Mathematical model and i-v characteristics. a) Symbol. b) Equivalent model for the breakdown region (ON_{rev}) c) *i-v* characteristics

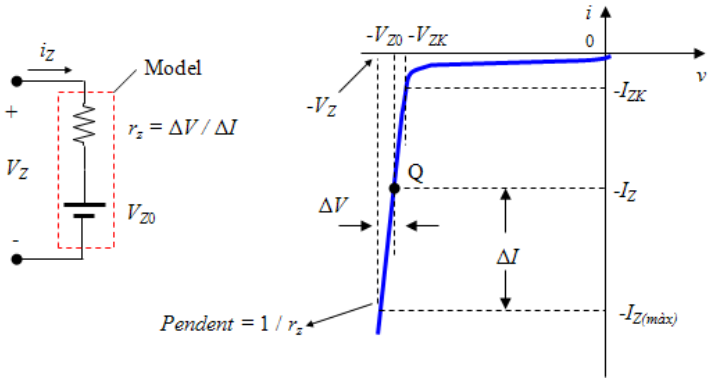
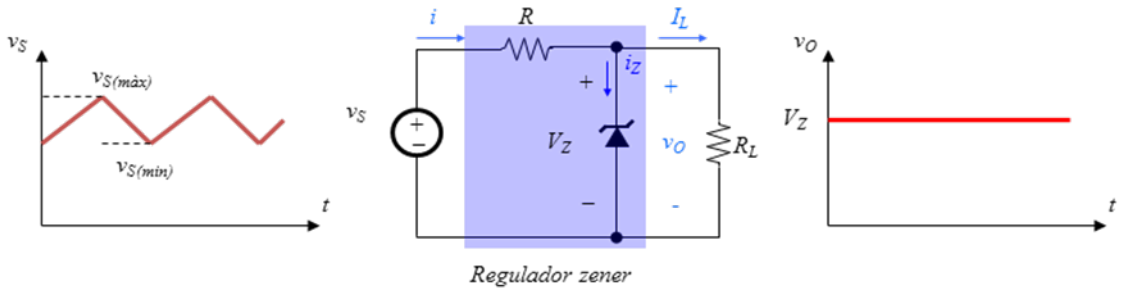


***Figure* 12.** The breakdown region of a real zener diode in more detail



(d)

***Figure* 13.** Zener-based voltage regulator. The goal of the zener is to provide a more stable output in relation to that od the capacitor. In addition, this voltage is independent to power line fluctuations.

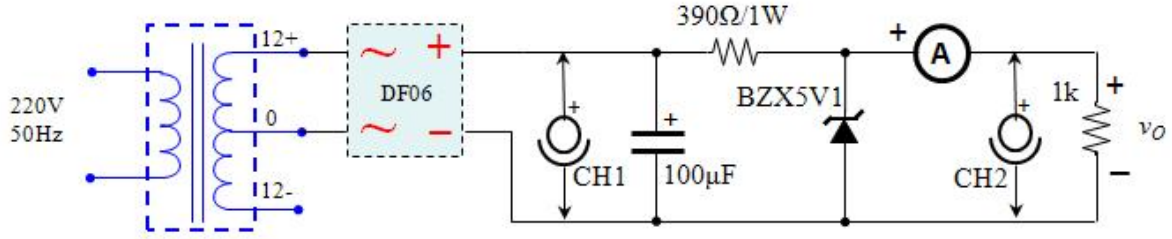


***Figura* 14.** Esquema de la font DC completa amb regulador Zener.

Task LAB3: Obtain the regulator output V_O *and* the electric current I_L and check whether this stage is implementing its function correctly.

- **1)** Using the capacitance value $\boldsymbol{C}$ **= 100µF**, mount the full DC power supply, including the zener-based regulator, as shown in Fig. 14. Use the **5.1V** zener (**BZX5V1**) and the resistor $\boldsymbol{R}$ **= 390Ω/1W**. **2)** Connect the positive terminal of the ammeter at the cathode and the negative terminal at the $\boldsymbol{R_L}$ **= 1kΩ** resistor; and select the DC current option (IDC) **3)** Connect the probe from CH1 in parallel with the capacitor *C* and CH2 in parallel with the resistor R_L. **4)** Turn the transformer on. **5)** Represent both signals in the grid and, using the ammeter write down the values of $\boldsymbol{I_L}$ and use the oscilloscope to measure the ripple $\boldsymbol{V_r}$, and the average voltage, $\boldsymbol{V_O}$.
- Repeat the preceding steps for the resistors: $\boldsymbol{R_L}$ = **560Ω** and $\boldsymbol{R_L}$ = **10kΩ** (There is no need to drqw the waveforms again). Is $\boldsymbol{V_r}$ independent from $\boldsymbol{V_O}$? Explain why.

5. Integrated Regulators (el 7805)

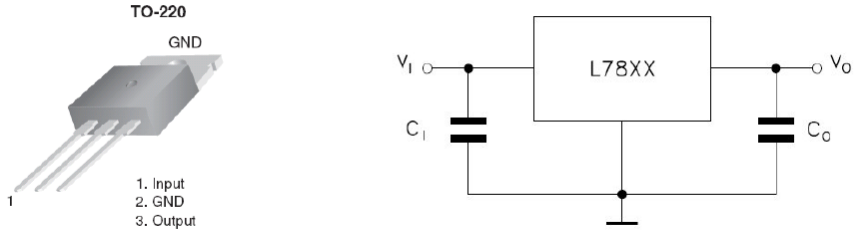
Voltage regulators are also manufactured as integrated circuits, so that they can be used more easily and reliably. One group available from many manufacturers are those regulators of fixed output. Perhaps, the most popular is the family of 78XX regulators from *Intersil* (where XX indicates the fixed output voltage).

One example is the popular 7805 (Fig. 15), which is manufactured by several companies. This is a three-terminal IC able to provide a fixed voltage of 5V at a maximum current of 1A. The IC incorporates a series of peripherals aimed at protecting the devices from overloads, accidental short-circuit and thermal shut-down, among other features.). In addition, if a heat sing is used the output current can be increased up to several amperes. Finally, even though its main functionality is to provide a fixed voltage, one can obtain a variable output by using additional resistors and potentiometers. Table 2 shows the main electrical characteristics provided by the manufacturer.

Task PRELAB4: In the Bread-Board template, draw the connections from the DC power supply based on the 7805 IC (Fig. 16) you'll carry out in the lab session in order to obtain its main electrical parameters 7805 (Fig. 16).

Task LAB4: Mount the circuit in Fig. 16 and check out the correct performance of the DC power supply..

- **1)** Mount the circuit. 2) Measure its output with three different resistors $\boldsymbol{R_L}$: **390Ω, 560Ω** and **1kΩ**. What are the differences, benefits and drawbacks of this configuration in relation to the Zener?



(a) (b)

***Figure* 15.** Voltage regulator 78XX. A) Pin distribution and; b) Basic connection for fixed output.

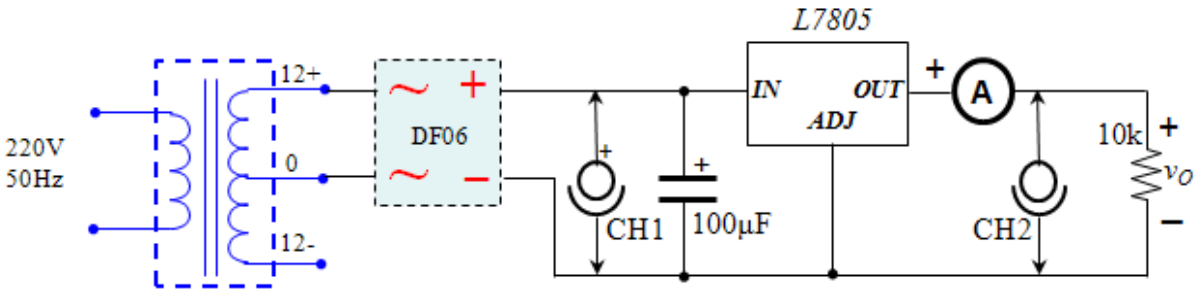


***Figure* 16.** Schematics of a 5V full DC power supply based on the L7805 IC.

Table 4. Electrical characteristics of L7805

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	T_J = 25°C	4.8	5	5.2	V
V_O	Output voltage	I_O = 5 mA to 1 A, V_I = 8 to 20 V	4.65	5	5.35	V
ΔV_O(1)	Line regulation	V_I = 7 to 25 V, T_J = 25°C		3	50	mV
		V_I = 8 to 12 V, T_J = 25°C		1	25	
ΔV_O(1)	Load regulation	I_O = 5 mA to 1.5 A, T_J = 25°C			100	mV
		I_O = 250 to 750 mA, T_J = 25°C			25	
I_d	Quiescent current	T_J = 25°C			6	mA
ΔI_d	Quiescent current change	I_O = 5 mA to 1 A			0.5	mA
		V_I = 8 to 25 V			0.8	
$\Delta V_O/\Delta T$	Output voltage drift	I_O = 5 mA		0.6		mV/°C
eN	Output noise voltage	B =10 Hz to 100 kHz, T_J = 25°C			40	µV/V_O
SVR	Supply voltage rejection	V_I = 8 to 18 V, f = 120 Hz	68			dB
V_d	Dropout voltage	I_O = 1 A, T_J = 25°C		2	2.5	V
R_O	Output resistance	f = 1 kHz		17		mΩ
I_{sc}	Short circuit current	V_I = 35 V, T_J = 25°C		0.75	1.2	A
I_{scp}	Short circuit peak current	T_J = 25°C	1.3	2.2	3.3	A

1. Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Table 2. Main electrical features from the datasheet L7805 from *Intersil*.

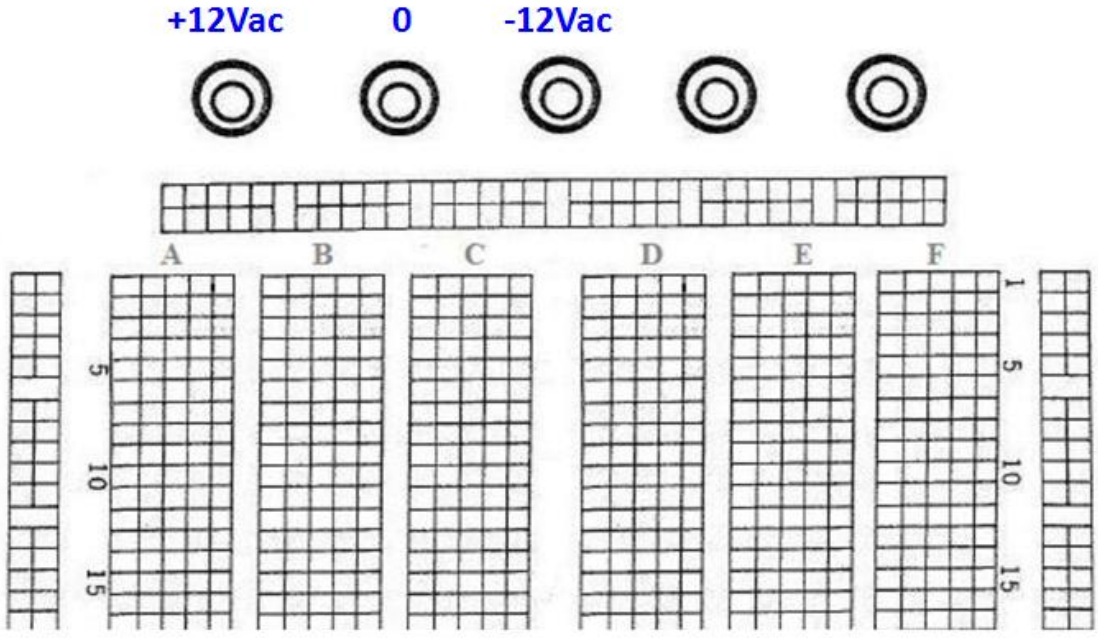
Annex 1 – Results form PRELAB

REMARK: You **MUST DO THESE ACTIVITIES BEFORE THE LAB SESSION CORRESPONDING TO PRT3**

UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH Escola Politècnica Superior d'Enginyeria de Vilanova i la Geltrú	EEL
Sistemes Electrònics (SIEK) **Activity 3:** Introduction to DC supplies **PRELAB**	
Students:	**Date:**

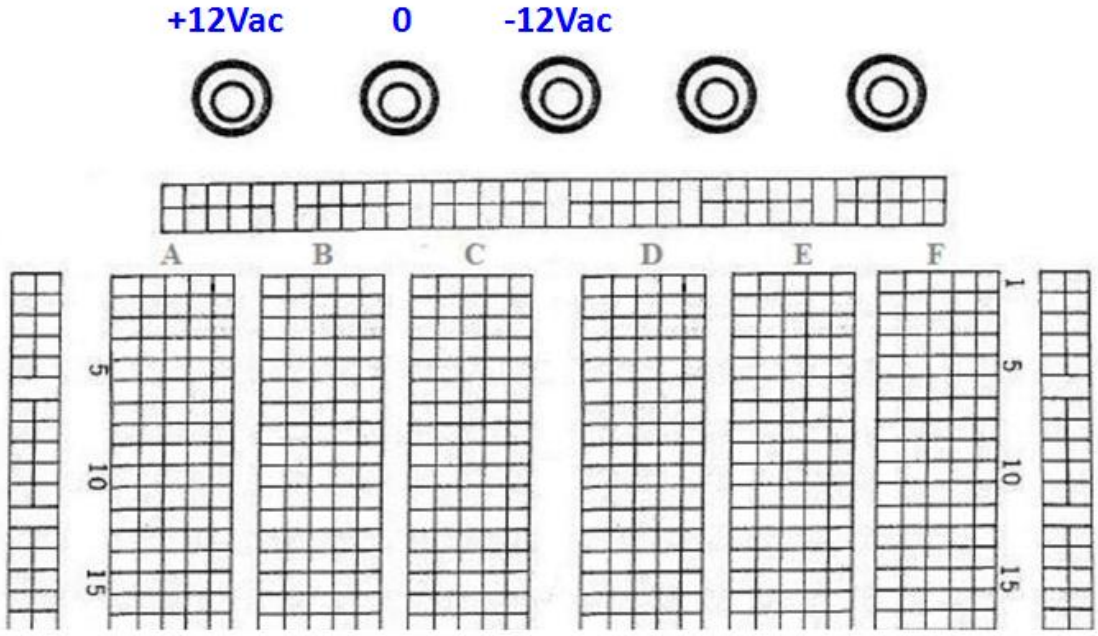
PRELAB 1: *Voltage rectifier circuits*

a) Connections corresponding to the single-phase half-wave rectifier (Fig. 7a)[3]



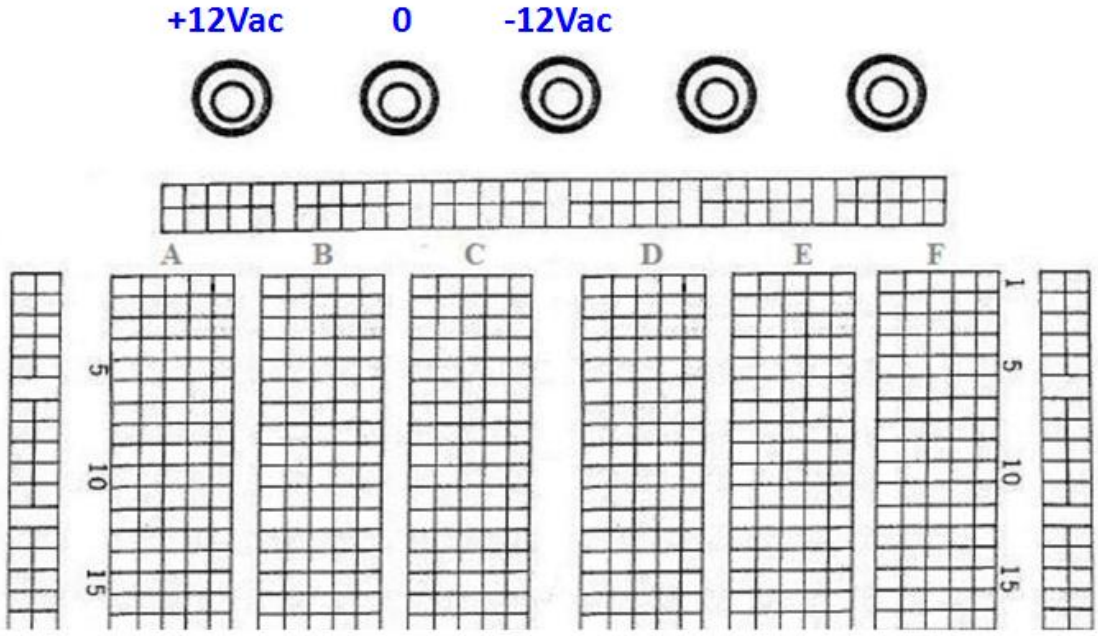
[3] From now on, assume that the three outputs of the transformer are connected to the Board terminals.

b) Connections corresponding to the two-phase half-wave rectifier (Fig. 7b)



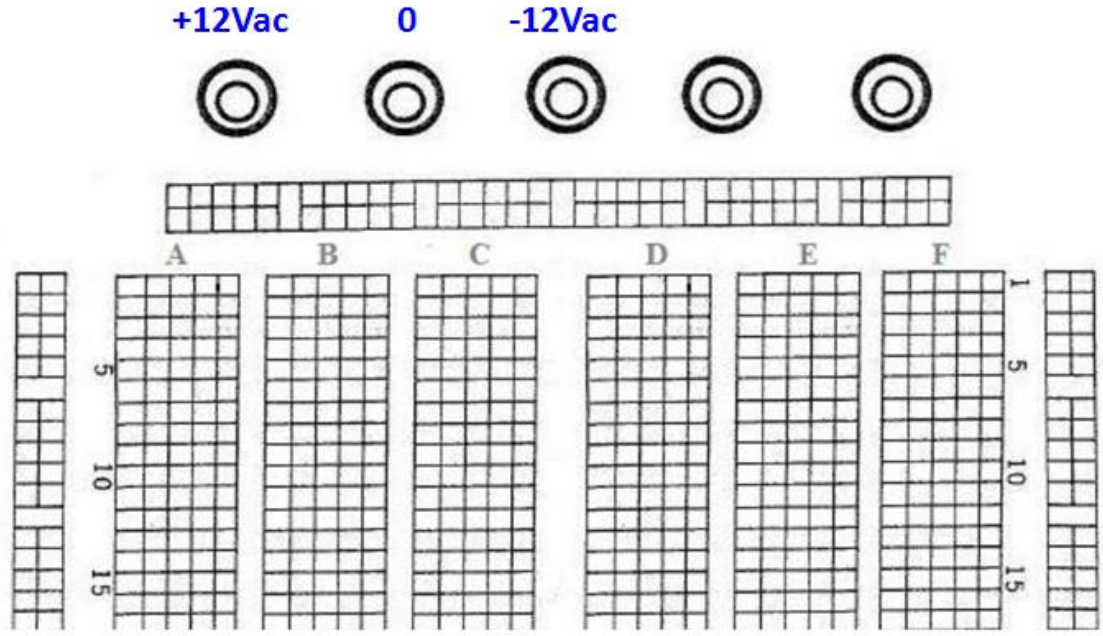
PRELAB 2. Voltage filter

Connections corresponding to the single-phase half-wave rectifier using filter (Fig. 10)



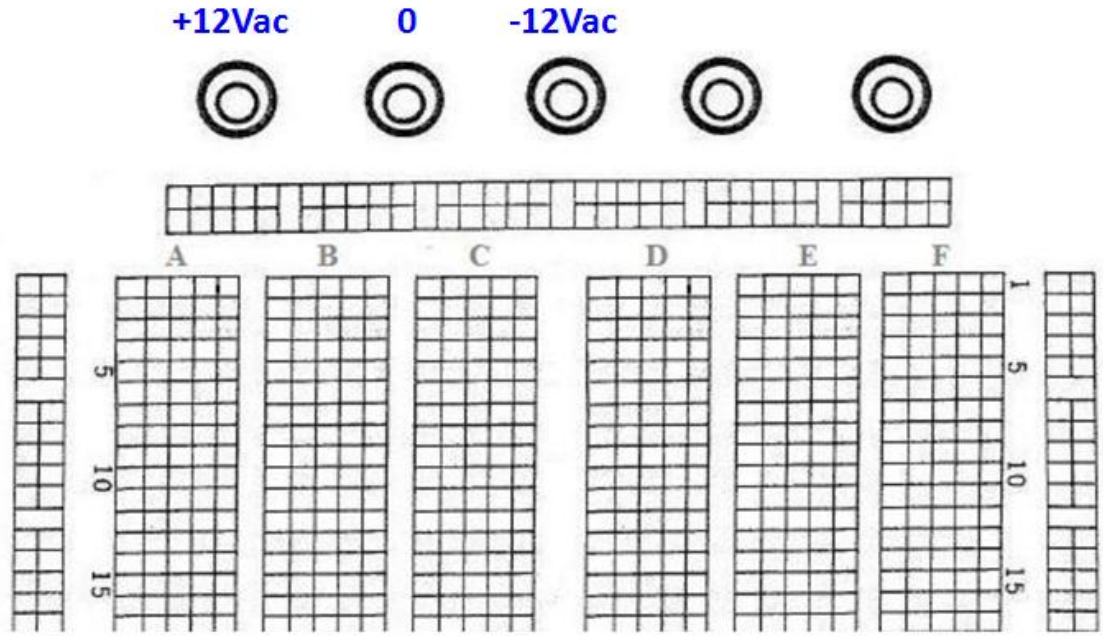
PRELAB 3. Estabilitzador de tensió Zener

Connexions de la font d'alimentació DC completa amb regulador Zener (Fig. 14)



PRELAB 4. Regulador de tensió integrat

Connexions de la font d'alimentació DC completa amb regulador integrat L7805 (Fig. 16)



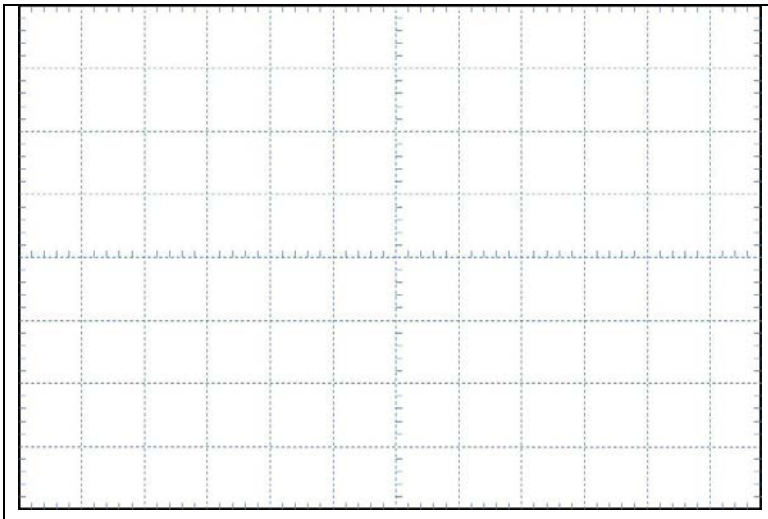
Annex 2 –Lab activities

REMARK: You **MUST PRINT OUT** this form and **TAKE IT WITH YOU** the day of the lab session

UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH Escola Politècnica Superior d'Enginyeria de Vilanova i la Geltrú	EEL
Electronic Systems (SIEK) **Activity 3:** Introduction to DC supplies **FULL DE RESULTATS**	
Estudiants:	**Data:**

LAB 1: Voltage rectifiers

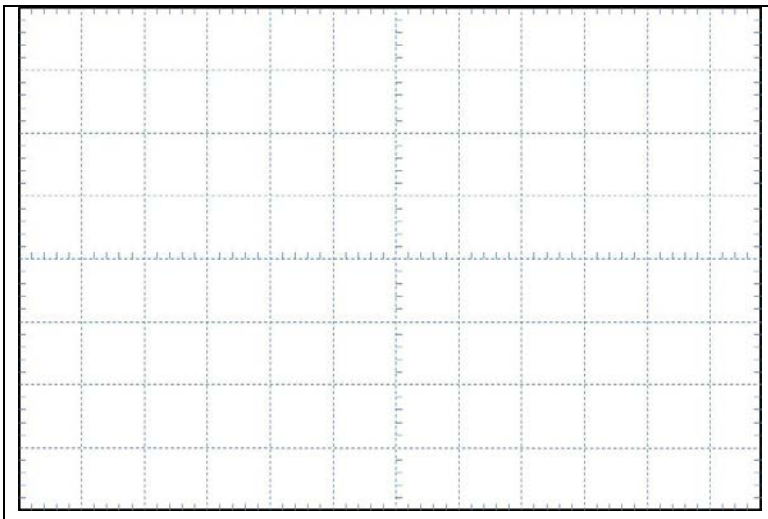
Waveforms $v_I(t)$; $v_O(t)$ and $v_D(t) = v_I(t) - v_O(t)$ observed in the single-phase half-wave rectifier (Fig. 7a).



CH1 VOLT/: **5V/**
Zero POS1: 0V
CH2 VOLT/: 5V/
Zero POS2: 0V
MATH VOLT/: **5V/**
TIME/: 5mseg/
Acob: DC

V_{RRM}: _____ $V_{O(av)}$: _____

Waveforms $v_I(t)$; $v_O(t)$ and $v_D(t) = v_I(t) - v_O(t)$ observed in the two-phase half-wave rectifier (Fig. 7b).

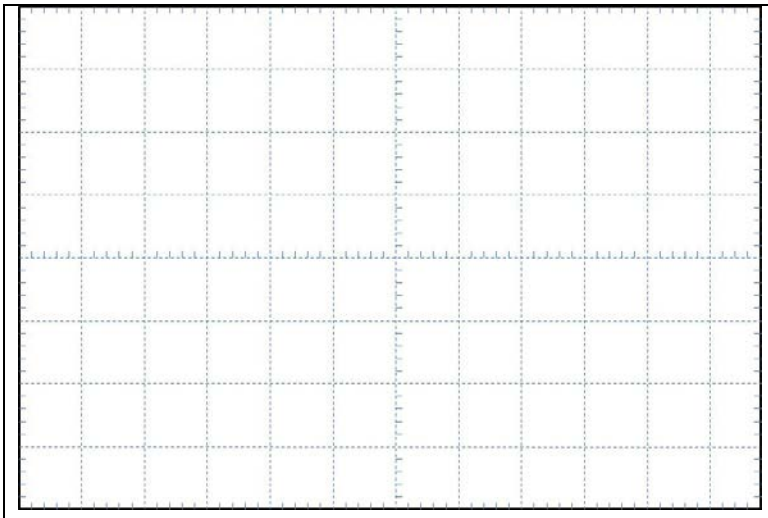


CH1 VOLT/: **5V/**
Zero POS1: 0V
CH2 VOLT/: 5V/
Zero POS2: 0V
MATH VOLT/: **10V/**
TIME/: 5mseg/
Acob: DC

V_{RRM}: _____ $V_{O(av)}$: _____

LAB 2: Voltage filter

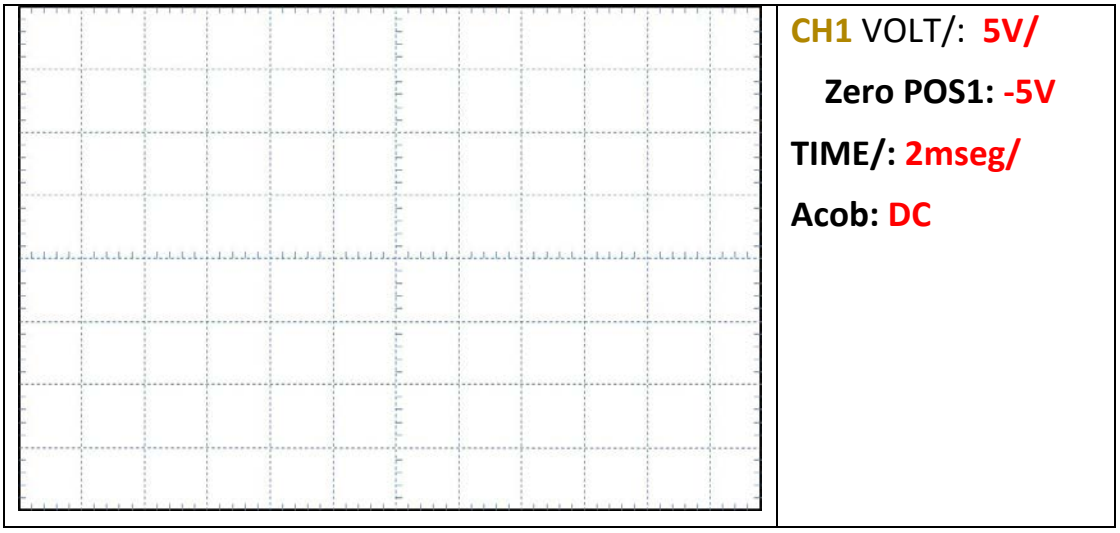
Waveform corresponding to $v_O(t)$ using **C = 100nF**.



CH1 VOLT/: **5V/**
Zero POS1: -5V
TIME/: 2mseg/
Acob: DC

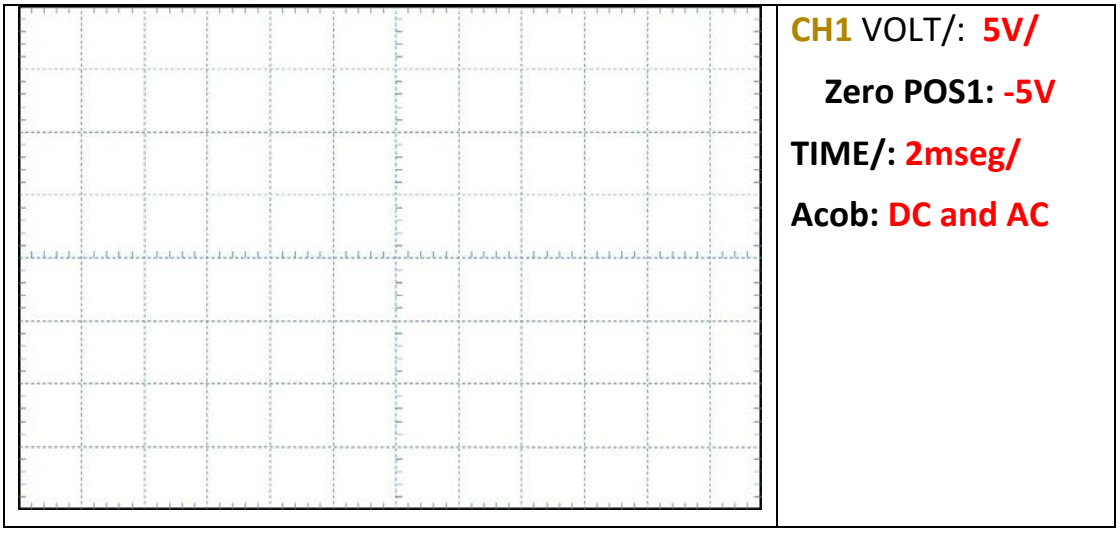
V_{Omax}: _____ V_{Omin}: _____ V_r: _____ $V_{O(av)}$:_____

Waveform corresponding to $v_O(t)$ using **C = 10µF**.



V_{Omax}: _____ V_{Omin}: _____ V_r: _____ $V_{O(av)}$:_____

Waveform corresponding to $v_O(t)$ using **C = 100µF**.



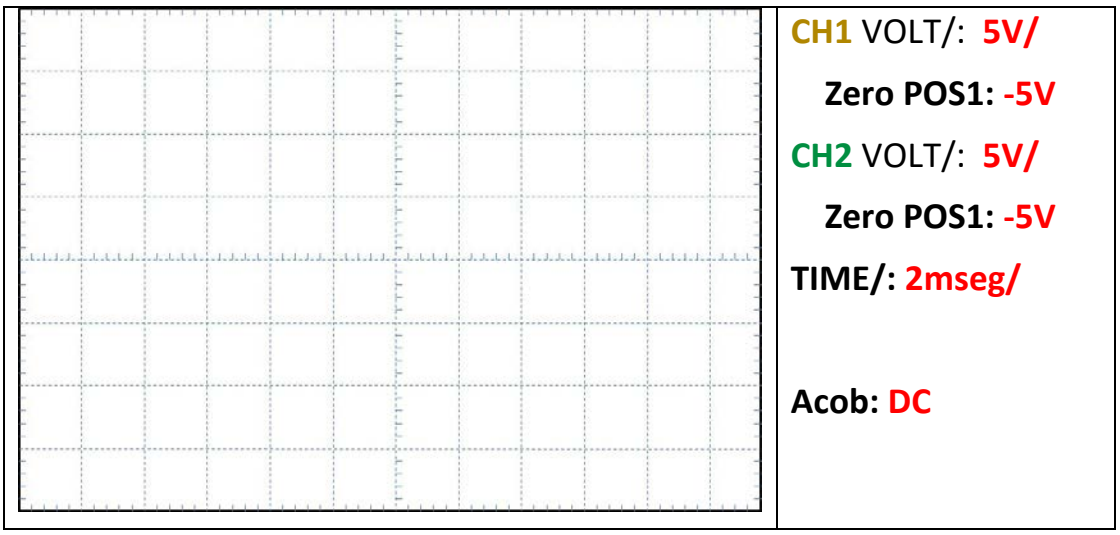
V_{Omax}: _____ V_{Omin}: _____ V_r: _____ $V_{O(av)}$:_____

Explain the results:

_____
_____
_____

LAB 3: Voltage regulator

Waveforms corresponding to $v_c(t)$ and $v_O(t)$



Variable	R_L = 560Ω	R_L = 1kΩ	R_L = 10kΩ
V_r			
V_O			
I_L			

***Table* 3.** Electric variables corresponding to the Zener regulator

Is V_r independent from V_O? Explain why

LAB 4: Voltage regulator using integrated circuit

Variable	R_L = 390Ω	R_L = 1kΩ	R_L = 10kΩ
V_r			

V_O			
I_L			

***Taula* 4.** Electric variables corresponding to the IC regulator L7805

Explain the difference of results regarding to the Zener configuration of section LAB3. What are the improvements and drawbacks of this configuration?

_____
_____
_____
_____
_____

Lab Activity 4. Switching Electronics: the *Bipolar Junction Transistor* (BJT)

Main goal: To understand the performance of the bipolar transistors (aka BJT)[1] and knowing its main application in the field of switching electronics (analog, digital and mixed).

1 Introduction

In this lab activity you'll get introduced to the most common three-terminal electronic device: the *bipolar junction transistor* (BJT). Its operation principle is quite similar to a two-terminal current source which is controlled from another terminal. That is, the electric current at the *base* terminal (B) sets (or controls) the amount of current flowing from the *collector* terminal (C) to the emitter (E).

Both electric symbols and current/voltage conventions are shown in Fig. 1. In general, we find two types of BJT: the *npn* (Fig. 1a) and the *pnp* (Fig. 1b). Their main difference lie on the sign convention used in all variables, which is opposite in relation to the other.

As for the electric currents in each of the terminals, it holds that:

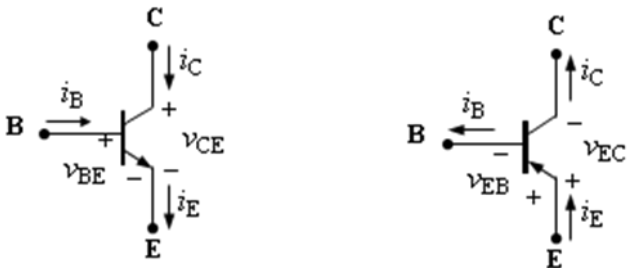
$$i_E = i_B + i_C \,. \tag{1}$$

On the other hand, v_{BE} corresponds to the voltage drop between base and emitter terminals, whereas v_{CE} is the collector-emitter voltage.

Unlike the diode, the BJT is able to operate up to three regions depending on the different conditions that may be given in the electrical variables when the three terminals are connected to other components (see Table 1):

- When the base current i_B is zero, there is no current flow at the collector terminal i_C=0. In this case, we say that the BJT operates in the **CUTOFF** mode. This happens whenever the v_{BE} voltage is under the threshold level $V_{BE\gamma}$ (typically $\boldsymbol{V_{BE\gamma}}$ **= 0.7V**), specified by the manufacturer's datasheet.
- When the electric power at the base is significantly enough so as to make the base current i_B greater than zero, the BJT leaves the cutoff region and enters in **ACTIVE** mode. The BJT will remain in this region as long as i_B is significantly enough to keep the v_{CE} voltage above the threshold level $V_{CE(sat)}$ (also specified in the datasheet). In this situation, v_{BE}=$V_{BE\gamma}$ and i_C is proportional to i_B. The *gain* in current that is obtained between this to variables is denoted as h_{FE} and is also provided by the manufacturer in the datasheet.

[1] From now on we will use these terms to refer to this type of electronic semiconductor



(a) (b)

Figure 1. The BJT. Symbols and electric current/voltage sign conventions. a) *npn*, b) *pnp*.

Operating zone	Electrical conditions	Electrical behavior
Cutoff (OFF)	$v_{BE} < V_{BE\gamma}$, $v_{CE} > V_{CE(sat)}$	$i_B = 0$, $i_C = 0$
Active	$i_B > 0$, $v_{CE} > V_{CE(sat)}$	$v_{BE} = V_{BE\gamma}$, $i_C = h_{FE} i_B$
Saturation (ON)	$i_B > 0$, $i_B > i_C/h_{FE}$	$v_{BE} = V_{BE\gamma}$, $v_{CE} = V_{CE(sat)}$

Table 1 Operating modes in the *npn* BJT: electric conditions and device behavior are specified. The same considerations apply to the *pnp* type when changing the variable index, i.e. $v_{CE} \rightarrow v_{EC}$.

- When i_B is very large, the relation $i_C = h_{FE} i_B$ is not fulfilled anymore and the BJT enters the **SATURATION** mode. The voltage v_{CE} takes its minimum value ($v_{CE(sat)}$), and v_{BE} is the same as in the active region, $V_{BE\gamma}$.

Fig. 2 summarizes the BJT *i-v* characteristics. In fact, the *base-emitte*r junction acts as a diode: in both active and saturation regions this BE junction is in ON mode ($v_{BE} = V_{BE\gamma}$ i $i_B > 0$), whereas in the cutoff region this junction is in OFF mode ($v_{BE} < v\ V_{BE\gamma}$ i $i_B = 0$).

In order to understand these three operating regions, consider the BJT circuit of Fig. 3, where V_{in} is some variable input voltage. Applying both KVLs at the input and output meshes (left and right, respectively) we obtain:

$$V_{in} - R_B i_B - v_{BE} = 0 \tag{2}$$

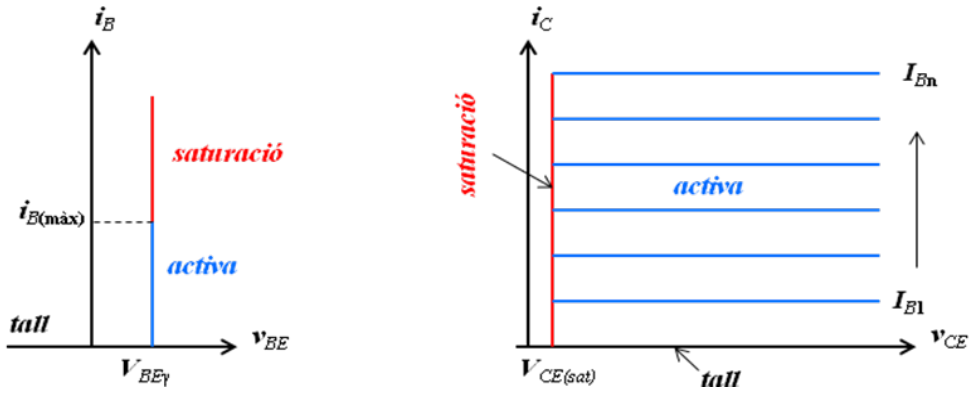
$$v_2 - R_C i_C - v_{CE} = 0 \tag{3}$$

- ***CUTOFF*** operation**:** The boundary of V_{in} between the cutoff and active mode is obtained by using the condition $v_{BE} < V_{BE\gamma}$ and setting $i_B = 0$ in (2) (see Table 1). So the condition of $\boldsymbol{V_{in}}$ **in the cutoff region is,**

$$V_{in} \leq V_{BE\gamma} . \tag{4}$$

Since $i_C = 0$, the condition $v_{CE} > V_{CEsat}$ must hold, so,

$$v_{CE} = V_2 > V_{CE(sat)} \tag{5}$$



(a) (b)

Figure 2. The BJT *i-v* transfer characteristics. a) Input: $i_B - v_{BE}$. b) Output: $i_C - v_{CE}$.

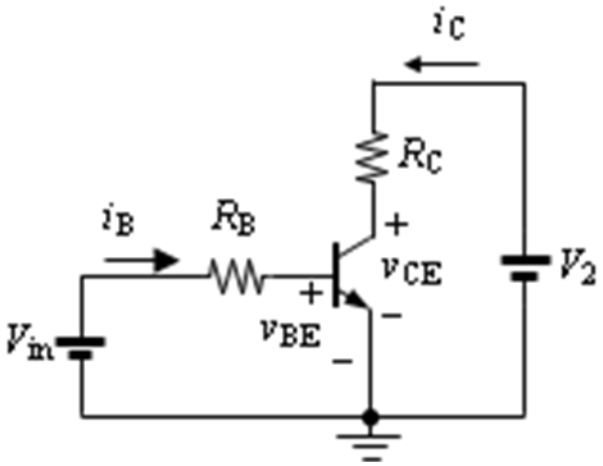


Figure 3. Schematics of the basic BJT configuration: *npn* type.

- **ACTIVE** operation: It is clear that the input condition must be opposite to (4) if the BJT is to operate in this region. Indeed, expressing i_B from (2) and using the equality $v_{BE} = V_{BE\gamma}$ we obtain,

$$i_B = \frac{V_{in} - v_{BE}}{R_B} \geq 0 \quad \rightarrow \quad V_{in} \geq V_{BE\gamma} \,. \tag{6}$$

However, this is not the only condition for the active region because, on the other hand, when i_B is large enough the BJT may enter the saturation region. The other boundary is determined using the condition $v_{CE} > V_{CE(\text{sat})}$. In addition, since we have $i_C = h_{FE} i_B$ in active mode, using (6) in (3) leads to the condition,

$$V_{in} \leq R_B \frac{v_2 - V_{CE(sat)}}{R_C h_{FE}} + V_{BE\gamma} \,, \tag{7}$$

Therefore, the **active region** is obtained within the input range**,**

$$V_{BE\gamma} \le V_{in} \le R_B \frac{v_2 - V_{CE(sat)}}{R_C h_{FE}} + V_{BE\gamma} . \quad (8)$$

In this situation, it holds that the output v_{CE} is,

$$v_{CE} = V_2 - R_C i_C = V_2 - R_c h_{FE} \frac{V_{in} - V_{BE\gamma}}{R_B} \quad (9)$$

- ***SATURATION*** operation: Obviously, the saturation condition is the opposite to (7). To confirm this hypothesis we use the condition

$$i_B > \frac{i_C}{h_{FE}} \quad (10)$$

from Table 1. In this case, the equalities $v_{BE} = V_{BE\gamma}$ and $v_{CE} = V_{CE(sat)}$ must hold so, if we use (3), i_C is readily obtain as,

$$i_C = \frac{v_2 - v_{CE}}{R_C} = \frac{v_2 - V_{CE(sat)}}{R_C} . \quad (11)$$

Using (6) and (11) in (10) allows **the BJT saturation condition** to be obtained as,

$$\frac{V_{in} - V_{BE\gamma}}{R_B} > \frac{v_2 - V_{CE(sat)}}{R_C h_{FE}} \quad \rightarrow \quad V_{in} > R_B \frac{v_2 - V_{CE(sat)}}{R_C h_{FE}} + V_{BE\gamma} \quad (12)$$

which, of course, is the opposite to active mode.

Table 2 summarizes all the conditions for the BJT behavior in this circuit. As shown, with no input ($V_{in} = 0$) the collector-emitter voltages (v_{CE}) takes its maximum value (V_2) and $i_C = 0$. However, if the input level is greater than the value obtained from (12) the output is almost zero ($v_{CE} = V_{CE(sat)} = 0.2$V) and $i_C \neq 0$.

So, in cutoff mode the transistor opens the circuit between collector and emitter when $V_{in} = 0$, and they are shorted when $V_{in} > V_{BE\gamma}$. On the other hand, the BJT has a linear behavior in active mode, as shown in (9). For this reason, the BJT is considered one of the most important general purpose semiconductor used in electronics: ranging from *signal amplifiers*, *power control systems*, *digital switches* and *memory* devices, among others.

Region	Conditions	Circuit behavior
Cutoff	$v_{\text{in}} < V_{\text{BE}\gamma}$	$i_B = 0,\ i_C = 0$ **and** $v_{CE} = V_2$
Active	$V_{BE\gamma} \le V_{in} \le R_B \dfrac{v_2 - V_{CE(sat)}}{R_C h_{FE}} + V_{BE\gamma}$	$i_C = h_{FE} i_B\ v_{CE} = V_2 - R_C i_C$
Saturation	$V_{in} > R_B \dfrac{v_2 - V_{CE(sat)}}{R_C h_{FE}} + V_{BE\gamma}$	$i_B = \dfrac{V_{in} - V_{BE\gamma}}{R_B}$ $i_C = h_{FE} i_B\ v_{CE} = V_2 - R_C i_C$

Table 2. Summary of operating modes in the circuit of Fig. 3

For brevity, we will only consider switching applications in this activity (cutoff and saturation regions). The reader can find some application examples of the BJT operating in active mode in Annex 1.

Task PRELAB 0. Search the web for information on the bipolar transistor **BC547C** and specify its main characteristics.

- Look for the datasheet of the reference BC547C and draw its contour Package in the box provided. Identify each of the terminals: *collector*, *base* and *emitter*; and specify the value of $\boldsymbol{h_{FE}}$, $\boldsymbol{V_{Be\gamma}}$ i $\boldsymbol{V_{CE(sat)}}$

2. The BJT as main logic unit in Digital Circuits

The previous circuit (Fig. 3) is one way of implementing a logic inverter (the NOT gate). The term “logic” refers to the fact that it is a circuit generating ON/OFF commands. As such, they find applications in decision making tasks.

Very often, when talking about digital electronics, the “0” and “1” value is used to designate the OFF and ON state, respectively. The “0” denotes the lower level voltage (0V), whereas the high level “1”corresponds, for example, to 5V.

The NOT, OR and AND gates, with their inverted versions (NOR and NAND) and the EX-OR gate; are some of the binary functions used in digital electronics (Fig. 4). As for the NOT gate, when the input level is “0” the output is “1”. On the other hand, the output is “0”. This behavior is represented by the following logic expression:

$$O = \overline{A} \tag{13}$$

where the upper line denotes variable inversion.

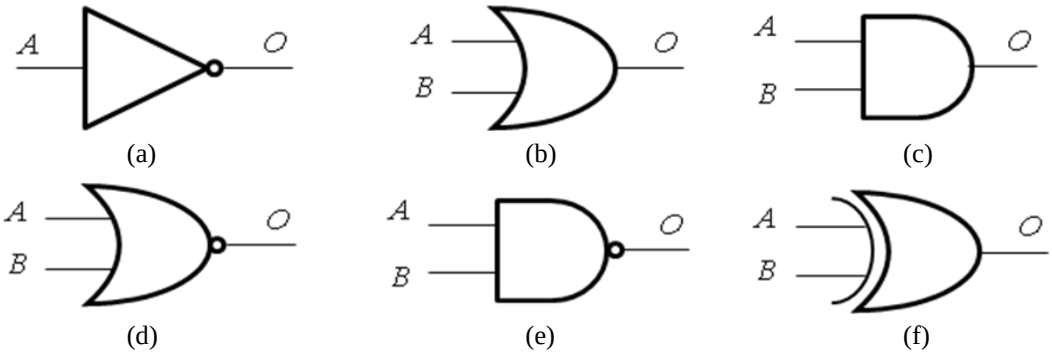


Figure 4. Some of the basic binary digital functions: a) the NOT gate; b) The 2-input OR gate; c) The AND; d) The NOR; e) The NAND; f) The EX-OR.

Comb.	***A***	***B***	***NOT***	***OR***	***AND***	***NOR***	***NAND***	***OR-E***
0	**0**	**0**	1	0	0	1	1	0
1	**0**	**1**	1	1	0	0	1	1
2	**1**	**0**	0	1	0	0	1	1
3	**1**	**1**	0	1	1	0	0	0
Logic function			$O=\overline{A}$	$O=A+B$	$O=AB$	$O=\overline{A+B}$	$O=\overline{AB}$	$O=A\oplus B$

Table 3. Truth table corresponding to the basic binary functions in Fig. 4.

The circuit in Fig. 5a modifies the inverter circuit so as to turn a led on when the input is v_{in} = 0V and turn it off otherwise (v_{in} = 5V). This is the performance:

- When the switch position is *S*=*A* (Fig. 5b), the input is $\boldsymbol{v_{in}}$ **= 5V** (V_{CC}). In this case, the transistor *Q* works in **saturation mode** but to make this possible, the value R_B cannot be any. That is, if $v_{CE} = V_{CE(sat)}$, the collector current is

$$i_{RC} = i_C = \frac{V_{CC} - V_{CE(sat)}}{R_C}. \tag{14}$$

Note that in saturation mode, the collector-emitter voltage, $\boldsymbol{v_{CE} = V_{CE(sat)}}$, is not enough to turn the led on (or else the value should be $\boldsymbol{v_{CE} > V\gamma_{led} = 1.2V}$). Therefore, the condition for the transistor to operate in saturation mode is:

$$i_{RB} > \frac{i_C}{h_{FE}} = \frac{V_{CC} - V_{CE(sat)}}{R_C h_{FE}} \tag{15}$$

where i_{RB} is obtained from the input mesh in a way very similar to (2),

$$i_{RB} = \frac{v_{in} - V_{BE\gamma}}{R_B}. \tag{16}$$

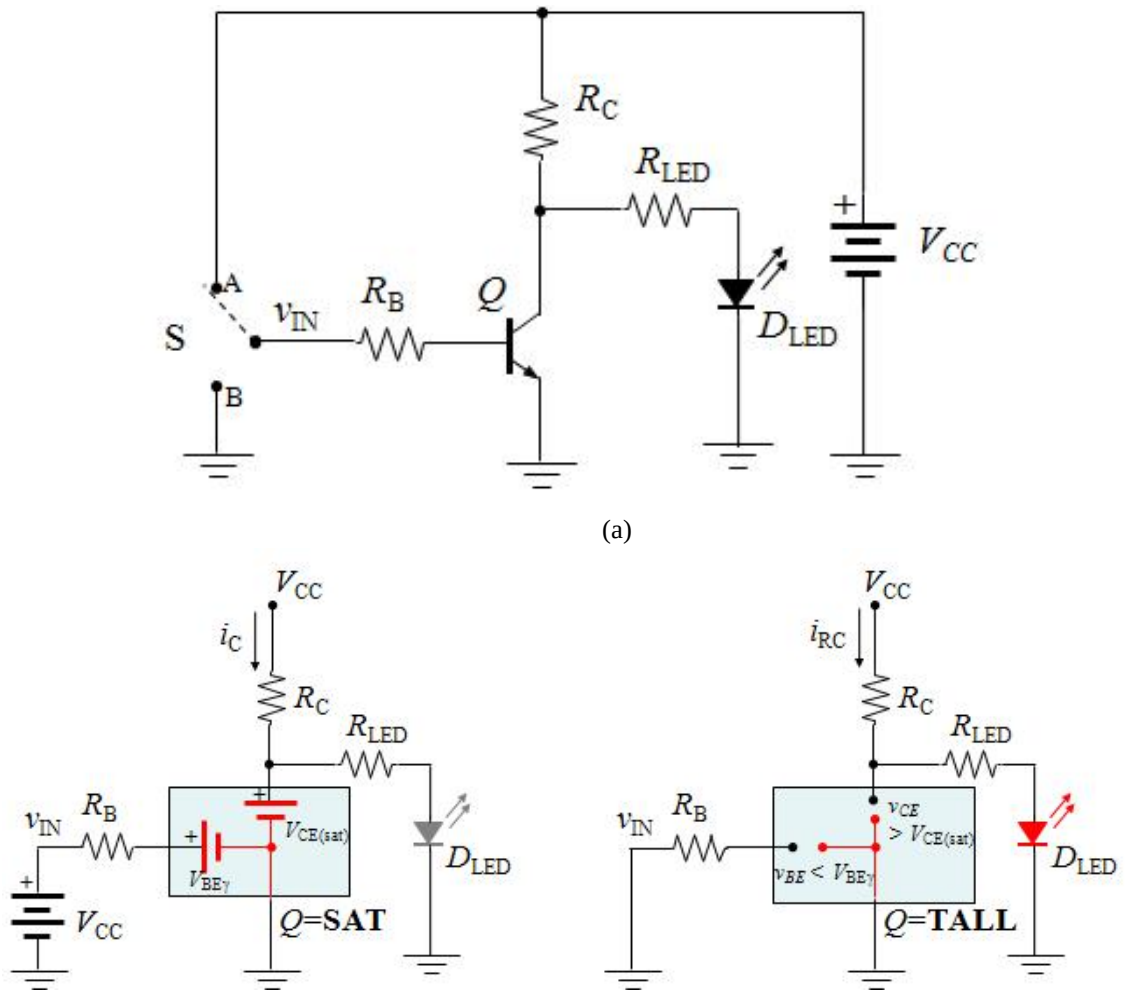


Figure 5. Implementation of a logic NOT gate using a BJT and a LED. a) Electric diagram; b) Operation with $S = A$; c) Operation with $S = B$.

Substituting (16) into (15) and equating R_B permits to obtain the design expression of this component so that the BJT can work in the saturation region (and not the active one) when v_{in} = 5V:

$$R_B < \frac{v_{in} - V_{BE\gamma}}{V_{CC} - V_{CE(sat)}} R_C h_{FE} \approx 0.9 R_C h_{FE} \tag{17}$$

- On the other hand, for S=B, v_{IN} = 0V (Fig. 5c) the BJT operates in cutoff mode. This is only possible if $v_{in} < V_{BE\gamma}$. Since $i_B = i_C = 0$, the current flows to the led passing through R_C and it will be turned ON. In this case,

$$v_{CE} = R_{LED} i_{RC} + V_{\gamma led} \tag{18}$$

where,

$$i_{RC} = \frac{V_{CC} - V_{\gamma led}}{R_C + R_{LED}} \tag{19}$$

In other words, $i_{R1} > 0$ the led is turned on whenever the supply voltage (habitually 5V) is set above the led threshold ($V_{CC} > V_{\gamma led}$). Only in this way, the

condition $v_{CE} = R_{LED}i_{R1} + V\gamma_{led} > V_{CE(sat)}$ can be satisfied to force the BJT operating in the cutoff mode when S=B.

Task PRELAB 1. In the Board template provided in Annex 2, draw the circuit connections of the inverter in Fig. 6. Include the oscilloscope connections for measuring both the output $v_O = v_{CE}$ and base signal v_B when the waveform generator is connected.

- Specify component distribution, wires and instrument connections for taking the corresponding measurements.
- Draw the signals you'll expect to observe on screen for a **TTL** input ($\boldsymbol{v_{in}}$) ranging from **0** to **5V**, and frequency $\boldsymbol{f}$ **= 1Hz**, assuming that CH1 is Connected to v_B and CH2 to v_{CE}

Task LAB1. Mount the circuit of Fig. 6 and use the oscilloscope to observe both the base voltage v_B and the output voltage v_{CE}.

- **1)** Mount the circuit. **2)** Configure the waveform generator with a frequency $\boldsymbol{f}$ **= 1Hz** and connect its **TTL** output (0 a 5V) to the circuit. **3)** Configure the oscilloscope settings to observe on screen an entire cycle with CH1 connected at v_B and CH2 at v_{CE}. **4)** Represent both signals. Make comments about the results justifying, for example, the logic levels ("0" and "1", respectively) by means of expressions (14) – (19).

3. Electronic Switches.

One of the main utilities of the BJT operating in switching mode (cutoff and saturation) is the *electronic switch*. Electronic switches are very used for electrically connecting and disconnecting all kind of devices. One example is the BCD[2] *display* using 7 leds for monitoring characters and decimal values (Fig. 7).

The 7-segment BCD display consists of seven integrated led diodes (eight, including the decimal point) distributed strategically so as to represent the number "8". Each segment is represented with a letter: "a" "b", "c", "d", "e", "f", "g" and "dp"; and are assembled in a way that each led can be activated independently. Some examples are:

- The number "**8"**, activating all segments.
- The number "**0**", activating: "a", "b", "c", "d", "e" and "f".
- The number "**2**", activating: "a", "b", "e", "d" and "g".
- The number "**4**", activating: "b", "c", "f" and "g".

[2] BCD stands for Binary-Coded Decimal and serves to designate the conversion of a decimal number to a binary code. In the 7-segment BCD display, however, this differs from this definition, as an additional conversion is necessary: decimal-to-binary and binary-to-BCD, respectively. There are integrated circuits, such as the 74LS47, which develops this last functionality in a transparent way to the user.

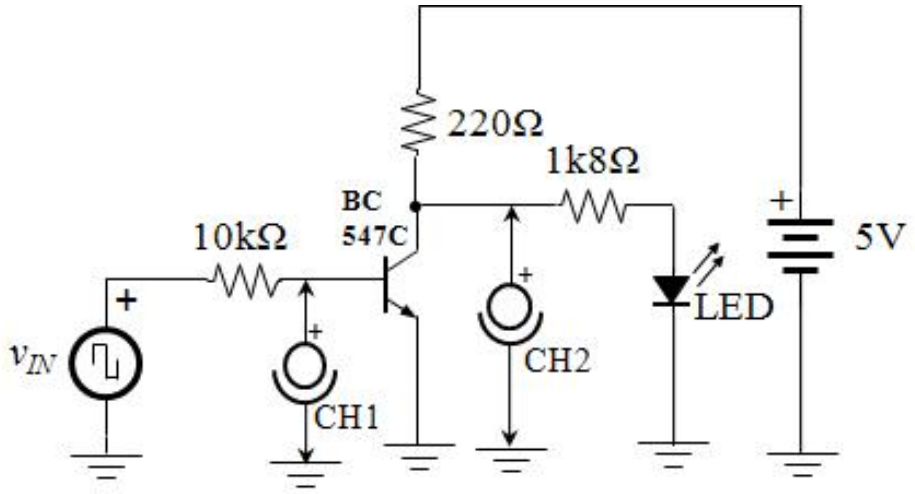
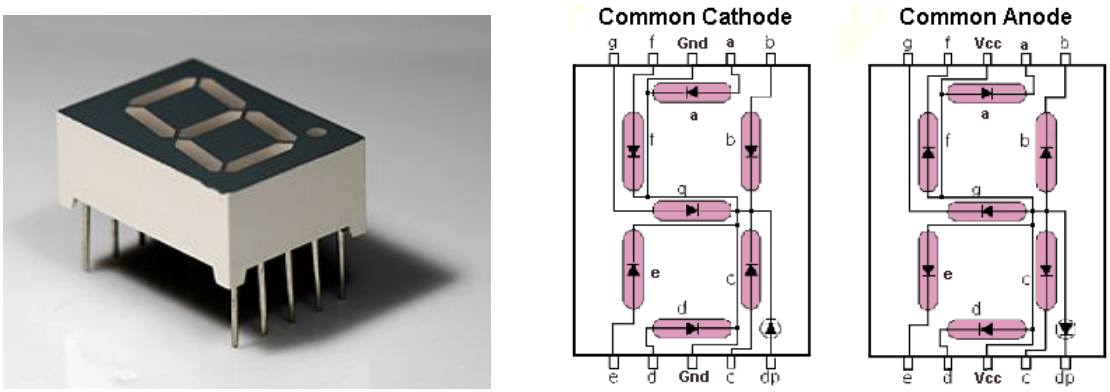


Figure 6. Connection diagram corresponding to the inverter circuit (NOT) in Task LAB1



(a) (b)

Figure 7. The 7-segment BCD display. a) Aerial view, b) Internal connection for the *common cathode* configuration (left) and *common anode* (right)

There are two types of 7-segment BCD displays: *common anode* and *common cathode*. In the first type, all diode anodes are internally connected to the V_{CC} terminal. As such, turning a led on requires setting the corresponding terminal to "0" by means of a biasing resistor, and connecting the V_{CC} to power. The resistor is necessary to limit the amount of current flowing through the led. In the second type, however, the cathode is the common terminal and is connected to GND, instead. As such, the resistor must be connected in order to set the corresponding pin to "1".

The circuit of Fig. 8 is an example of a BJT-based enabling system for a 7-segment BCD display, in the goal of representing the character related to the ON/OFF position of eight integrated switches in a single package (Fig. 9a). When *S*=*A* the input voltage is v_{IN} = 0, and the transistor will operate in cutoff mode. The collector current will be i_C = 0 and all leds will be turned off. When *S*=*B*, the input will be high (v_{IN} = 5V). This closes the path to ground and ($i_C \neq 0$) through the integrated resistors (9A102G, Fig. 9b) and turns the corresponding led ON. The display is then enabled and will show the character represented by the array of switches.

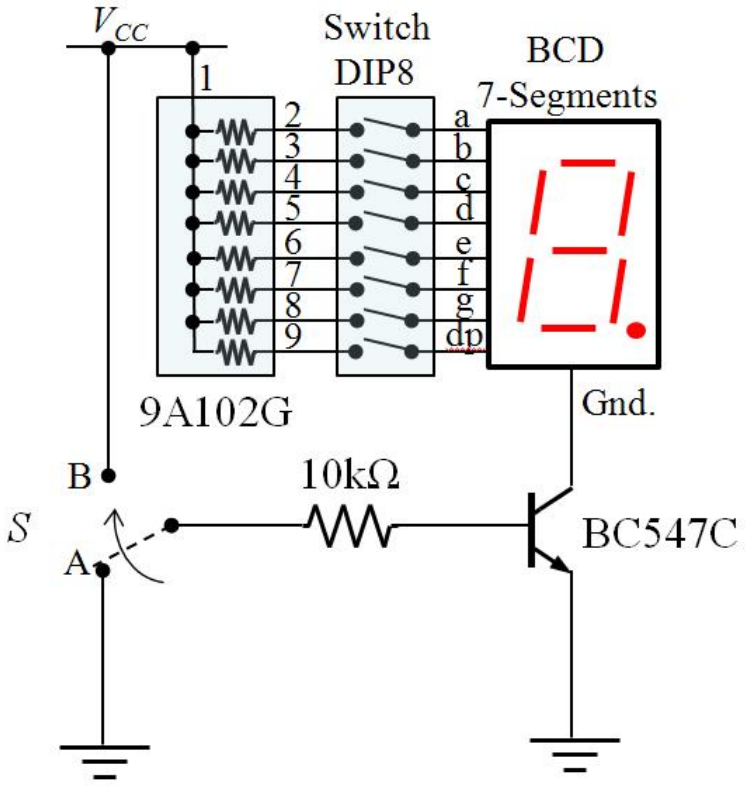
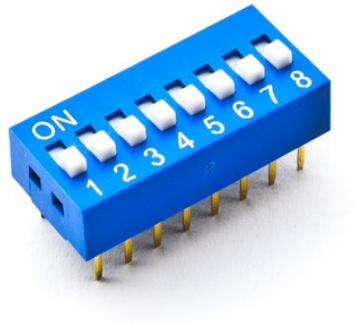
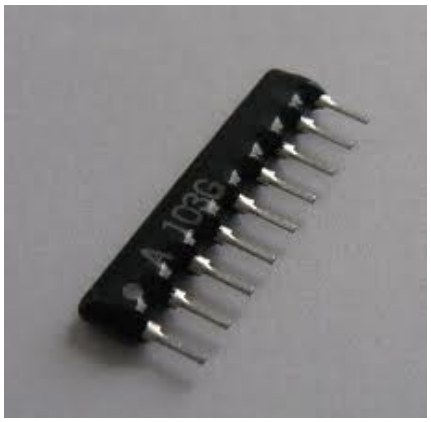


Figure. 8. Enabling System of a 7-segment BCD display to be implemented in Task LAB2.



(a)



(b)

Figure. 9. Other mechanical and passive elements of the circuit in Fig. 9. a) DIP8-switch[3] used in the activation of all leds from the 7-segments BCD display; b) Integrated circuit 9A102G. It contains eight 1kΩ resistors with one terminal Connected to a common pin.

Task PRELAB2. Identify the new components in the circuit of Fig. 8. Then, use the Board template to draw the connections you need to develop in order to make the enabling circuit of Fig. 8 work.

- Use the web for looking for information on the 9A102G and LSD5355 integrated circuits. In the case of the 9A102G specify the meaning and the way

[3] DIP – Dual In-line Package

of specifying the common pin. Which type of BCD display is necessary for in Fig. 8: *common cathode or common anode*?

Task LAB2. Mount the circuit of Fig. 8 and check its behavior

- **1)** Mount the circuit on the Bread-Board. Place the components so as to minimize wire connections. **2)** With the selector switch at position $S = A$, connect the power supply V_{CC} **= 5V**. **3)** With all switches in the DIP8-switch turned on, change the selector position ($S = B$). Mark the leds corresponding to the number represented in the display.
- Change the position of switches in order to represent other decimal numbers and characters. Develop three examples, and indicate your selection in the results form specifying the configuration of switches in the table.
- How would you use the waveform generator in order to show the number 8 (including decimal point) with a blinking pattern of 1-second interval? Specify the configuration of the waveform generator.

4. *Latch* SET/RESET (Optional section)

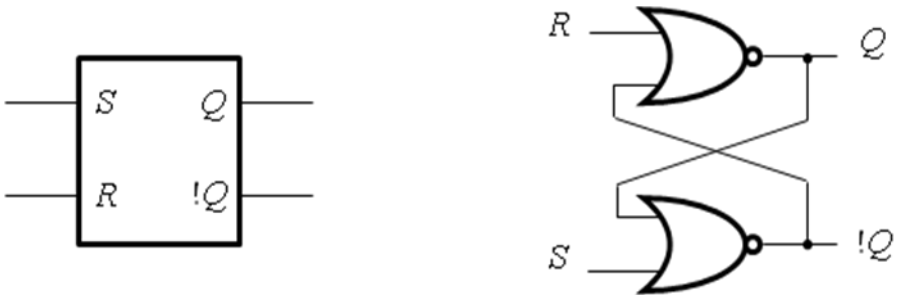
In the digital functions introduced in section 3, the logic output is updated by the inputs at the same instant time *t*. That is, the inputs, and solely the inputs, specify the output of the system. This performance is known as a "memory-less" system.

Digital circuits become interesting when they have memory. That is, they recall their last previous states. This allows, among different things, *digital counters*, *arithmetical accumulators* and all forms of circuits that work in a **sequential fashion** (one function executed after the other) to be implemented. Hence, it is said that this sort of digital systems use "sequential logic".

The most basic memory unit in digital circuits is known as the *latch* (or two-shot multivibrator). One type is the SET/RESET multivibrator (Fig. 9). Its output can be SET $\{Q = 1\}$ or RESET $\{Q = 0\}$. In general, the output is modified using the 2nd and 3rd combination in Table 4 but, if $S = 0$ and $R = 0$, it remains unchanged, remembering the value updated in the previous state (see Fig. 10).

Fig. 11 shows the electric diagram of a SET/REST multivibrator implemented with discrete components, including two bipolar transistors. As the NOT gate, both BJT can operate either at **cutoff** ($I_C = 0$) or **saturation** ($V_{CE} \approx 0$) mode. This is the circuit performance:

- When the power supply V_{CC} is connected, both BJTs (T_1 and T_2) start their conduction cycle, since both base terminals are driven by positive voltages: T_1 through resistors $R_2 - R_6 - R_7$; and T_2 through $R_1 - R_5 - R_8$. However, not both transistors are identical (because of the tolerances within their manufacturing process caused by different level of impurities in the silicon material), so one transistor will conduct before the other.



(a) (b)

Figure 9.SET/RESET multivibrator. a) Symbol; b) Implementation using 2-input NOR gates.

Cases	***S***	***R***	***Q***	***!Q***
1	0	0	Q^*	$!Q^*$
2	0	1	0	1
3	1	0	1	0
4	1	1	X	X

Table 4. Truth table of the SET/RESET multivibrator. Q* and !Q* denote previous output (before a ner update of the SET/RESET terminals is reached. !*Q* means inversion of *Q*. The combination *S*=*R*=1 is not valid in the SET/RESET multivabrator and is denoted with X.

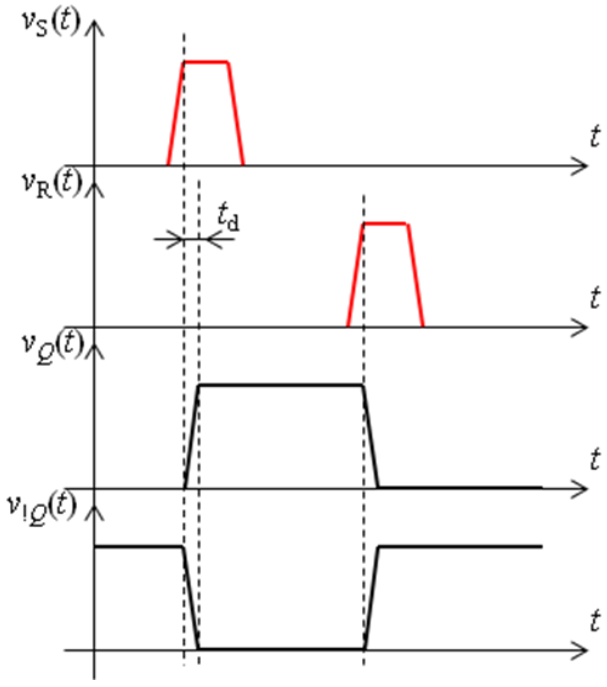


Figura 10. Behavior example of the SET/RESET multivibrator by means of a time diagram. Note that the output can be either *Q* = 0, or *Q* = 1 with *S* = *R* = OFF, depending on the previous state.

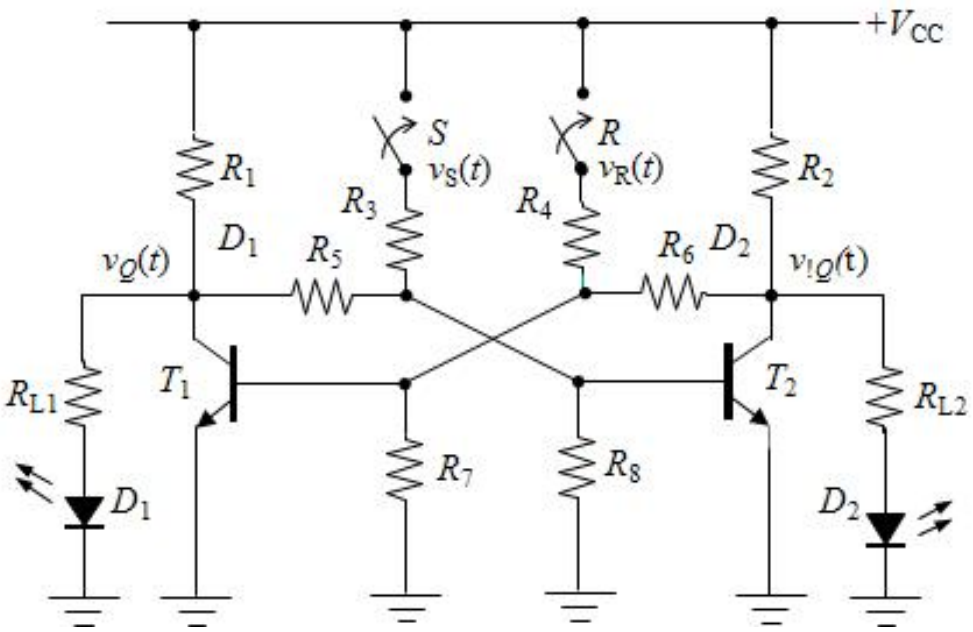


Figure 11.Schematics of the SET/RESET multivibrator implemented by means BJTs.

At start up, assume that T_1 is the first BJT conducting when S = R = OFF. Then, $\boldsymbol{T_2}$ **= OFF** and $i_{C2} = 0$. In this case, $V_{!Q} > V_{D2} = V_\gamma$ and the led D_2 will be turned ON. The current flow at the base of T_1, i_{B1} is then expressed as:

$$i_{B1} = i_{R6} - i_{R7} = \frac{V_{!Q} - V_{BE1\gamma}}{R_2 + R_6} - \frac{V_{BE1\gamma}}{R_7} \tag{20}$$

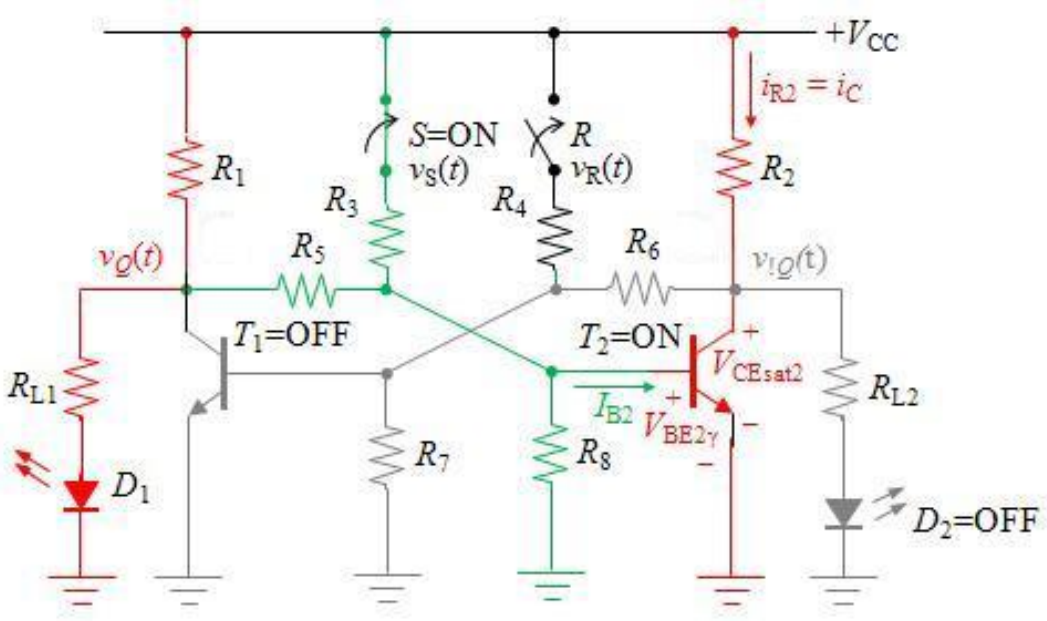
where $V_{!Q}$ can be obtained from the KCL applied at the collector terminal of T_2,

$$i_{R2} = i_{R6} + i_{RL2} \quad \rightarrow \quad \frac{V_{CC} - V_{!Q}}{R_2} = \frac{V_{!Q} - V_{BE1\gamma}}{R_6} + \frac{V_{!Q} - V_\gamma}{R_{L2}} \quad \rightarrow$$

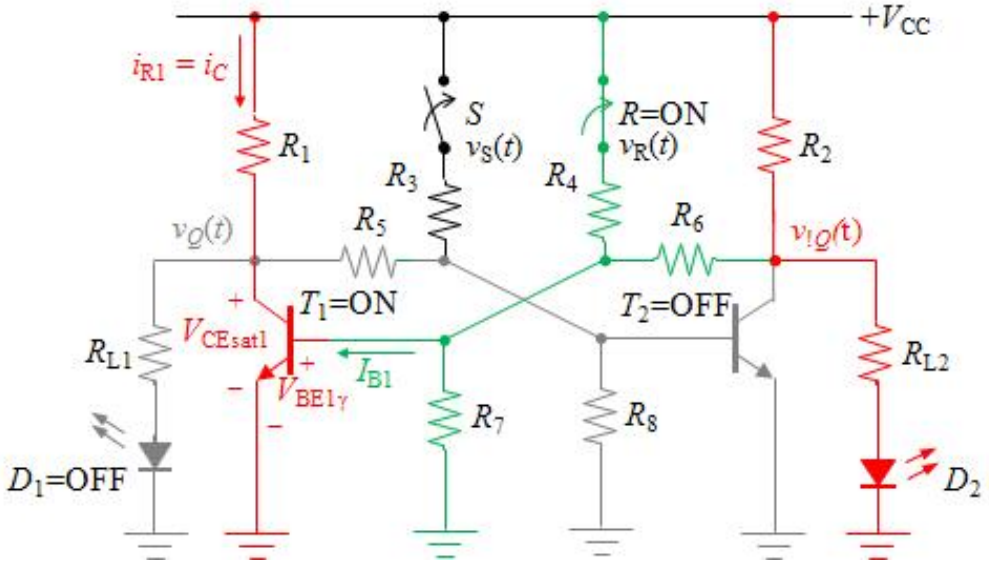
$$\rightarrow \quad V_{!Q} = \frac{V_{CC}R_6R_{L2} + V_{BE1\gamma}R_2R_{L2} + V_\gamma R_2R_6}{R_6R_{L2} + R_2R_{L2} + R_2R_6} \tag{21}$$

Thus, i_{B1} will be large enough to cause the saturation of T_1 (**$\boldsymbol{T_1}$ = ON**) and, therefore, its collector-emitter voltage will decrease drastically ($v_Q = V_{CE1\ (sat)} \approx$ 0.2V). Since this potential is not enough to drive the base of T_2, $v_{BE2} = V_{CE1(sat)}R_8/(R_8 + R_5) < V_{BE2\gamma}$, this transistor will work on cutoff mode. These will be the initial conditions of the circuit, the RESET state (**$\boldsymbol{Q}$ = 0** and !Q = **1**).

- Now, assume that the switch S is activated (S = ON) for a small time period. Then, i_{B2} is momentary fixed by R_3 (green path of Fig. 12a). The value of this variable during this interval is expressed as:



(a)



(b)

Figure 12. Idea del funcionament de la bàscula RS. a) Condició de SET. b) Condició de RESET. El camí marcat en verd indica el camí que causa la la saturació del BJT, mentre que el vermell indica el camí de circulació de corrent per activar els Leds.

$$i_{B2} = \frac{V_{CC} - V_{BE2\gamma}}{R_3 + R_5 // R_8} - \frac{V_{BE2\gamma}}{R_5 // R_8} \qquad (22)$$

and is large enough to cause the saturation of (***T*₂ = ON**). Since $v_{CE2} = V_{CE2(sat)} \approx$ 0.2V, this potential will not only be enough to maintain led D_2 on but will also cutoff T_1 (***T*₁ = OFF**). That is, both transistors change their behavior (SET: ***Q* =1** i **!*Q* = 0**) and now the led that glows is D_1.

The reader can note that this new situation is guaranteed even after the fading of $v_S(t)$ as i_{B2} will be given with an expression similar to (20) but with resistors R_1, R_5 and R_8,

$$i_{B2} = i_{R5} - i_{R8} = \frac{V_Q - V_{BE2\gamma}}{R_1 + R_5} - \frac{V_{BE2\gamma}}{R_8} \qquad (23)$$

when S=R=OFF, so the voltage V_Q is also analogous to (21). In other words, the new outputs are,

$$V_Q = \frac{V_{CC}R_5R_{L1} + V_{BE2\gamma}R_1R_{L1} + V_\gamma R_1R_5}{R_5R_{L1} + R_1R_{L1} + R_1R_5} \;;\quad v_{!Q} = V_{CE2(sat)} \approx 0 \qquad (24)$$

- For returning to the RESET state, the user must activate the switch R (R = ON). Both BJTs will exchange again their operation (***T*****2** = **OFF** and ***T*****1** = **ON**) and ***Q*** = **0**; !Q = **1** (Fig. 12b). The procedure by which T_1 is set to ON is analogous to that just explained above for T_2 and the outputs will be given again by (21).

Task PRELAB 3. Draw the component connections of the SET/RESET multivibrator from Fig. 11 in the Board template provided.

Task LAB 3. Check the correct operation of the SET/RESET multivibrator.

- **1)** Mount the circuit. Use the following components:

  T**1** = ***T*****2** = BC547C**,** ***R*****1** = ***R*****2** = 1k, ***R*****3** = ***R*****4** = 1k2, ***R*****5** = ***R*****6** = 10k, ***R*****7** =***R*****8** =100k, ***R*****LED1** = ***R*****LED2** = 1k8, ***D*****1** = ***D*****2** of threshold voltage: $V\gamma$=1.2V.

- **2)** Connect the power ***V*****CC** = **5V** and check which led is turned on. **3)** Push the RESET button (R) if D_1=ON, or push SET (S) if D_2 = ON). Both leds should change operation mode. **4)** Check that pushing again the same button (R or S depending on the initial case) does not alter the operation of leds. 5) Push the other button to return to the initial case.

  REMARK: Use wires for implementing the push buttons by connecting one end to V_{CC} and emulate the effect of setting $v_S(t)$ and $v_R(t)$ to "1" by connecting momentarily the other end of the wire to R_3 and R_4, respectively.

- Explain a possible utility of the SET/RESET circuit in digital electronics.

Annex 1.- BJT applications operating in the active region

This section considers two typical applications of BJTs operating in the active region. No activities are proposed, since the main goal here is just to show the advantages and the utility of this operating region. The signal amplifier and the current source constitute two of the main general purpose applications of the BJT operating in this mode.

A1.1 Signal amplifier using BJT

One basic application where the BJT is "always" assumed to operate in active mode is called the *voltage amplifier* (or the *signal amplifier*). This electronic system is used very often to improve the power of audio and sensor signals. Strictly speaking, its functionality consists in "**increasing**" the input voltage magnitude in order to provide more power to the output.

The following expression represents the mathematical function corresponding to this operation

$$v_{out}(t) = k v_{in}(t) \tag{1}$$

where $k > 1$ is the *gain factor* of the electronic system, v_{out} is the output and v_{in} the input to be amplified. Figure A1 shows the block diagram corresponding to this operation. The slope of the input/output transfer characteristics $v_{out} - v_{in}$ (Fig. A2) gives an idea of the gain that is obtained at the output.

One way of implementing the amplifier by means of a BJT consists in changing the source v_{in} in Fig. 3 by the same signal source $v_{in}(t)$ and modifying R_B to so as to operate in the active region. Unfortunately, the *npn* BJT can only operate in active mode when $v_{in} > V_{BE\gamma}$, so the circuit admits only positive values of v_{in}. This problem can be solved adding a DC voltage in series with v_{in} so that an offset voltage level and all values from the input v_{in} can be positive, but this would increase the implementation cost of the amplifier because another DC power supply (or battery) is required.

The BJT amplifier in Fig. 3 develops its functionality and circumvents the offset problem using one single DC voltage source. This basic amplifier is know as the *Common Emitter* (CE) amplifier. In order to design its components, the analytical process consists of the following three steps:

A. *Offset estimation* (V_{OUT}) (or transistor ***biasing***):

The output offset is estimated by just considering the **DC voltage supply** (V_{CC}) **and disconnecting the remaining independent sources** (the AC input, $v_{in}(t) = 0$, in this case). If capacitors exists they are considered as open circuits because when $s = 0$, their impedance becomes infinite ($Z_C(s) \rightarrow \infty$). In fact, the goal of C_1 is to permit the biasing of the BJT through resistor R_2 and connect the AC input source to the base junction so that the input signal can be amplified.

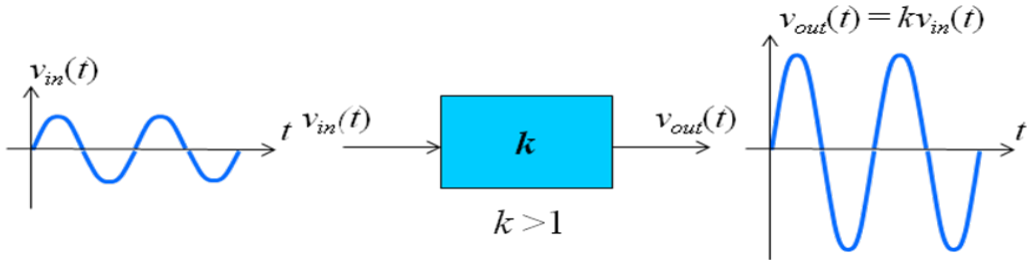


Figure A1. Block diagram of the BJT voltage amplifier. The input magnitude v_{in} is increased by a factor k at the output v_{out}.

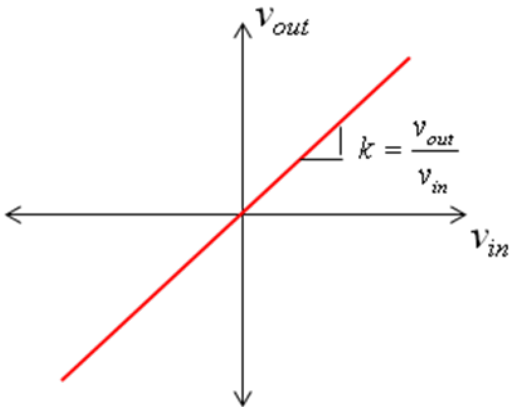


Figura A2. Input/output transfer characteristics: $v_{out} - v_{in}$ of the voltage amplifier

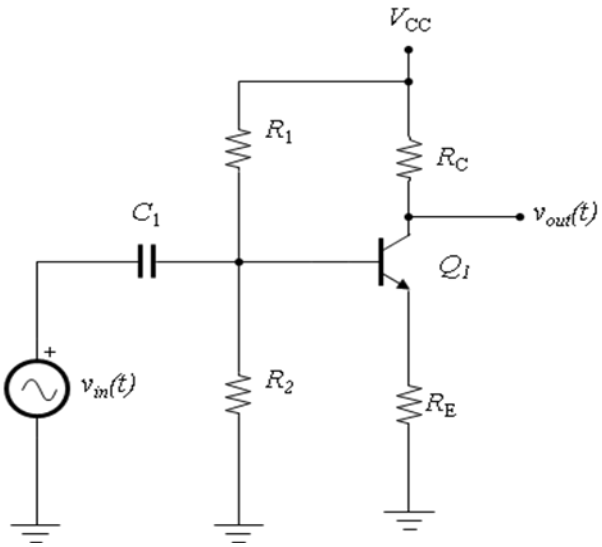
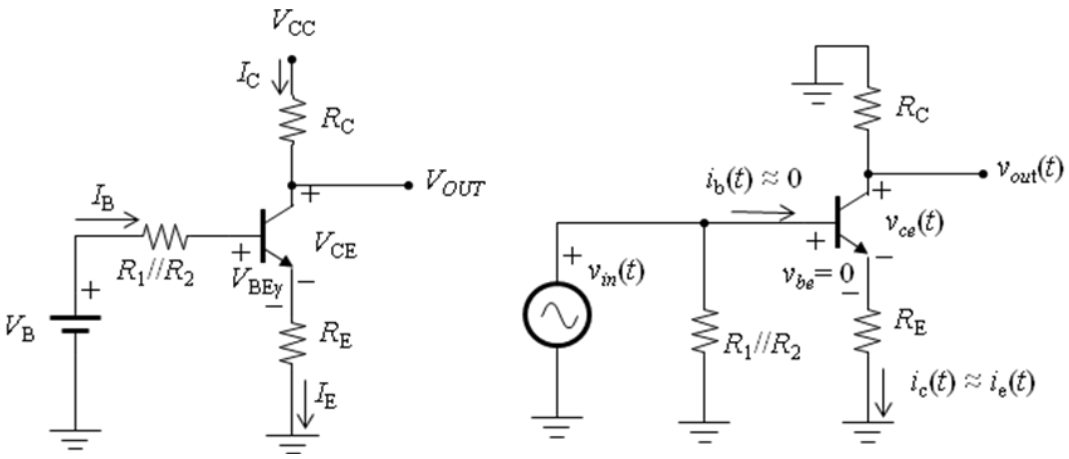


Figure A3 Common Emitter voltage amplifier using BJT.

When only the DC source is considered the circuit can be simplified to that of Fig. 4a (just use the Thevenin equivalent observed at the base terminal). Assume that the BJT is operating in the active region. The current I_B is obtain by means of the KVL expression,

$$V_B - \left(R_1 // R_2\right) I_B - V_{BE\gamma} - R_E I_E = 0. \qquad (2)$$



(a) (b)

Figure A4. Analytical diagrams of the BJT voltage amplifier. a) DC analysis. b) AC analysis

where $V_B = R_2 V_{CC}/(R_1 + R2)$. Since $I_E = I_B + I_C = I_B(h_{FE} + 1)$, equating I_B leads to:

$$I_B = \frac{V_{CC}\left(R_2/\left(R_1+R_2\right)\right) - V_{BE\gamma}}{R_1//R_2 + R_E\left(h_{FE}+1\right)} \tag{3}$$

where the term $R_E(h_{FE} +1)$ the ***input resistance*** ($R_{in(BJT)}$) the BJT has in this circuit. If we design the resistors so as to obtain $R_{in(BJT)} >> R_1//R_2$ (10 times: $R_{in(BJT)} \approx 10\ R_1//R_2$), then I_C can be approximated and estimated as

$$I_C = h_{FE} I_B \approx \frac{V_B - V_{BE\gamma}}{R_E}. \tag{4}$$

In other words, the base DC voltage V_B and the resistor R_E controls the amount of electric DC current flow in the the collector terminal I_C . With this approximation, the base current can be underestimated ($I_B \approx 0$) and the output offset V_{OUT} is expressed as

$$V_{OUT} = V_{CC} - R_C I_C = V_{CC} - R_C \frac{V_B - V_{BE\gamma}}{R_E} \tag{5}$$

B. *Voltage gain estimation* (***k***):

The gain factor is obtained by considering just **the AC sources (AC) from the circuit and setting the DC supply to zero** ($V_{CC} = 0$). In this case, electrolytic capacitors are considered short-circuits at relatively higher frequencies ($s = j\omega = j2\pi f$ where $f > 1$kHz) an their impedances can be underestimated, $|\boldsymbol{Z_C(s)}| \rightarrow \mathbf{0}$. The capacitor C_1 will then connect the AC source to the base junction of the BJT and the input AC resistance of the amplifier, R_{in} becomes

$$R_{in} = R_1//R_2//R_{in(BJT)} = R_1//R_2//R_E\left(h_{FE}+1\right) \tag{6}$$

Since, $v_b(t) = v_{in}(t)$ and the base-emitter junction can be considered a biased diode during the full input range, the swing of the base-emitter voltage will be negligible $v_{be}(t) = 0$, so in practical terms it can be assumed that the input voltage falls on $v_{RE}(t)$.

For this reason, the collector current $i_c(t)$ is obtained as

$$i_c(t) = \frac{v_{RE}(t)}{R_E} = \frac{v_{in}(t)}{R_E} \tag{7}$$

and the output AC voltage expression, $v_o(t) = -v_{RC}(t) = -R_C i_c(t)$ is obtained as:

$$v_{out}(t) = -R_C \frac{v_{in}(t)}{R_E} \tag{8}$$

Thus, the **voltage gain** (***k***) of the circuit is

$$\boxed{k = \frac{v_{out}(t)}{v_{in}(t)} = -\frac{R_C}{R_E}} \tag{9}$$

Finally, we can use (5) and (9) to obtain the full DC and AC output, $v_{OUT}(t)$, by means of the *superposition principle*

$$\boxed{v_{OUT}(t) = V_{OUT} + v_{out}(t) = V_{CC} - \frac{R_C}{R_E}\left(V_B - V_{BE\gamma} + v_{in}(t)\right)} \tag{10}$$

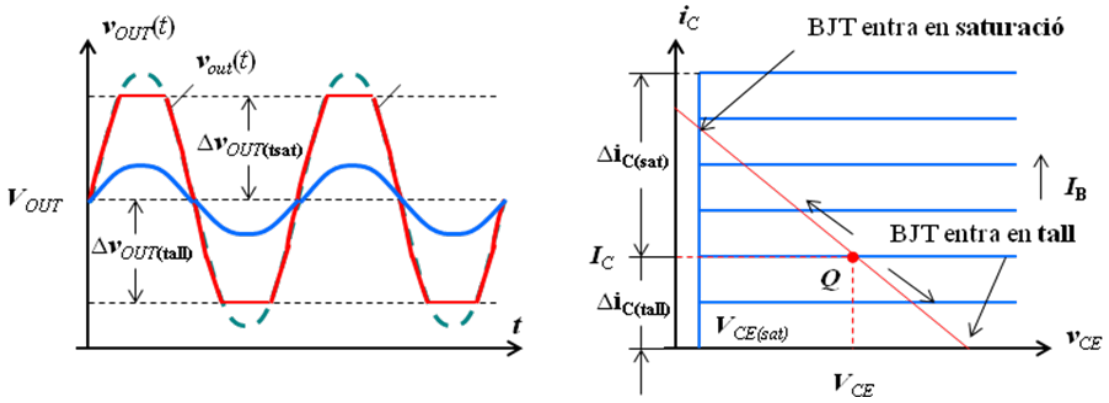
C. *Estimation of the output swing* ($\Delta \boldsymbol{v_{out}}$):

We define as the *output swing* to the limitation in **dynamic range Δv_{out} existing at the output of the voltage** amplifier when the BJT leaves the active region, and which is normally expressed in terms of the maximum peak value that can be obtained at the output without causing signal distortion.

Theoretically, the input $v_{in}(t)$ there is no limit for both the input and output amplitude. In practice, however, this assumption is not true because the BJT could leave the active region. When this happens, the result at the output is a pulsating signal of considerable distortion in relation to that of the input.

Figure A5 illustrates the root of this problem. At $v_{in}(t) = 0$, the zero reference at the output is fixed by the BJT operating point $Q = \{I_C, V_{CE}\}$. When the input varies, this point moves along a straight line which depends on the design of resistors R_C and R_E. To this line we refer to as the *load line*.

The expression representing this line can be determined if both DC and AC analysis are overlapped when obtaining the collector-emitter voltage. On one hand, the contribution of input variations to this variable (Fig. A4b) is obtained by the KVL,



(a) (b)

Figure A5. Output swing.. a) Full output voltage $v_{OUT}(t)$ for two different inputs. b) Operating point moving along the load line when an AC input $v_{in}(t)$ is present. The output $v_{OUT}(t)$ contains an offset (V_{OUT}). A significant input magnitude v_{IN} may cut the output peak (discontinuous trace).

$$v_{ce} + \left(R_C + R_E\right) i_c = 0 . \tag{11}$$

As such, the AC version of the collector current i_c is

$$\Delta i_c = \frac{\Delta v_{ce}}{R_C + R_E} . \tag{12}$$

where the symbol Δ denotes the variations of i_C and v_{CE} respectively.

The dynamic range of v_{OUT} then is determined by specifying the voltage v_{CE} at both ends of the load line (Fig. A5b), one corresponding to the *saturation* boundary, and the other corresponding to the *cutoff* boundary. Since the saturation limit is $v_{CE} = V_{CE(sat)}$, the maximum possible output range in half input cycle, $\Delta v_{CE} = V_{CE} - V_{CE(sat)}$, is

$$\Delta v_{OUT\,(sat)} = \left| R_C \Delta i_{C(sat)} \right| = \frac{R_C}{R_C + R_E} \left(V_{CE} - V_{CE(sat)} \right) \tag{13}$$

The limit at the other half input cycle is set by the cutoff boundary as

$$\Delta v_{OUT\,(tall)} = \left| R_C \Delta i_{C(tall)} \right| = R_C I_C \tag{14}$$

Finally, the full output swing without signal distortion is represented by the minimum of both these two values:

$$\Delta v_{OUT} = \min \left\{ \Delta v_{OUT\,(tall)}, \Delta v_{OUTsat)} \right\} \tag{15}$$

In practice, the output is connected to other electronic systems and loads. As such, the DC component may be altered considerably if the collector terminal is not isolated (see expression 10), and the voltage amplifier may change its behavior.

One way of isolating the DC component from the AC swing is by introducing a capacitor C_L between the collector terminal and the input terminal of the subsequent system. The situation of Fig. A6 is more realistic in this sense, since the resistor R_L represents the load connection of another system whose input is meant to be provided by the voltage amplifier.

Using a capacitor C_L does not affect the bias point of the amplifier but in AC domain resistor R_C is connected in parallel with R_L. As such, expressions (9), (13) and (14) must be modified, so the new *gain factor* (***k***) and dynamic range $\Delta \boldsymbol{v_{out}}$ become:

$$k' = \frac{v_{out}(t)}{v_{in}(t)} = -\frac{R_C // R_L}{R_E} \tag{16}$$

$$\Delta v_{OUT(sat)} = \frac{(R_C // R_L)(V_{CE} - V_{CE(sat)})}{R_C // R_L + R_E} \tag{18}$$

$$\Delta v_{OUT(tall)} = (R_C // R_L) I_C \tag{19}$$

Rewriting (16) as:

$$\frac{v_{out}(t)}{v_{in}(t)} = -\frac{R_C}{R_E}\frac{R_L}{R_C + R_L} = k\frac{R_L}{R_{out} + R_L} \tag{20}$$

allows a new and more general model of the voltage amplifier to be inferred (Fig. A7). This new schematic represents its AC behavior but using fewer elements. In here, $R_{out} = R_C$ corresponds to the **output resistance** and is considered a way of representing the loss of (k) obtained at the output. The same consideration can be taken when evaluating the losses of the **input resistance** $\boldsymbol{R_{in}}$ due to the output characteristics of $v_{in}(t)$.

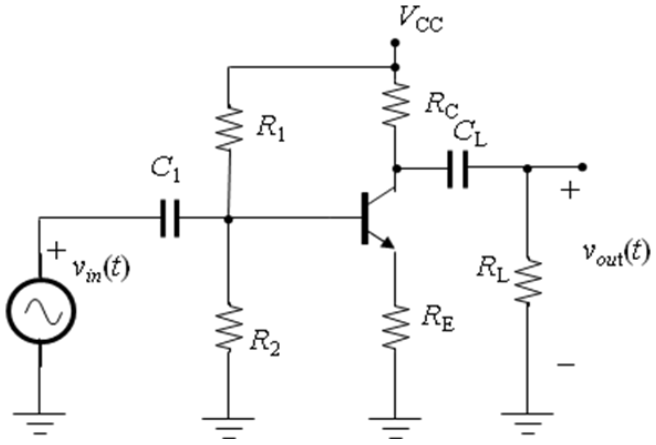


Figure A6. Voltage amplifier using capacitor DC coupling both at the circuit input and output.

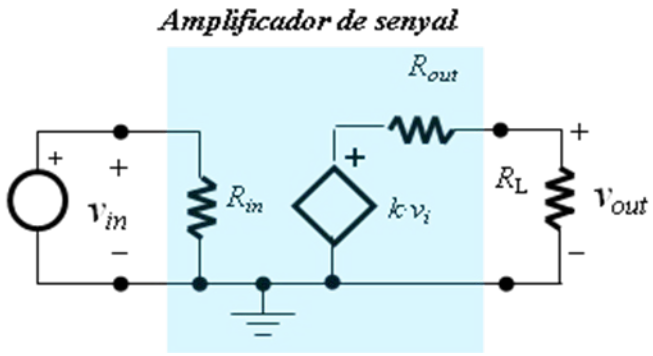


Figure A7. General overview of the AC behavior of the voltage amplifier. A voltage amplifier can be thought of as "controlled voltage source" with factor k and depending on v_{in}. The input and output resistance, R_{in} and R_{out} establish the amount within the amplification stage when the main body is connected to other stages that build up a much more complex electronic system.

A1.2 Electric DC current sources

Although, circuits are generally powered by DC voltage supplies, the role of *electric current sources* becomes essential in several electronic systems. Circuits implementing integrators, ramp or saw-tooth generators, are some application examples that very often need of this resource to develop its function.

The most simple and intuitive way of implementing a current source is depicted in Figure A8. In this circuit, whenever the resistor R_L is quite small in relation to R ($R >> R_L$) the output current will be quite constant and approximately:

$$I = v_I/R \tag{21}$$

Unfortunately, this circuit requires of large values of v_I when operating at significant output current values. Another drawback lies on the fact that the current value cannot be easily programmed (i.e. by means of a potentiometer) within a certain range.

The solution to this problems lies on the use of active components with the ability of setting (or controlling) the electric current at the desired nodes of the circuit, such as the bipolar transistor BJT. In the circuit of Fig. A9, if the input is set such that the condition $V_I > V_{BE\gamma}$ holds, the emitter voltage is expressed as:

$$V_E = V_I - V_{BE\gamma} \tag{22}$$

The emitter current then becomes,

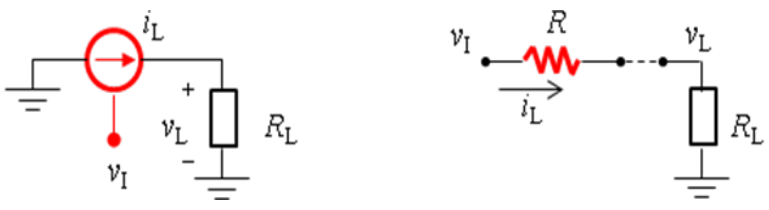
$$I_E = V_E/R_E = (V_I - V_{BE\gamma})/R_E, \tag{23}$$

But, since $I_C \approx I_E$ for large h_{FE} we obtain:

$$I_C \approx (V_I - V_{BE\gamma})/R_E \tag{24}$$

The reader can observe that the value I_C is constant despite of the variation at V_C due to R_L (provided that the BJT does not leave the active region: $V_C > V_E + V_{CE(sat)}$).

The base voltage V_I can be provided in many ways. The voltage divider (Fig. A10a) will suffice whenever the base resistors do not load the base terminal of the BJT (and thus altering its operation). This condition is guaranteed as long as the equivalent resistance (seen from the base terminal) is much lower in relation to the factor $R_E(h_{FE}+1)$. A more practical, solution consists in using a biasing zener diode (Fig. 10b), or a series of rectifier diodes (Fig. 10c). In this last case, using a *pnp* transistors alllows the circuit to operate with output loads referred to ground.



(a) (b)

Figure A8. Electric current source.. a) Symbol and Electric diagram. b) Voltage divider implementation.

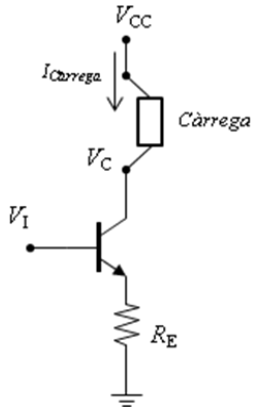
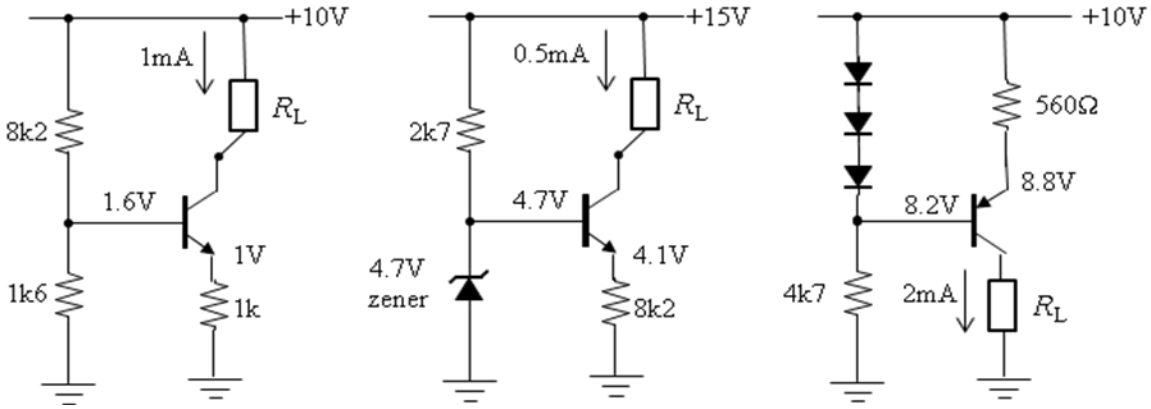


Figure A9. BJT-based current source. Operation principle



(a) (b) (c)

Figura A10. Three different ways of biasing a BJT for developing a DC current source. a) Voltage divider. b) Zener implementation. c) *pnp* tBJT and output referred to ground.

Annex 2 – Results form PRELAB

REMARK: You **MUST** do these activities **BEFORE THE LAB SESSION CORRESPONDING TO PRT4**

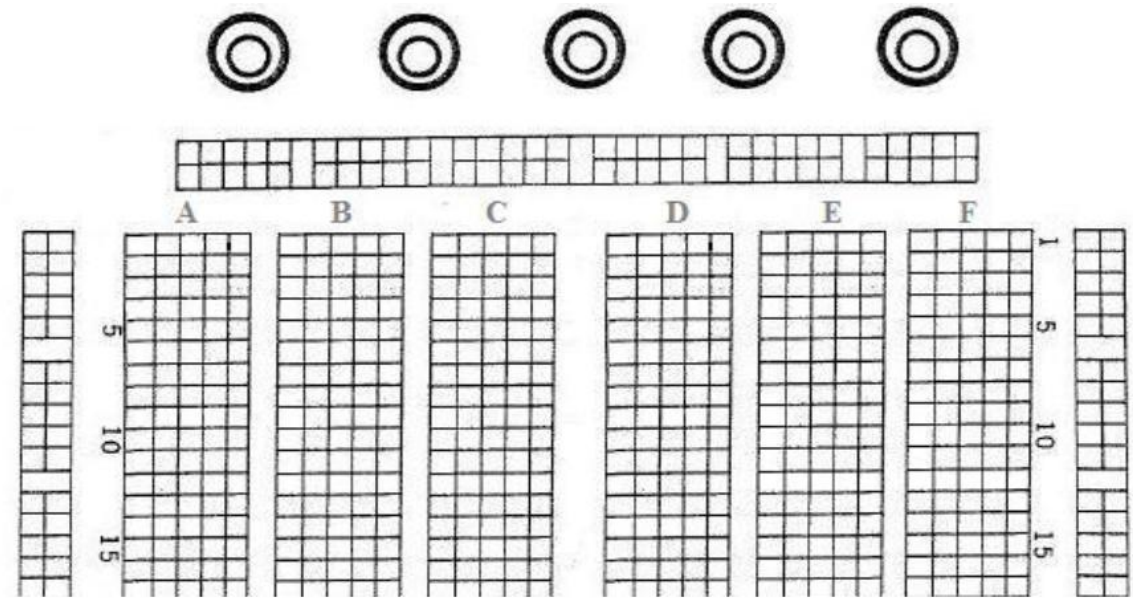
UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH Escola Politècnica Superior d'Enginyeria de Vilanova i la Geltrú	EEL
Electronic Systems (SIEK) **Activity 4:** Switching Electronics: The Bipolar transistor (BJT) **PRELAB**	
Students:	**Date:**

PRELAB 0: Draw the contour package of the bipolar transistor BC547C and identify the pins corresponding to *collector*, b*ase* and e*mitter* terminals, respectively

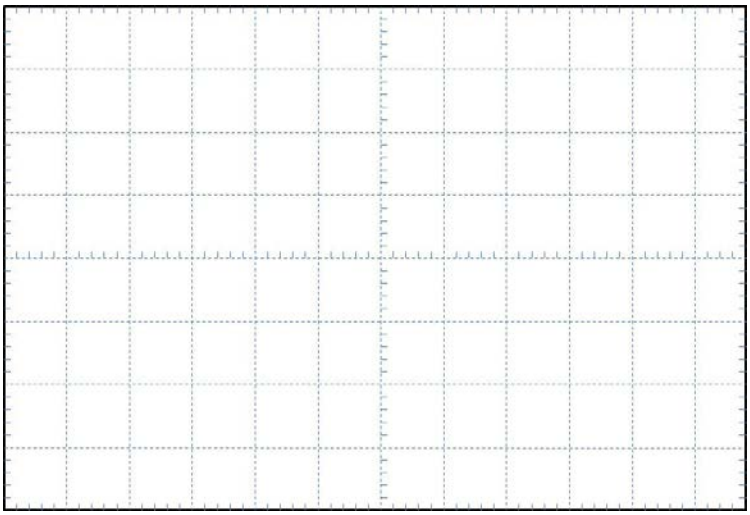
BJT specification	***Value indicated by the manufacturer***	***Considerations:*** Comment the measure conditions used by the manufacturer to specify this parameter (test, operating conditions)
h_{FE}		
$V_{BE\gamma}$		
V_{CEsat}		

Taula A2.1 Specify the information related to the BC547C found in the datasheet.

PRELAB 1. The logic inverter (The NOT gate) using BJT.



Represent the waveforms you expect to see of $v_B(t)$ and $v_{CE}(t)$



CH1 VOLT/:

Zero POS:

CH2 VOLT/:

Zero POS:

TIME/:

Acob:

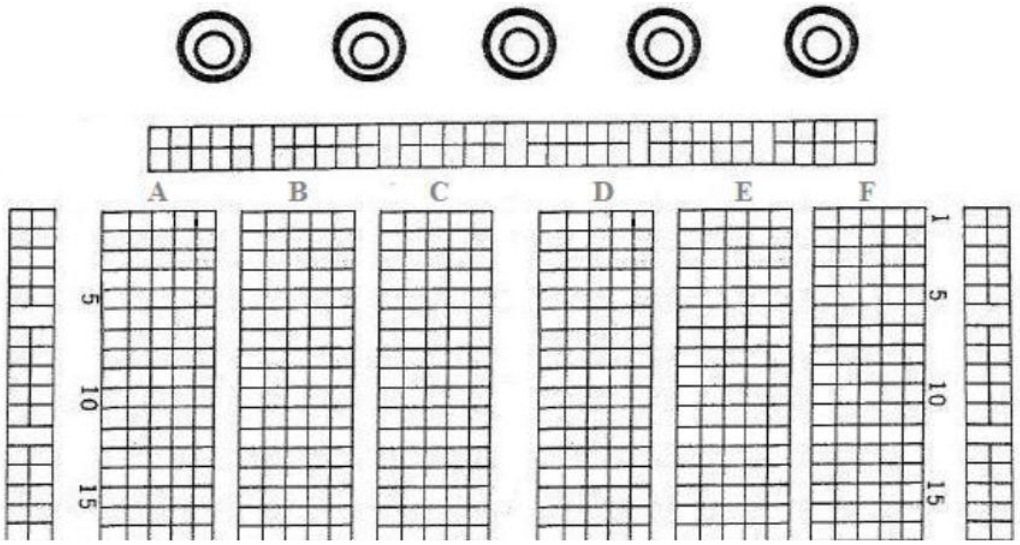
PRELAB 2: Electronic switch with 7-segment BCD Display.

Draw the internal connections of the integrated circuit 9A102G and LSD5355

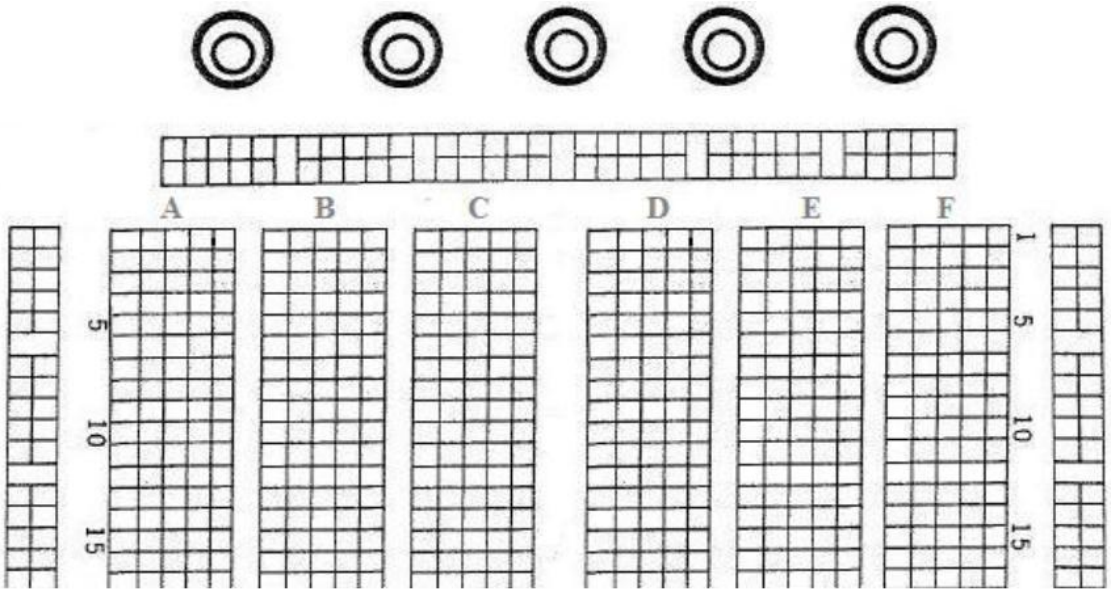
Specify the meaning of the reference 9A102G:

Specify common terminal at the 9A102G IC:_____

Configuration used in the 7-segment BCD display:_____



PRELAB 3 (Opcional). SET/RESET multivibrator



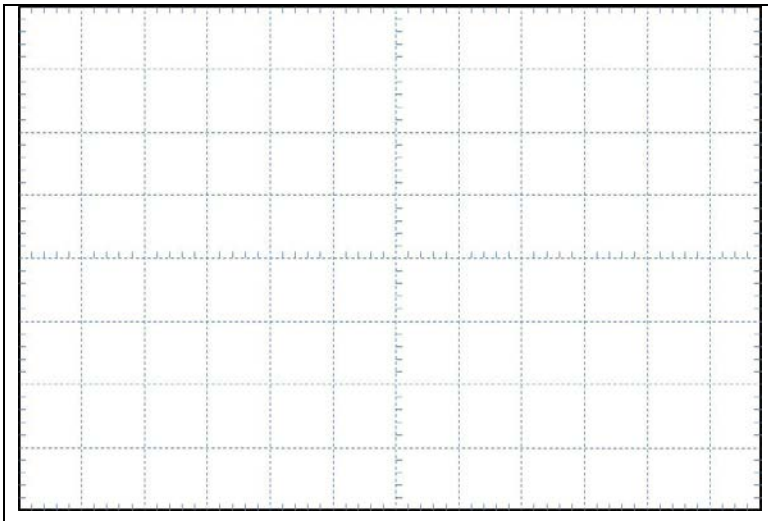
Annex 3 –Lab activities

REMARK: You **MUST PRINT OUT** this form and TAKE IT **WITH YOU** the day of the lab session

UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH Escola Politècnica Superior d'Enginyeria de Vilanova i la Geltrú	EEL
Electronic Systems (SIEK) **Activity 4:** Switching Electronics: The Bipolar Transistor (BJT) **RESULTS FORM**	
Students:	**Date:**

LAB 1. The inverter logic (NOT Gate) using BJT.

Represent the waveforms of $v_B(t)$ and $v_{CE}(t)$ from the oscilloscope



CH1 VOLT/:

Zero POS:

CH2 VOLT/:

Zero POS:

TIME/:

Acob:

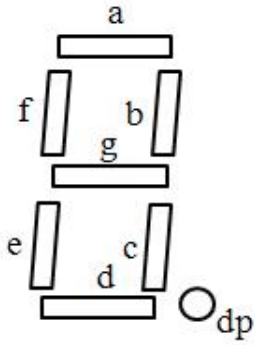
Specify the values of v_B and v_{CE} both at cutoff and saturation regions

$V_{B\ (cutoff)}$: _____ $V_{B(saturation)}$: _____

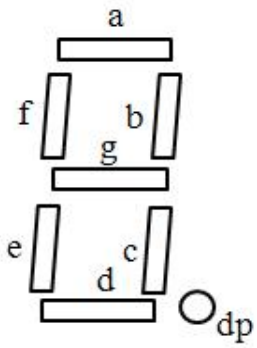
$V_{CE\ (cutoff)}$: _____ $V_{CE(saturation)}$: _____

LAB 2. Electronic switch with 7-segment BCD display

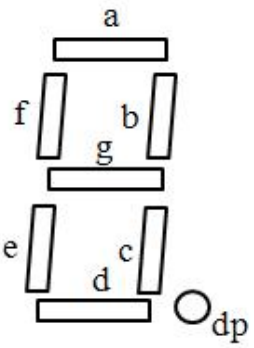
- Display visualization with ***S*** = ***B*** and S_1=...=S_8 = **ON**[4]



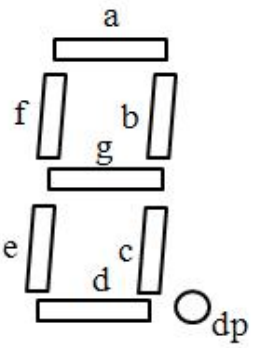
- Visualization with ***S*** = ***B*** and three random examples



1)



2)



3)

Exemple	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
1								
2								
3								

Table A3.1 Specify switch positions in each example. Use ON and OFF to specify whether the switches are OPEN or CLOSED, respectively.

[4] Mark the segments you believe will glow after setting the specified configuration.

- Specify the waveform generator configuration for observing the number "8" (decimal point included) with a blinking pattern of ONE SECOND.

  - ***SORTIDA:*** ☐ *TTL* ☐ 50Ω.
  - ***FUNCIÓ:*** ☐ ***Defecte*** ☐ *SQUARE* ☐ *SINUS* ☐ *TRIANGULAR*
  - ***OFFSET:*** ☐ Defecte ☐ Valor: _____
  - ***AMPLITUD:*** ☐ Defecte ☐ Valor: _____
  - ***FREQÜÈNCIA:*** _____

LAB 3 (Optional). SET/RESET multivibrator

Explain the behavior observed in the SET/RESET multivibrator and specify some use of this circuit in digital electronics:

Lab Activity 5. Analog electronics: The *Operational Amplifier* (OPAMP)

Main Goal: Knowing the operation principle of the operational amplifier and to understand its utility in analog electronic applications, such as audio amplifiers and signal synthetization systems.

1 Introduction

The *operational amplifier* (OPAMP) is a **voltage amplifier** with "extremely" high gain. For example, the popular 741 has a typical gain k = 200,000, whereas the gain of more expensive integrated circuits with advanced features, such as the reference OP-77 is k = 12,000,000. Due to such high values, the gain is often expressed in V/mV (or V/μV) and *decibels*. In the later case, the scale transformation used is

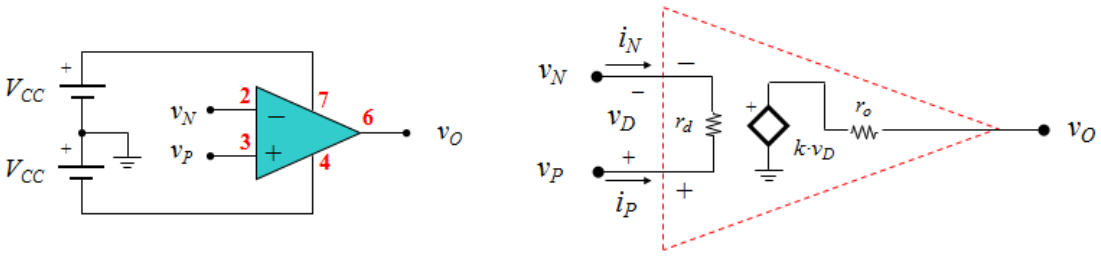
$$k\big|_{dB} = 20\log_{10}(k). \tag{1}$$

Thus, the OP-77 has a voltage gain of 12V/μV, which is also equivalent to 141.6 dBs.

Figure 1 shows the symbol of the OPAMP and the DC power-supply connection to make it work (though most of the times the power-supply is not represented in the diagram in order to minimize schematic cluttering). The inputs, identified by the "-" and "+" symbols are designated *inverting* and *non-inverting*, respectively. Their voltages with respect to ground are denoted v_N and v_P, and the output voltage as v_O. The arrowhead form pointing to the right specifies the signal transmission direction from the input to the output. Figure 1b shows the equivalent circuit of a properly powered OPAMP. Though the integrated circuit itself does not have ground pin, the ground symbol represents the common point of the symmetric power supply of Fig. 1a. The model includes a voltage source controlled by v_D, of gain factor $\boldsymbol{k}$, the differential input resistance $\boldsymbol{r_d}$ and the output resistance $\boldsymbol{r_o}$, respectively.

Figure 2 shows the input-output transfer characteristics (v_O-v_D) of this component. Taking into account that $v_D = v_P - v_N$ corresponds to the *differential input* voltage, this electronic device is mathematically modelled as

$$v_O = \begin{cases} V_{OH} & , \text{for } v_D > \dfrac{V_{OH}}{k} \\ kv_D & , \text{for } \dfrac{V_{OL}}{k} \le v_D \le \dfrac{V_{OH}}{k} \\ V_{OL} & , \text{for } v_D < \dfrac{V_{OL}}{k} \end{cases}. \tag{2}$$



(a) (b)

Figure 1. The OPAMP: a) Symbol and power connection; b) Internal mathematical model. This integrated circuit operates as a voltage amplifier. The values in red indicate component pin for the reference LM741, which is most used in 8-pin integrated circuits.

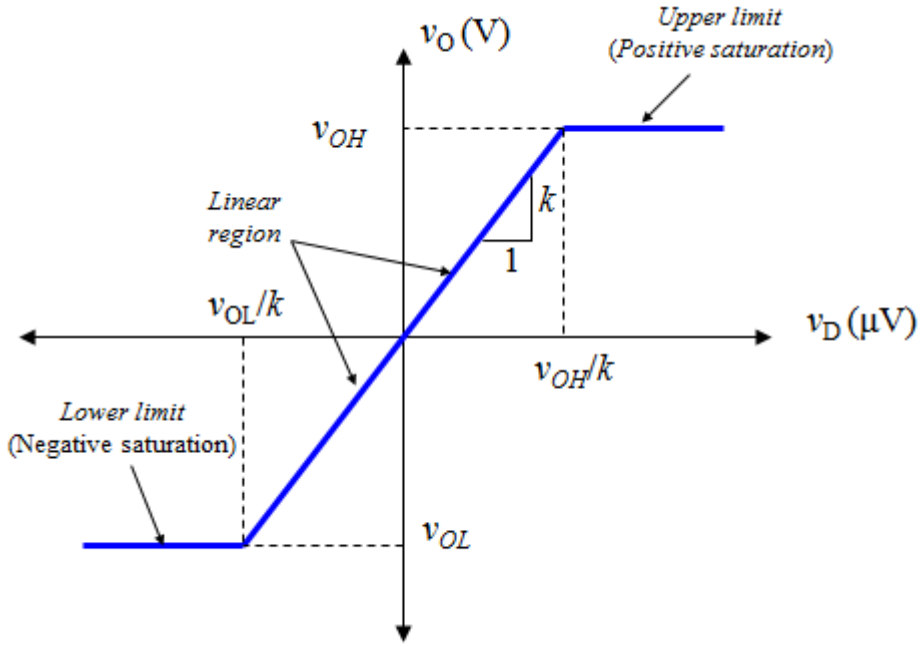


Figure 2. The OPAMP transfer characteristics $v_O - v_D$. The horizontal axis has been extended (μV scale) in order to show the linear region in more detail.

The supply voltages set the upper and lower limits, and the output swing of the amplifier $V_{OL} < v_O < V_{OH}$: $V_{OH} = v_{(7)} - V_{Drop\text{-}out}$ i $V_{OL} = v_{(4)} + V_{Drop\text{-}out}$; with $v_{(7)}$ being the positive supply and $v_{(4)}$ the negative one. The voltage drop information can be obtained from the manufacturer's datasheet, and for the 741 this value is about $\boldsymbol{V_{Drop\text{-}out} = 2V}$.

Since the 741 is powered with $\boldsymbol{v_{(7)} = -v_{(4)} = V_{CC} = 15V}$ and the output range is $\boldsymbol{\Delta v_O = \pm 13V}$, the input voltage is bound to be very small ($\boldsymbol{\Delta v_D = \Delta v_O / k = \pm 65\mu V}$). For For instance, to sustain v_O = 6V and unloaded 741 requires v_D = 6/200,000 = 30μV.

By connecting external components around an OPAMP, we obtain what we shall henceforth refer to as an *OPAMP circuit*. Understanding the difference between an OPAMP circuit and the OPAMP itself containing all the circuitry for developing its function is crucial. One example is the *noninverting amplifier.*

Task PRELAB0. Identify the new components you are going to use in this lab activity: the power transistors and the OPAMP.

- Search the important information regarding the **LM741** (or UA741) integrated circuit, the power BJTs: the **BD243** and **BD244**; Find the manufacturer's datasheet of each device and represent their contour package in the box provided. Indicate pin name and distribution.
- Read the electrical characteristics from the OPAMP and specify open-loop voltage gain (k) drop-out and maximum power supply.

2. The *noninverting* amplifier

The circuit of Fig. 3a consists of an OPAMP and two external resistors: R_1 and R_2. To understand its function, finding the relation between v_{OUT} and v_{IN} is necessary. To this end, the circuit is redrawn as in Fig. 1b, where the OPAMP has been replaced by its equivalent model (Fig. 1a), the internal resistors have been removed ($r_D \rightarrow \infty$ and $r_o \rightarrow 0$) and the resistive network has been rearranged strategically to emphasize its role in the circuit (Fig. 3b).

v_{OUT} can be found by means of (2) but expressions for v_P and v_N must be obtained previously. By inspection, it holds that

$$v_P = v_{IN} . \tag{3}$$

On the other hand, using the voltage divider at the output yields

$$v_N = \frac{R_1}{R_1 + R_2} v_{OUT} . \tag{3}$$

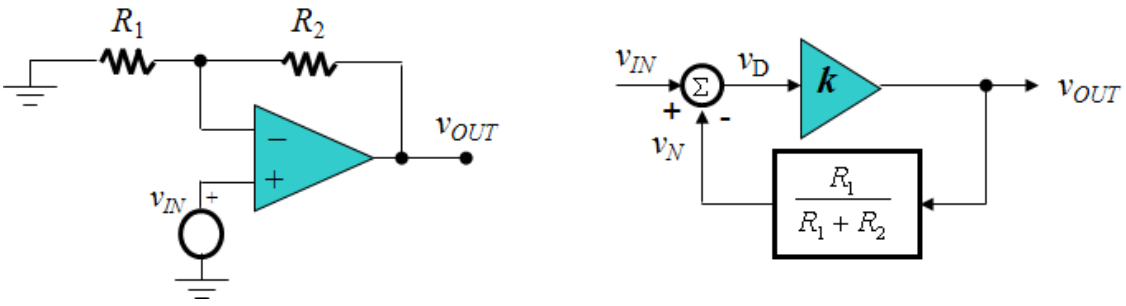
In fact, the voltage v_N represents the fraction (or "sample") of v_{OUT} that is being fed back to the inverting input in order to be compared with the system input. So the system error, characterized by v_ε is

$$v_\varepsilon = v_D = v_P - v_N = v_{IN} - \frac{R_1}{R_1 + R_2} v_{OUT} . \tag{4}$$

Using the relation (2), $v_{OUT} = k v_D$ allows the output to be expressed as,

$$v_O = k \left(v_{IN} - \frac{R_1}{R_1 + R_2} v_{OUT} \right) . \tag{5}$$

Collecting terms and solving the ratio v_{OUT} / v_{IN} leads to,



(a) (b)

Figure 3. The noninverting voltage amplifier. a) Schematics; b) Block diagram of the noninverting configuration aimed at correcting the error signal $v_D = v_{IN} - v_N$ so ther the input can track the sample $v_P = v_{OUT}R_1/(R_1+R_2)$.

$$\frac{v_{OUT}}{v_{IN}} = k' = \frac{A}{1+A\beta} = \frac{k}{1+k\dfrac{R_1}{R_1+R_2}} \tag{6}$$

Where we shall designate $k = A$ and $\beta = R_1 / (R_1 + R_2)$. This result reveals that the circuit of Fig. 3 consisting of an OPAMP and a resistor pair is itself another voltage amplifier with different gain. This is not surprising, as the two amplifiers, while sharing the same output $v_{OUT,}$ have different inputs, namely v_D in the case of the OPAMP and v_{IN} for the circuit. To understand this difference, k is referred to as the *open-loop gain*, and k' as the *closed-loop gain*.

- *The ideal OPAMP*

Considering the simplicity of the analysis corresponding to the the noniverting configuration, and its ideal closed-loop results, we wonder whether there is not a simpler technique to derive similar results in other more complex OPAMP circuits, bypassing most of the tedious algebra.

Such a technique exists and is based on the fact that when the OPAMP is operated with negative feedback, in the limit $k \to \infty$ its input voltage approaches zero ($v_D = v_{OUT} / \infty = 0$). As such, since $v_D = v_P - v_N$ in the limit it holds that,

$$\lim_{k\to\infty} v_N = v_P \,. \tag{7}$$

This property, referred to as the *input constraint* makes the input terminals seem as if they were shorted together, though they are not. Additionally, an ideal OPAMP draws no current at its input terminals "+" "- since its differential input resistance is also very large. In other words for voltage purposes the input port seems to be shorted, but for current purposes it seems to be open. Hence the popular designation "virtual short".

Definition 1: *When operated with negative feedback, the ideal operational amplifier will output whatever voltage and electric current* $\{v_{OUT}, i_{OUT}\}$ *it takes to drive* $v_D = 0$ (*or equivalently to force* v_N *to track* v_P) *but without drawing any current at either input terminal* ($i_N = i_P = 0$).

From Fig. 1b it can be seen that is the voltage v_N which tracks v_P and not the other way round. Otherwise, the OPAMP would be unable to control the system and (7) will never hold. Thus, the OPAMP controls v_N via the external feedback network and the output is always within the linear región of Fig. 2, so ideally the voltage gain of the circuit is

$$\frac{v_{OUT}}{v_{IN}} = k'_{ideal} = \lim_{A\to\infty} \frac{A}{1+A\beta} \approx \frac{1}{\beta} = 1+\frac{R_2}{R_1} \tag{8}$$

To understand better the functionality of the OPAMP, consider the electric diagram of Fig. 4, where, by inspection, we have $\boldsymbol{v_P = v_N = v_{IN}(t)}$. Since the operational drives v_{OUT} to whatever $v_N = v_P$ it takes to cause $i_N = i_P = 0$, it holds that $\boldsymbol{i_{R1} = i_{R2}}$,

$$\frac{0 - v_{IN}(t)}{R1} = \frac{v_{IN}(t) - v_{OUT}(t)}{R_2}. \tag{9}$$

Equating (9) in order top find the ratio $v_{OUT}(t)/v_{IN}(t)$ leads to the gain factor,

$$\frac{v_{OUT}}{v_{IN}} = 1+\frac{R_2}{R_1} \tag{10}$$

which is equivalent to that of (8). In general, when operated with negative feedback the OPAMP obtains the output fraction trough the path connected from the output to v_N (from v_{OUT} to v_N, and from v_N to ground). On the other, with *positive feedback* (path towards v_P instead of v_N), or *no feedback* at all, the OPAMP act as a **voltage comparator**: *positive saturation* (V_{OH} when $v_P > v_N$) or *negative saturation* (V_{OL} when $v_P < v_N$;).

3. Current driver

Obviously, there are a wide range of applications with th OPAMP using negative feedback. The idea that the output value can be set regardless of the load connected to it makes the OPAMP a good candidate for developing complex electronic systems with multi-stage connection (one stage connected after the other). In Annex 1, the reader can find a summary of applications using a single or several OPAMPS.

In practice, however, the definition of the ideal OPAMP is only valid within the limitations specified by the manufacturer and, consequently, they may be taken into account in design purposes. For instance, one may be tempted to connect a **8Ω**-speaker at the output, and use the noninverting configuration as an audio amplifier. However, if $\boldsymbol{V_{OUT}}$ **= 10V** the OPAMP must be able to draw **1.25A**, far too much in relation to the maximum **10mA** of the 741.

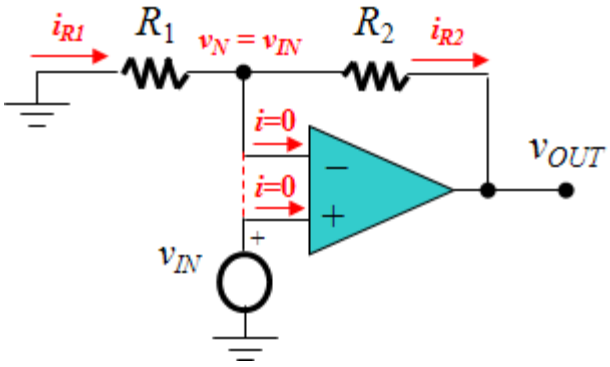


Figure 4. Use of the ideal OPAMP definition for estimating the circuit function.

In these situations where a higher current capacity is required, the solution is to place a *current driver*[1] between both elements (Fig. 5a). A driver current is an amplifier of voltage gain $\boldsymbol{K_V = v_{OUT}/v_{IN} \approx 1}$, but with great current sourcing capabilities ($\boldsymbol{i_{OUT} >> i_{IN}}$).

Fig. 5b, shows a possible implementation of this operation. It consists of a complementary pair of transistors (*npn* and *pnp*) connected in such a way that both cannot be activated simultaneously. When the input is within the range $\boldsymbol{-V_{EB\gamma} \leq v_{IN} \leq V_{BE\gamma}}$, both transistors are cut-off, since the potential is not enough to turn the base-emitter junction on, and the output $\boldsymbol{v_{OUT}}$ will be zero. As $\boldsymbol{v_{IN} \geq V_{BE\gamma}}$, Q_N enters the active area and operates as an emitter follower. As such, the output is connected to the input via the base-emitter junction and,

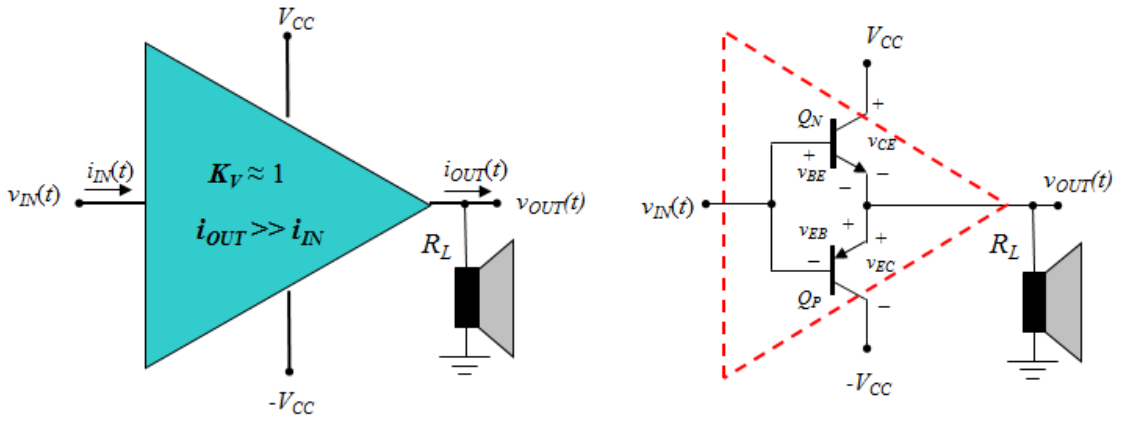
$$v_{OUT}(t) = v_{IN}(t) - V_{BE\gamma},. \tag{12}$$

The electric current requested by the load will then by provided by the source V_{CC} through Q_N and the output will be positive. Meanwhile, the emitter-base junction will be reversed-biased, $\boldsymbol{v_{EB} = -V_{BE\gamma}}$ ($\boldsymbol{<V_{EB\gamma}}$), and Q_P will remain in cut-off mode. On the other hand, when $\boldsymbol{v_{IN} \leq -V_{EB\gamma}}$, the transistors Exchange their behavior and Q_P will the be active. The output is then connected again to the input through the emitter-base junction of Q_P, and it will be negative.

$$v_{OUT}(t) = v_{IN}(t) + V_{EB\gamma}. \tag{13}$$

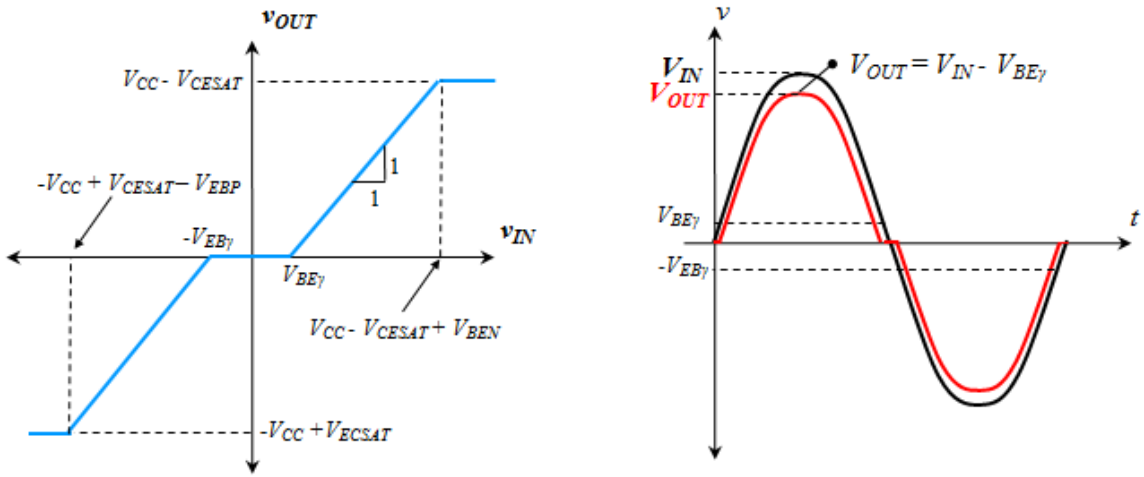
As such, the output current will be derived to $-V_{CC}$. This circuit is often said to operate in a *push-pull* fashion: Q_N "pushes" (sources) current into the load when v_I is positive, and Q_P "pulls" (sinks) current from the load when v_I is negative. Fig. 6a shows the transfer characteristics of the current driver. When the input is large enough to cause saturation of Q_N, the output reaches its maximum $\boldsymbol{V_{OUT} = V_{CC} - V_{CESAT}}$ and, analogously the minimum – $\boldsymbol{V_{OUT} = -V_{CC} + V_{ECSAT}}$ (Fig. 6b) when the input is small so as to saturate Q_P. These values define the output swing and is almost fully determined by the power supplies $\boldsymbol{\Delta v_{OUT} \approx \pm V_{CC}}$.

[1] In the field of electronics, the terme *driver* is used to coin the action of transferint a signal between two circuits (or stages) that cannot be directly connected, due to electrical compatibility. Hence the term *driver*.



a) b)

Figure 5. Current driver. a) Symbol, output connection and power source. b) Electric diagram of the *push-pull* configuration using complementary BJTs.

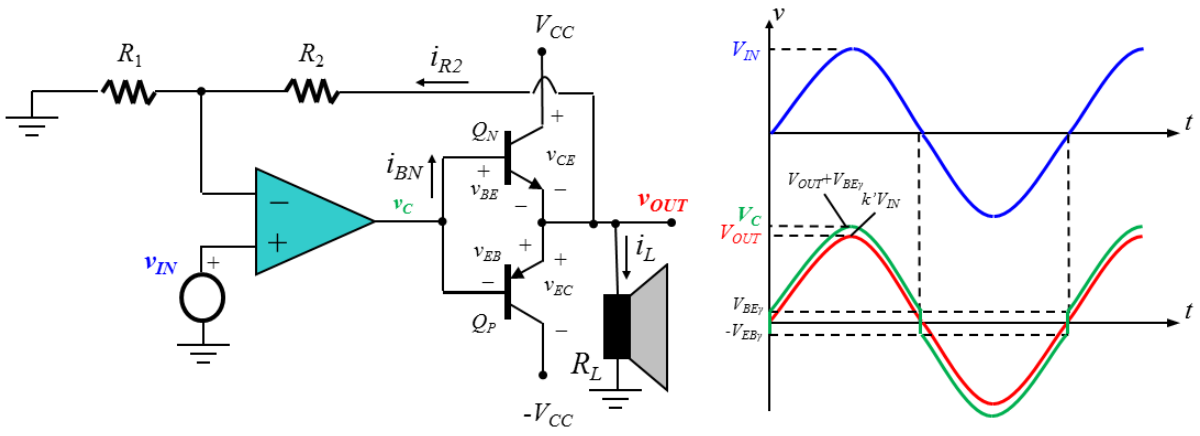


(a) (b)

Figure 6. Transfer characteristics of the current driver. a) v_{OUT}-v_{IN} plot. b) Output example for a sinusoid input. v_{IN} – black; v_{OUT} - red.

The **dead band** corresponds to the range where both transistors are cut-off and results in the *crossover distortion*. The effect of this distortion will be pronounced when the input amplitude is very small and results in unpleasant sounds. This problem can be reduced substantially by means of a high-gain OPAMP and taking advantage of the noninverting configuration seen in section 2. In this solution, the driver is placed between the OPAMP and the speaker, with the resistor terminal R_2 connected at the circuit output, instead of the operational output (Fig. 7a). The **±0.7V** ($V_{BE\gamma}$) dead band is then reduced to almost $\Delta \boldsymbol{v_i}$ = **±0.7V/*k***.

Nevertheless, the OPAMP must provide an instantaneous transition at v_C, $\Delta \boldsymbol{v_C}$ = **±0.7V** (Fig. 7b), and the alternate turning on and off of the transistors will be noticeable due to the *Slew-Rate* (SR) limitation of the 741, so the distortion will be slightly present, especially at higher frequencies. Since the SR in the 741, defined as



(a) (b)

Figure 7. Reducing crossover distortion using OPAMP in the basic audio amplifier. a) Schematics. b) Most representative signal waveforms for a sinusoid input: v_{IN} (blue), driver input v_C (green) and output v_{OUT} (red).

$$SR = \left.\frac{dv_C}{dt}\right|_{\max}, \tag{14}$$

is SR = **0.5V/µseg**, for an output swing Δv_C **= ±15V** the maximum operating frequency

$$f_{\max} = \frac{SR}{2\pi\Delta v_C}, \tag{15}$$

results in f_{max} = **2.65KHz**. Other OPAMPS with advanced features present a *slew rate* as high as 100V/µseg.

Finally, despite reducing the current capacity at the driver input by $i_B \approx i_L/(h_{FE}+1)$[2] this value is still even large for the OPAMP, due to the lower gain current factor (h_{FE} <**100**) are of the high-power BJTs[3]. To reduce the required base current drive, the *Darlington* configuration (Fig. 8) is frequently used to replace the *npn* transistor[4]. Since,

$$i_{BN} \approx \frac{i_{E1}}{(h_{FE1}+1)} = \frac{i_L}{(h_{FE1}+1)(h_{FE2}+1)}, \tag{16}$$

This configuration is equivalent to a *npn* BJT with current gain $h_{FE} \approx h_{FE1}h_{FE2}$, where h_{FE1} is the current gain for the low-power BJT, typically $h_{FE1(typ)} \approx$ **500**. As such, for h_{FE2} = **100**, the full gain factor is $h_{FE} \approx$ **500,000**. For this reason, this configuration is popularily known as the "supertransistor", but it has the disadvantage that it doubles the base-emitter voltage: $v_{BE} = 2V_{BE\gamma}$.

[2] For simplicity of the analysis, we assumí $i_L >> i_{R2}$.
[3] Generally, a power BJT provides high capacity current at the collector terminal (I_C > 1A) but in turn reduces drastically its current gain h_{FE} in relation to small signal low-power BJTs.
[4] Analogously the Darlington pair can be also adopted in *pnp* transistors

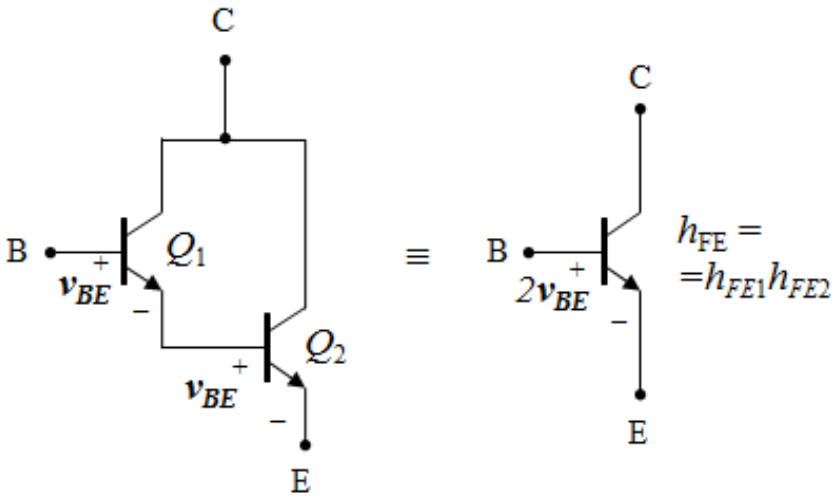


Figura 8. The Darlington configuration pair

The output swings of the Darlington pair and the complementary BJTs are the same: $\Delta v_{OUT} \approx \pm V_C$. In the Darlington case, since $v_{CEN} = v_{CE1} + v_{BEN}$ and habitually $V_{CENSAT} > V_{CE1SAT}$[5], when Q_N enters the saturation area Q_1 will still be in active mode. So the maximum power that can be transferred by the audio amplifier to the load speaker is

$$P_{Lef} = \frac{v_{OUTef}^2}{R_L} = \frac{V_{O\max}^2}{2R_L} = \frac{\left(V_{CC} - V_{CESAT}\right)^2}{2R_L} \qquad (17)$$

Task PRELAB1. In the Bread-Board template provided, represent the component connections of the audio amplifier (Fig. 9). Specify the connections of instruments, components, wires and terminals.

- Search information through the Internet about the connection of a log potentiometer.
- Specify power supply configuration for obtaining a symmetric DC voltage and explain how it should be connected to the circuit.
- Draw the circuit in the template. Specify speaker, potentiometer and oscilloscope connections, together with the JACK connector, which is needed to introduce audio signal from the PC.

[5] The V_{CESAT} of high power BJTs is also slightly superior to that of small signal transistors, between 1 or 2 volts, approximately.

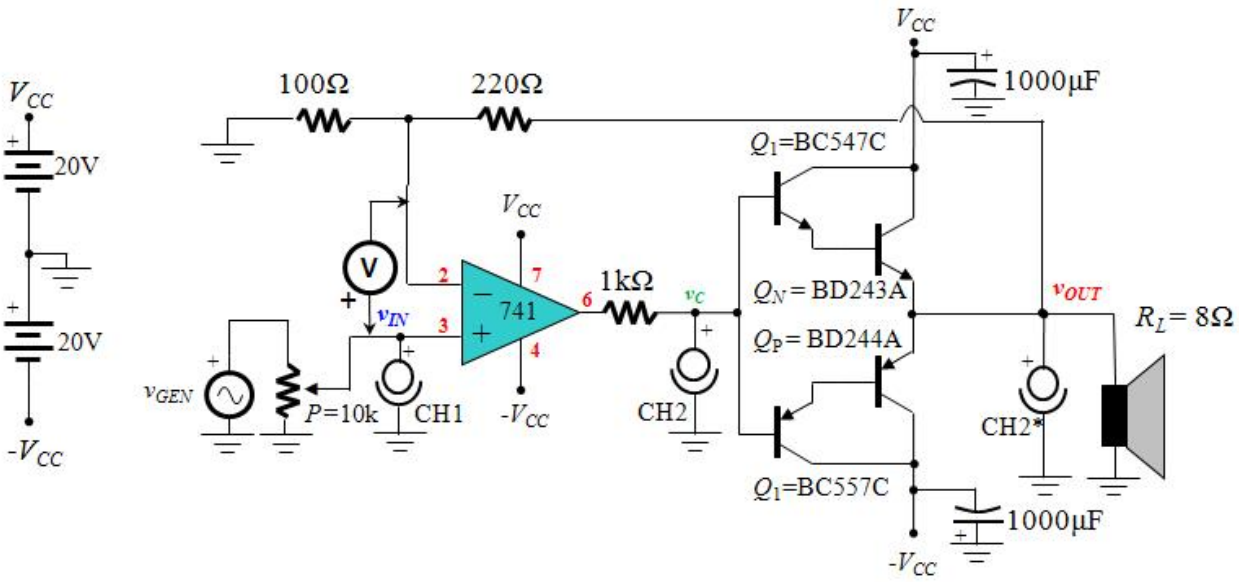


Figura 9. Full schematics of the audio amplifier

Task LAB1. Mount the audio amplifier (Fig. 9) and check its electric operation

- Operation check: **1)** Mount the circuit. Try to connect the DC supply directly to the power BJTs and place the capacitors next to them in order to avoid the effects of thermal noise. To start with, do not connect the potentiometer (*P*) yet and use a **10Ω/5W** load instead of the speaker (R_L) **2)** By means of the **50Ω** output in the waveform generator, configure a **1V**-peak **sinusoid**, set the frequency value to ***f* = 500Hz** and connect the output to the noninverting input of the OPAMP (v_{IN}) **3)** Observe the input through CH1 using the BNC-BNC probe and the T connector, and connect CH2* to the load in order to observe the output v_{OUT}. **4)** Configure the multimeter for measuring AC voltages (VAC) and measure v_D. Connect its terminals as indicated in Fig. 9 **5)** Measure the closed-loop voltage gain of the amplifier *k'* and contrast results (*k'*=3) from the theoretical expression (10). **6)** In the grid provided, represent the signals $v_{IN}(t)$, $v_{OUT}(t)$ and $v_C(t)$. Change the position of CH2* at the OPAMP output to observe and plot the third variable and write down the data specified in Table A3.1. Comment the results and justify the value $\boldsymbol{v_D}$ obtained with the multimeter.
- **7)** Increase the input magnitude top **2V** and repeat the precedent steps. Draw the new waveforms v_{IN}, v_{OUT} and write down the new value v_D. Comment the results.
- **8)** Turn all instruments off and now change the 10Ω load by the speaker. Set again a **1V-peak** input and turn the instruments on. Check whether a low sound can be heard from the speaker. **9)** Modify the amplitude and the frequency *f* in order to feel the sound differences.
- **10)** Finally, turn the instruments off. Change the generator by the soundcard of the PC and use the male-male JACK cord to input audio signals in your circuit. Now, connect the potentiometer *P* as indicated in Fig. 9. **11)** Go to the *YouTube* website

and search a video with audio. **12)** Turn the power supply on and play the video. Check the correct performance of the circuit.

4. Free running multivibrator (square waveform generator) with OPAMP (Optional)

As discussed in section 1, when the OPAMP is operated with positive or negative saturation its output can only take two possible values: either V_{OH} or V_{OL}. This type of behavior is known for being a *switching* (as well as *digital*) application. Examples of electronic systems using this principle are: *voltage comparators*, *ON/OFF controllers*, *waveform generators* or *analog-to-digital* (as well as *digital-to-analog*) converters, all of them wide spread at an industrial level.

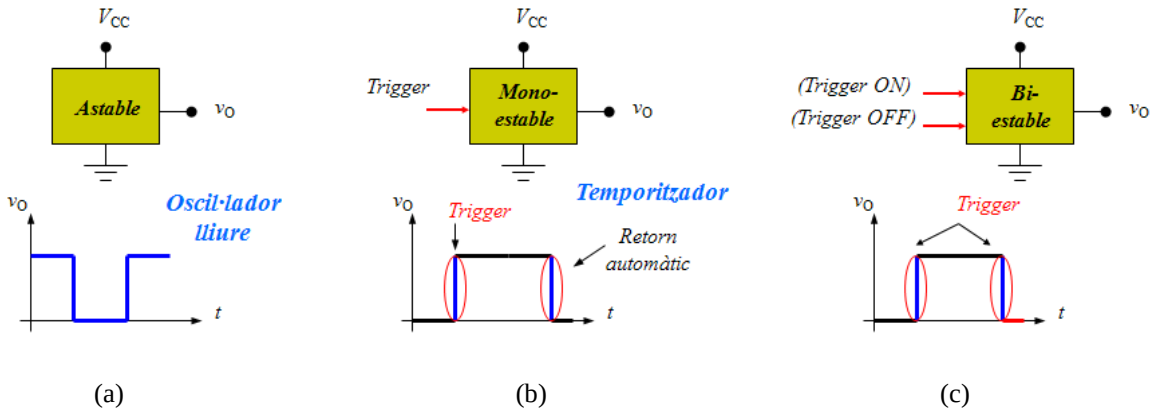
In the field of audio applications, another important operation that coexists with signal amplification is the synthesization (or generation) of periodic signals. The most demanded type of generators are the sinusoid oscillators, normally used for constructing "any" kind of waveform pattern in sound applications, as the sinusoid constitutes the basis function for obtaining almost any type of periodical signal[6]. But there are other types of signal generators whose specifications are not so strict. These generators construct signals of pulse characteristics. Among this group, instruments generating square, triangular or even saw-tooth waveforms can be found. To this type of oscillators, normally the term *free-running* oscillator (or also *relaxation oscillators*) is used.

Their operation principle is quite similar to that of the two-shot multivibrator considered in Lab Activity 4, with the main difference that no external trigger is needed to cause a level change at the output (in the SET/RESET changes were caused by external switches). In fact, multivibrators can be grouped in three categories according to Fig. 10:

a) **Free-running** (or *relaxation*) **oscillator:** This multivibrator toggles from "0" to "1" and vice versa with no need of external commands. This means the two logical values are unstable because they are alternated with the time without user intervention.
b) **One-shot multivibrator:** One of the two logical levels (either "0" or "1") is stable by default. When forced into the other logic state, say via an external command or trigger, it returns automatically to its original value after a certain time interval.
c) **Two-shot multivibrator:** Both logical levels are stable, and external commands are needed to toggle the output to a given state.

Multivibrators are considered regenerative circuit intended for timming applications and, as such, are normally used in sequential logic circuits. The free-running multivibrator find applications as clock signals while the one-shot multivibrator is used as a timer. On the other hand, latches and flip-flops (D-type, JK-type or RS-type, among others) are typical applications of the two-shot multivibrator.

[6] By using the *Fourier Series*, it can be shown that any periodical signal (no matter what the waveform is) can be expressed as a compostion of sinusoid wit diferent amplitude, frequency and phase shift.



(a) (b) (c)

Figure 10. The three multivibrator types and their operation principle: a) Free-running; b)One-shot c) Two-shot.

- *Free-running multivibrator with OPAMP*

In the free-running multivibrator with OPAMP of Fig. 11a, the capacitor *C* and the resistor *R* in the negative feedback, and the resistors R_1 and R_2 (positive feedback) form an inverting *Trigger Schmitt.*

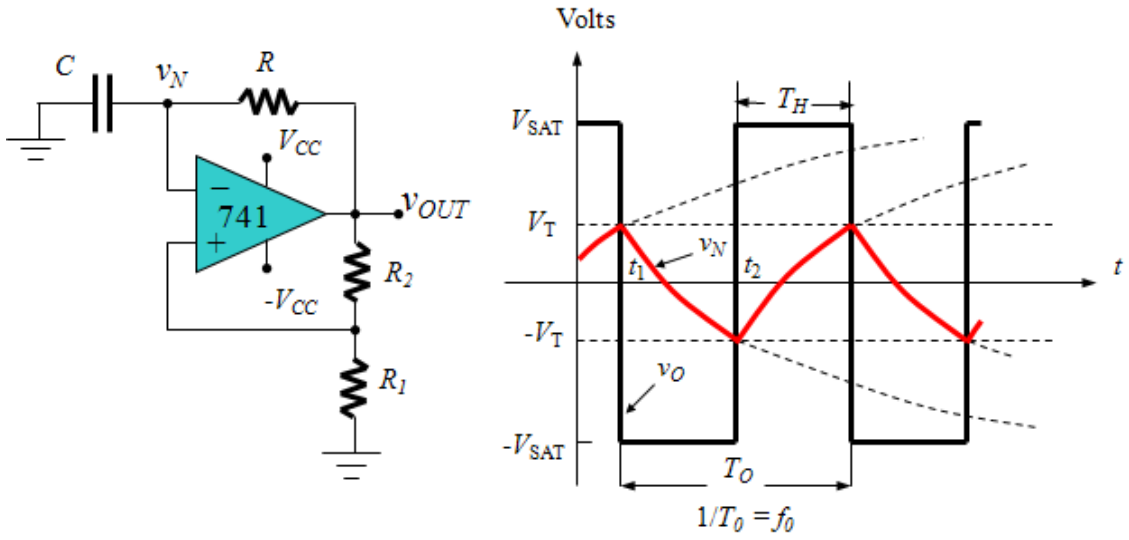
When $\boldsymbol{v_{(7)} = -v_{(4)} = V_{CC} = 15V}$ and assuming symmetric output saturation, $\boldsymbol{V_{SAT} = +13V}$ and $\boldsymbol{-V_{SAT} = -13V}$ since the positive feedback is predominant in this circuit[7], the thresholds at v_P will also be symmetric with $\boldsymbol{\pm V_T = \pm V_{SAT} R_1/(R_1 + R_2)}$ and the signal to the inverting input, while the inverting input v_N the voltage is determined by the *RC* network.

At power turn-on ($t = 0$), v_{OUT} will swing either to $+V_{SAT}$ or $-V_{SAT}$. Assume iy swings to $+V_{SAT}$, so that $v_P = +V_T$. This will cause the resistor *R* to charge *C* towards $+V_{SAT}$, leading to an exponential rise in v_N with time constant $\tau = RC$.

As son as v_N catches up with $v_P = +V_T < v_N$ at $t = t_1$, the output snaps to $-V_{SAT}$. This will not only snap $v_P = -V_T$ but it will reverse the sing of the capacitance current. As such, for $t > t_1$ the capacitor voltage will decay exponentially towards $-V_{SAT}$ until it caches up with $v_P = -V_T > v_N$ at $t = t_2$. At this point, the output will snap again to $+V_{SAT}$ thus repeating the cycle.

It is evident that once powered, the circuit has the ability to start and sustain oscillations: with v_O snapping back and forth between $+V_{SAT}$ and $-V_{SAT}$; and v_N slewing exponentially from $+V_T$ to $-V_T$ and vice versa; so the waveform signal becomes square and periodic (Fig. 11b). Thus, it is interesting knowing the oscillation frequency $\boldsymbol{f_0}$ which can be found from the period *T* as $T = 1/f_0$.

[7] One may think that this circuit uses negative feedback, because of the *RC* network, and that the concept of ideal OPAMP can be therefore applied. However, when another branch is present in the positive path, and in the absence of external input sources (as it is the case of this cexampl), the positive feedback prevails over the negative feedback and will force the OPAMP to operate in saturation mode, working as a voltage comparator.



(a) (b)

Figure 11. Free-running multivibrator using OPAMP. a) Electric diagram. b) Time signals at the output v_{OUT} and the inverting input v_N (red trace).

Thanks to the symmetry of the saturation levels, the output v_O has a *duty-cycle*, $D = T_H/T$ of 50% (=0.5), so finding the interval range $\Delta t = t_2 - t_1 = T/2$ is necessary. Using the standard expression corresponding to the capacitor charge/discharge[8] in this range,

$$v_C(t_2) = v_N(t_2) = v_C(\infty) + \left[v_C(t_1) - v_C(\infty)\right] e^{-\frac{\Delta t}{\tau}} \qquad (18)$$

where $\boldsymbol{v_C(\infty) = -V_{SAT}}$; it holds that for $\Delta t = T/2$, $v_N(t_1) = +V_T$, $v_N(t_2) = -V_T$; and $\tau = RC$ we obtain,

$$\frac{T}{2} = RC \ln\left(\frac{V_{SAT} + V_T}{V_{SAT} - V_T}\right). \qquad (19)$$

Substituting $V_T = V_{SAT}R_1/(R_1 + R_2)$ and equating $f_0 = 1/T$ it leads to,

$$f_0 = \frac{1}{T} = \frac{1}{2RC \ln\left(1 + 2\frac{R_1}{R_2}\right)}, \qquad (20)$$

It can be observed that f_0 depends only on the external components. In particular, it is unaffected by V_{SAT}, which is an ill-defined parameter which varies from one OPAMP to another: any variation in V_{SAT} will cause V_T to vary in proportion, thus ensuring the same transition time and, hence, the same oscillation frequency. On the other hand, the maximum operating frequency is determined by the OPAMP *slew-rate* of expression (15).

[8] See the document of PRT2, where the step response of the *RC* network was considered, in order to understand expression (11) in the interval $\Delta t = t_2 - t_1$

Task PRELAB2 (**Optional**). In the Bread-board template represent the component distribution and wire connections corresponding to the OPAMP-based free-running multivibrator of Fig. 12 to be implemented in the lab.

Task LAB2 (**Optional**). Mount the circuit and check the performance of the OPAMP-based free-running multivibrator (Fig. 12).

- **1)** Mount the circuit. Connect the DC power-supply and oscilloscope probes as indicated in Fig. 12. Turn the power on and represent the capacitor voltage v_C in CH1; and the output v_{OUT} in CH2. **2)** Obtain the threshold values: $\pm V_{SAT}$, $\pm V_T$; and measure the oscillation frequency f_0. 3) Compare the experimental results with the theoretical values obtained by means of (16).

Task PRELAB3 (**Optional**). How would you connect the two circuits of this activity (Fig's. 9 and 12, respectively) in order to synthesize and to hear a low sound of **500Hz** through the speaker? Represent the circuit in the box provided and specify component values.

Task Lab3 (**Optional**). Mount the circuit from PRELAB3 and check its electric operation.

- **1)** Mount the circuit. **2)** Using the oscilloscope and/or the multimeter represent the waveforms and obtain the data you believe it is important in order to understand circuit behavior.
- Comment results regarding the sound synthesizer.

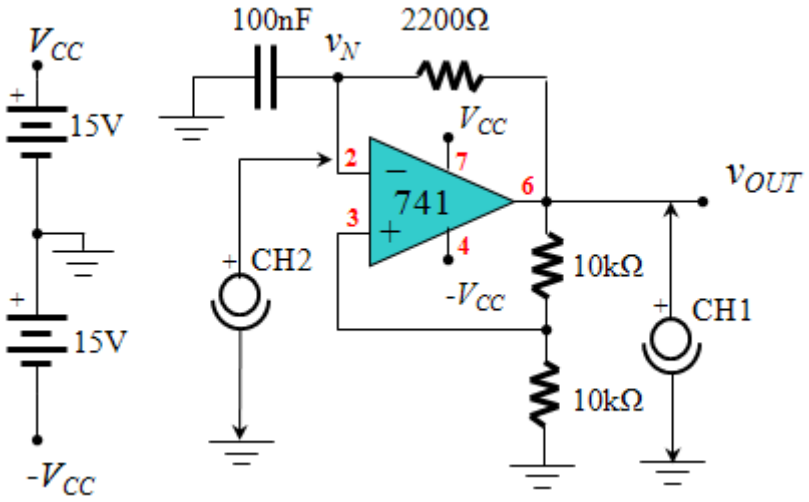
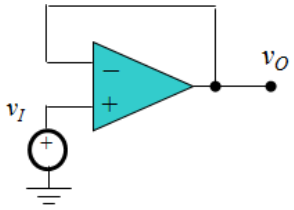
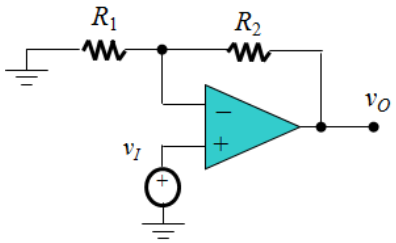
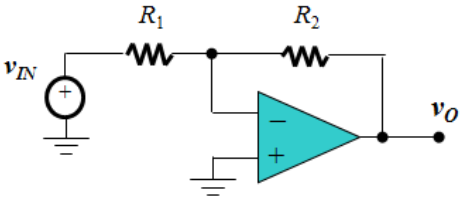
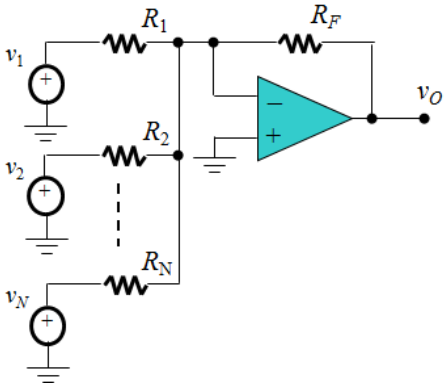
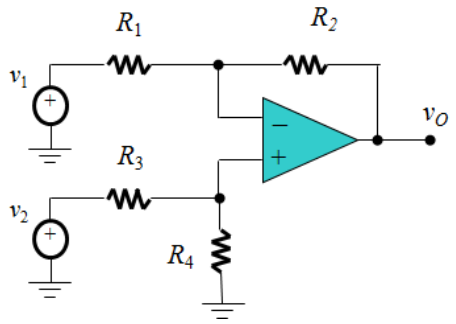
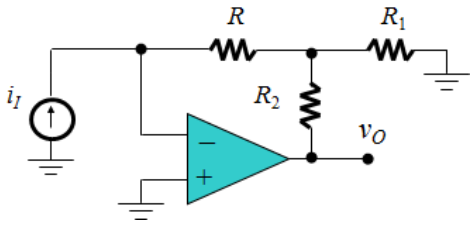
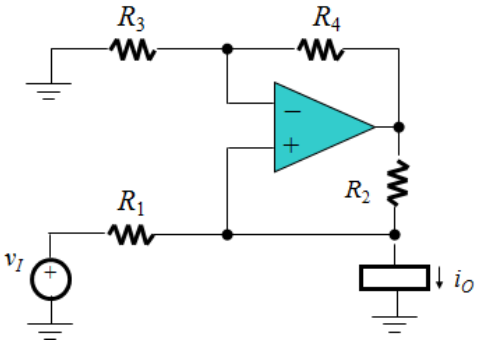
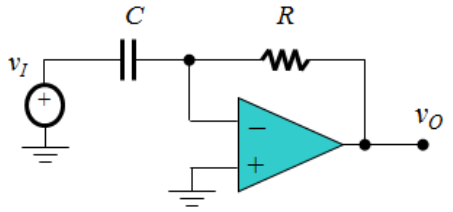
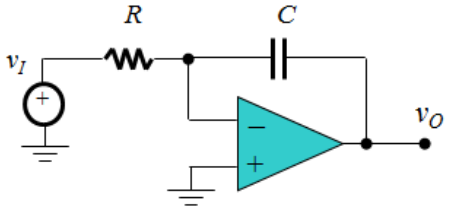


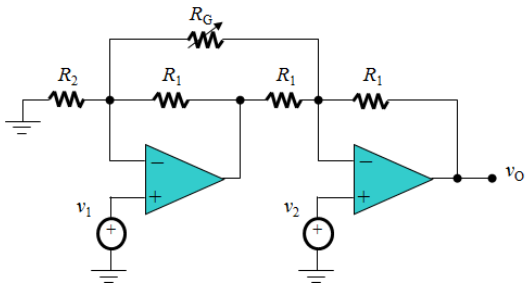
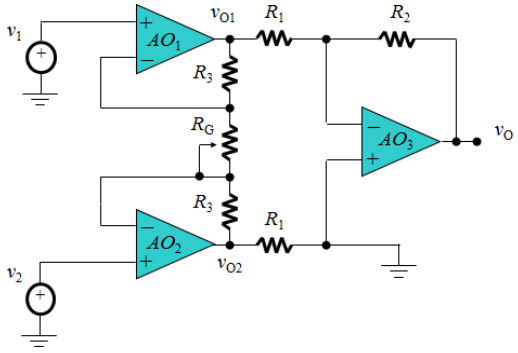
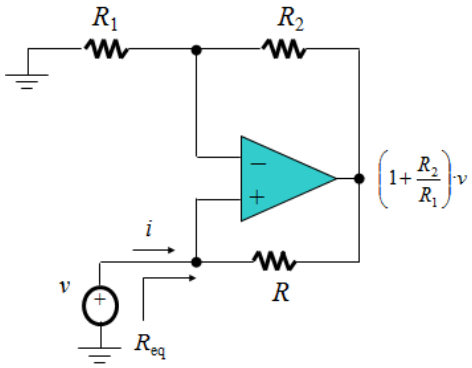
Figure 12. Mounting diagram corresponding to the free-running multivibrator in the lab.

Annex 1 – OPAMP basic configurations (with negative feedback)

The OPAMP circuits of this section are considered basic. Very often, these circuits are used as stages of very complex analog electronic systems. In here, all configurations use negative feedback operation. Only the connection diagram (without DC supply) and the transfer function of each circuit is specified in Table 1. The analytical process necessary to obtain these functions are left to the reader as an exercise.

Circuit name	Connection diagram	Function
Voltage Follower		$\frac{v_O}{v_I}=1$ $v_O = v_I$
Noninverting amplifier		$\frac{v_O}{v_I}=1+\frac{R_2}{R_1}$
Inverting Amplifier		$\frac{v_O}{v_{IN}}=-\frac{R_2}{R_1}$
Inverting adder Amplifier		$v_O = -R_F \sum_{i=1}^{N} \frac{v_i}{R_i}$

Diferential Amplifier		$v_O = \left(1+\frac{R_2}{R_1}\right)\frac{R_4}{R_3+R_4}v_2 - \frac{R_2}{R_1}v_1$ *** If** $R_1 = R_2 = R_3 = R_4$ $v_O = v_2 - v_1$
I/V Converter (T network)		$v_O = -kRi_I$ where $k = 1+\frac{R_2}{R_1}+\frac{R_2}{R}$
Howland's current source		$i_O = \left(\frac{R_4R_1 - R_2R_3}{R_1R_2R_3}\right) + \frac{v_I}{R_1}$ * if $R_4/R_3 = R_2/R_1$ $i_O = \frac{v_I}{R_1}$
Derivator		$v_O(t) = -RC\frac{dv_I(t)}{dt}$ $\frac{v_O(s)}{v_I(s)} = -RCs$
Integrator		$v_O(t) = -\frac{1}{RC}\int_0^t v_I(t)dt + v_c(t_0)$ $\frac{v_O(s)}{v_I(s)} = -\frac{1}{RCs} + \frac{v_c(t_0)}{s}$ * Habitually $t_0 = 0$

Instrumentation Amplifier (2 OPAMPS)		$v_O = A_d\left(v_2 - v_1\right)$ $A_d = \left(1 + \frac{R_2}{R_1} + 2\frac{R_2}{R_1}\right)$
Instrumentation Amplifier (3 OPAMPS)		$v_O = A_d\left(v_2 - v_1\right)$ $A_d = \left(1 + 2\frac{R_3}{R_G}\right)\frac{R_2}{R_1}$
Negative Impedance Converter (NIC)		$R_{EQ} = -\frac{R_1}{R_2}R$ *** If** $R_1 = R_2$ $R_{EQ} = -R$

Taula 1. Diverses configuracions bàsiques amb un o varis operacionals, i la seva funció de transferència

Annex 2 – Results form PRELAB

REMARK: You **MUST** these activities **BEFORE THE LAB SESSION CORRESPONDING TO PRT5**

UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH Escola Politècnica Superior d'Enginyeria de Vilanova i la Geltrú	EEL
Electronic Systems (SIEK) **Activity 5:** Analog Electronics: The operational amplifier (OPAMP) **PRELAB**	
Students:	**Date:**

PRELAB 0: Draw the contour package packages corresponding to the **LM741**; the BD243 and BD244.

Paràmetre	***LM741***	***Observacions:*** Coment manufacturer observations
k		
Δv_O		
V_{CC}		
SR		

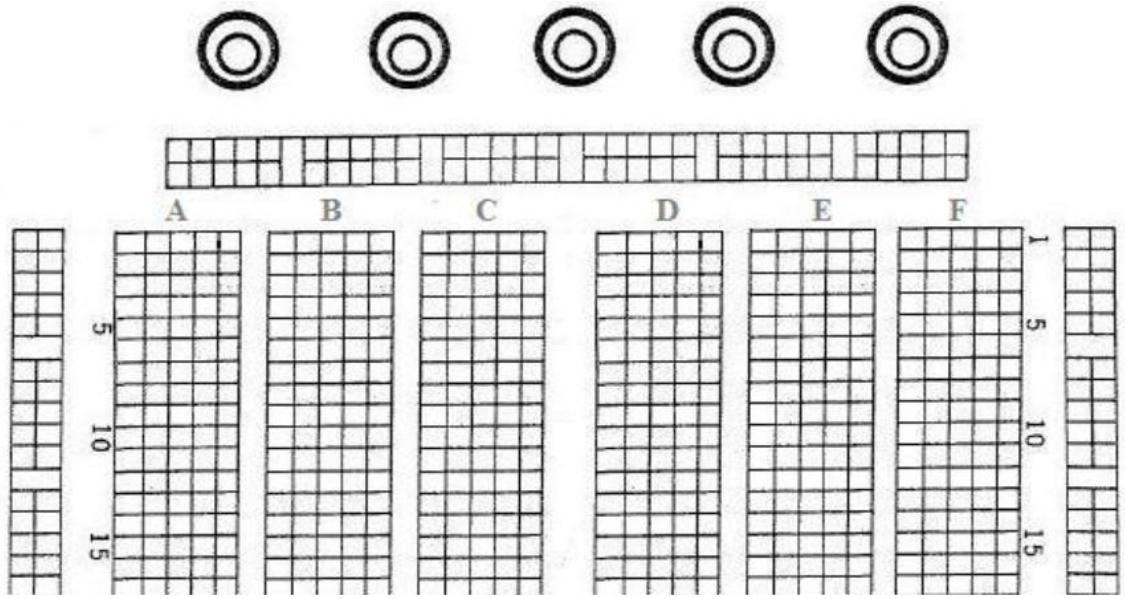
Taula A2.1 Anoti la informació relativa al BC547C que ha trobat al full de característiques

PRELAB1. Audio amplifier with OPAMP

Represente the contour package of the potentiometer and specify pin function

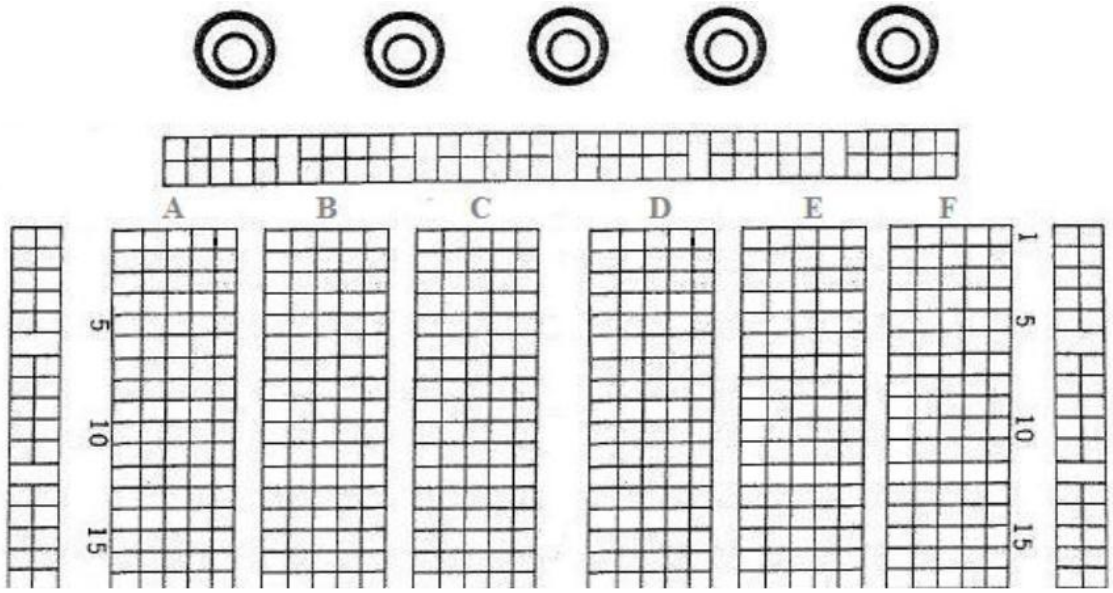
Specify connection and configuration of the DC-power supply so as to obtain **a symmetric power DC-voltage of ±15V**

Represent the component connections of the audio amplifier



PRELAB2(Optional): OPAMP free-running multivibrator

Represent the component connections of the OPAMP-based free-running multivibrator



PRELAB3 (Optional): Sound synthesizer

Represent the electric diagram corresponding to the sound synthesizer

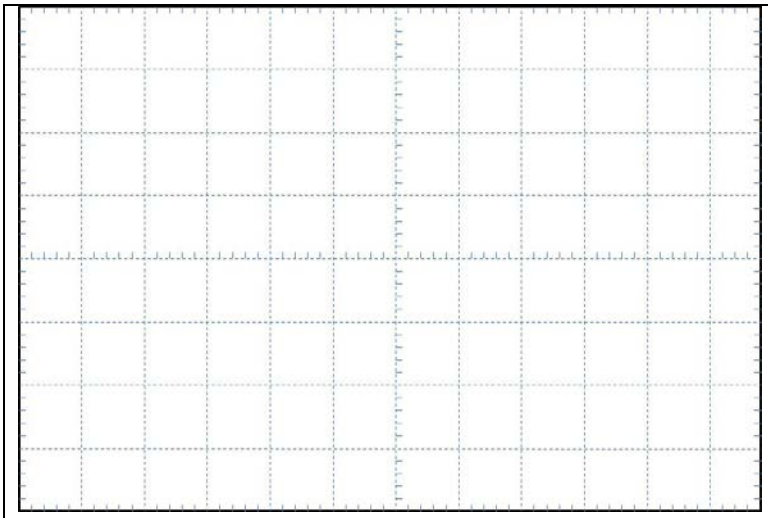
Annex 3 – Lab activities

REMARK: You **MUST PRINT OUT** and **TAKE IT WITH YOU** the day of the lab session

UNIVERSITAT POLITÈCNICA DE CATALUNYA BARCELONATECH Escola Politècnica Superior d'Enginyeria de Vilanova i la Geltrú	EEL
Electronic Systems (SIEK) **Activity 5:** Analog Electronics: The operational amplifier (OPAMP) **RESULTS FORM**	
Students:	**Date:**

LAB1. Audio amplifier.

Represent the waveforms $v_{IN}(t)$ and $v_{OUT}(t)$ (1V-peak v_{IN})



CH1 VOLT/:

Zero POS:

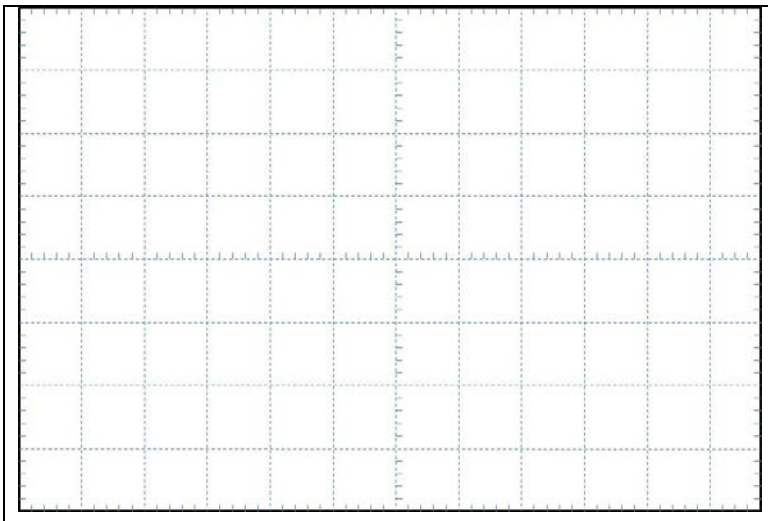
CH2 VOLT/:

Zero POS:

TIME/:

Acob:

Represent the waveforms $v_{IN}(t)$ and $v_C(t)$ (1V-peak v_{IN})



CH1 VOLT/:

Zero POS:

CH2 VOLT/:

Zero POS:

TIME/:

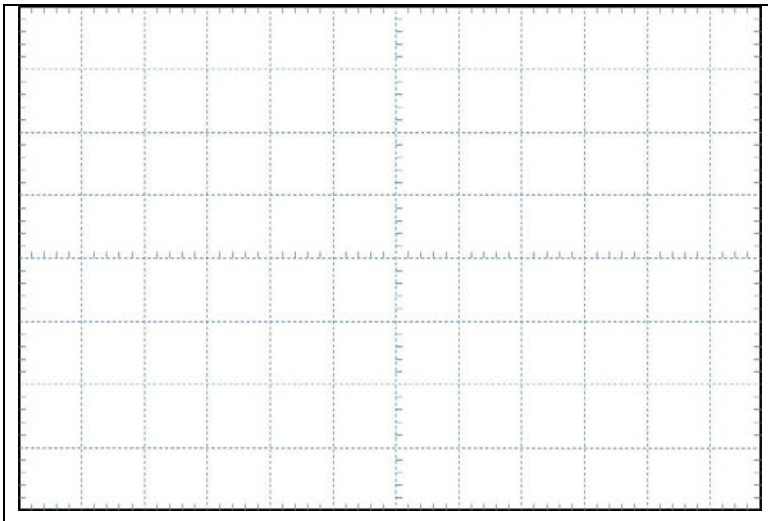
Acob:

Summary of results:

Variable elèctrica	*Teoric*	*Laboratori*	*Variable elèctrica*	*Teoric*	*Laboratori*
V_C			v_D (AC)		
V_{OUT}			ΔV_C (Zona morta)		
k'			P_L		

Table A3.1. Results of the audio amplifier

Represent the waveforms $v_{IN}(t)$ and $v_C(t)$ (2V-peak v_{IN})



CH1 VOLT/:

Zero POS:

CH2 VOLT/:

Zero POS:

TIME/:

Acob:

V_{OH}:_____ (Teòric); V_{OH}:_____ (lab); v_D (AC):_____

Your comments about the performance of the audio amplifier:

_____

_____

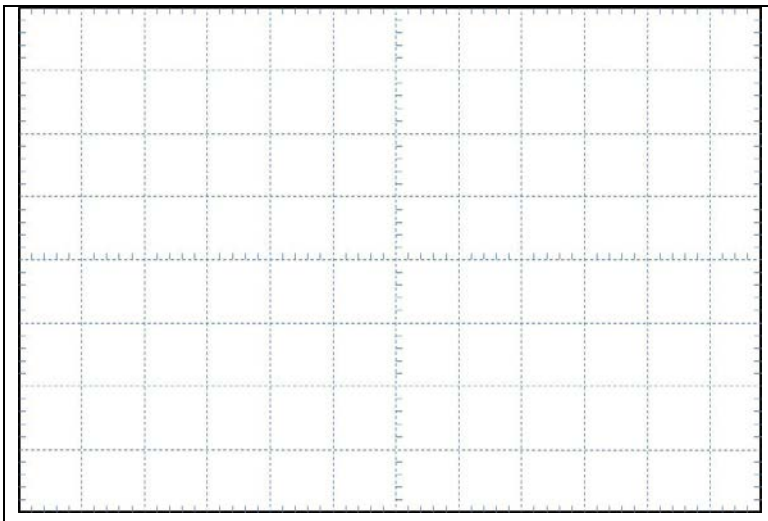
_____

_____

_____

LAB 2. (Optional): OPAMP-based free-running multivibrator

Represent the waveforms $v_C(t)$ and $v_{OUT}(t)$

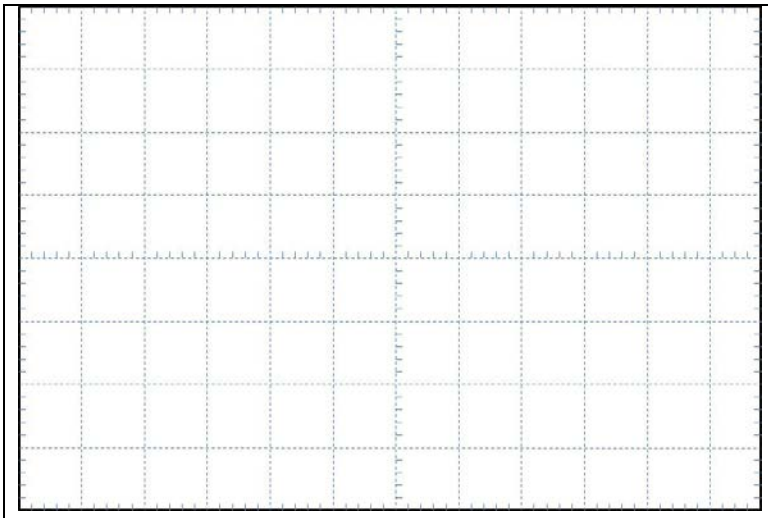
	**CH1** VOLT/: **Zero POS:** **CH2** VOLT/: **Zero POS:** **TIME**/: **Acob:**

V_{SAT}:_____ $-V_{SAT}$:_____ V_T :_____

f_O (theoretical):_____ f_O (lab):_____

LAB 3 (Opcional): Sintetitzador de so

Represent thecircuit signals you believe are important

	**CH1** VOLT/: **Zero POS:** **CH2** VOLT/: **Zero POS:** **TIME**/: **Acob:**

Your comments about the performance of the audio synthesizer circuit: