Advanced design features of Doherty power amplifiers

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***Abstract*- A Doherty power amplifier (DPA) is an effective structure born in 1936 which, after a scarce revival around year 2000), had been strengthened from 2005 because its capability to combine linear amplification with power efficiency. Despite the conceptual simplicity of its basic operation, a lot of practical drawbacks shrink the theoretical behavior, thus leading a significant number of research works to overcome them. The main objective in DPA research is to increase efficiency while maintaining linearity and filling the specified bandwidth. This paper presents a survey of the state of the art of DPA advanced design aspects. After a short review of the DPA operation principles, aspects regarding improvements for linearity, power efficiency and amplification bandwidth are introduced. Besides, some alternative structures and technologies, as well as practical design aspects and some trade-offs which the designer usually has to face are also presented.**

I. INTRODUCCIÓN

The power amplifier is the most expensive and power-hungry component in modern radio transmitters for communications and radar systems. So, aiming to achieve high power efficiency, some enhancement techniques using an envelope amplifier and/or a switching amplifier, such as envelope elimination and restoration (EER), polar transmitters (PT), and envelope tracking (ET), have been reported. These envelope-modulation (drain modulation) based amplifiers may provide excellent efficiency performances with the help of digital predistorters (DPD) to fulfill the high linearity requirements in new communications standards. However, these techniques have some unfavorable factors to be solved [1], such as the insufficient bandwidth of the envelope amplifier for some applications, the difficulty of delay adjustments in each path (RF and envelope path), and somewhat increased implementation complexity [2].

Even though it was first proposed by W.H.Doherty in 1936, the Doherty power amplifier (DPA) is an efficiency improvement alternative whose practical application has been practically ignored until last decade. Reasons are twofold: on one side, the elevated cost of the energy and the sensitivity to environmental effects (i.e, air conditioners in base-band power stations used to keep cold the power amplifiers). On the other hand, modern communication standards, with an increasing demand for higher data-rates, force the use of advanced modulation formats with information contained in both the amplitude and phase variations. Advanced QAM-based modulation and CDMA or OFDM accesses produce high peak-to-average power ratios (PAPR) of the signal, thus requiring, apart from a high bandwidth, a good PA linearity. The use of a typical single-ended linear power amplifier (class A, B, or AB) means that saturation levels are reached only in modulation peaks, thus showing low power efficiency, especially in the case of high PAPR. The DPA increases the power efficiency, especially at high power levels, exploiting the fact that power transistors deliver maximum efficiency when they operate at their saturation level.

Most important manufacturers of power amplifiers (PA) have already bet for spending in DPA research. Nowadays it is possible to have on the shelf both connectorized amplifiers and dedicated DPA as RFICs. Besides, DPA is currently the most favored method for the linearization of base-station amplifiers [3]. DPA have been constructed in different transistor technologies, such as Si LDMOS, GaN HEMT, GaAs PHEMT, GaAs HBT or GaN, and designs with transmit power ranging from few watts to 250-500 W have been reported [4]. Measured efficiencies range from 35 to 80% at medium-high power levels, depending on the applications and the particular structure of the DPA.

II. DPA OPERATION PRINCIPLE: LOAD MODULATION

The basic structure of a DPA ([4][5][6]) is shown in Fig.1.

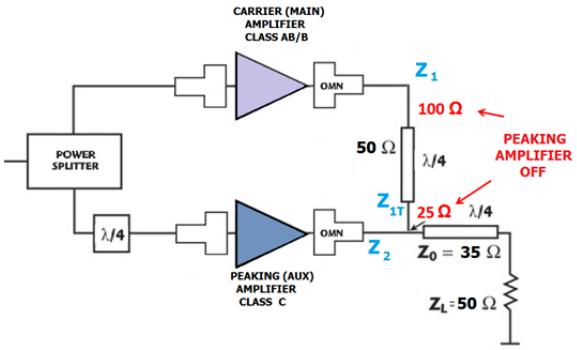


Fig 1. Fundamental structure of a DPA.

At low power levels (*low power region*), the *peaking amplifier* (PkA) is in cut-off state ($Z_2 \rightarrow \infty$), and the quarter wavelength transformers produce the impedances indicated in Fig.1 for a load impedance of 50 Ω (at VHF lumped matching circuits are used as impedance inverters). To assure the ideality within the low power region, some implementations add a transmission line (*offset-line*) after the output matching network (OMN) to assure the infinite impedance in Z_2 despite the actual output reactance of the

cut-off PkA. For the Doherty operation (Doherty region, i.e, the carrier amplifier -CA- being saturated and the PkA switched-on), the CA is biased at pinch-off and the PkA below pinch-off. The simplified model is shown in Fig.2,

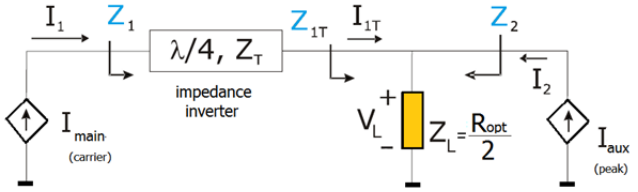


Fig 2. Doherty schematic diagram

It is straightforward to obtain:

$$V_L = \frac{Ropt}{2}(I_{1T}+I_2) \quad (1)$$

$$Z_{1T} = \frac{V_R}{I_{1T}} = \frac{Ropt}{2}\left(1+\frac{I_2}{I_{1T}}\right) \quad (2)$$

$$Z_2 = \frac{V_R}{I_2} = \frac{Ropt}{2}\left(1+\frac{I_{1T}}{I_2}\right) \quad (3)$$

The impedance inverter forces the impedance seen by the output of the CA to go down as the PkA turns on: from (2) when I_2 is increased, Z_{1T} also increased, so decreasing Z_1.

In the Doherty region (Fig.3), $I_1 = \frac{Imax}{4}(1+x)$, and $I_2 = \frac{Imax}{2}x$, being x=0 at the break point and 1 at maximum power (notice that if Doherty operation starts at half amplitude range, *x* corresponds to 6 dB of power backoff).

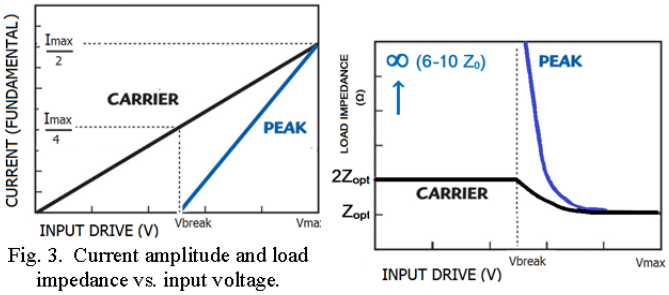


Fig. 3. Current amplitude and load impedance vs. input voltage.

In equilibrium conditions (maximum power), it is obtained:

$$I_{1T} = I_2 \quad \rightarrow \quad I_{1T} + I_2 = I_{total} = \frac{Imax}{2} \quad (4)$$

$$Z_{1T} = Z_2 = \frac{Ropt}{2}2 = Ropt \quad (5)$$

Within the Doherty region, I_1 is only dependent of V_{GS}, and the current through Z_L is increased because of the switch-on of the PkA. This implies a Z_{1T} increase, and consequently a Z_1 decrease. This decrease, together with an increase in I_1 ideally produces a constant value of V_{main}. Notice that if Z_{opt} = 100Ω, then $Z_{1T} = Z_2$ = 50 Ω, and the parallel results in 25 Ω in the combining point, the same value as in low power region.

III. DPA DRAWBACKS AND ADVANCED SOLUTIONS

Because the PkA is biased lower than the CA, the current of the PkA at the maximum input drive cannot reach, in practice, the maximum allowable current level [7]. Thus, the modulated load in not optimal and less power than expected is produced. On the other hand, in wideband applications the memory effects difficult to achieve high linearity degrees.

To overcome these drawbacks, ant to have a wide bandwidth, high linearity and high power DPA, some approaches have been proposed or experimented:

1) Uneven power driving
2) Multiway and multistage DPA
3) Individually optimized matching circuits
4) More power-efficient amplifier structures for both the PkA and the CA
5) Bias circuit optimization or adaptation
6) Use of linearizers
7) Broadband techniques

1) Uneven power driving

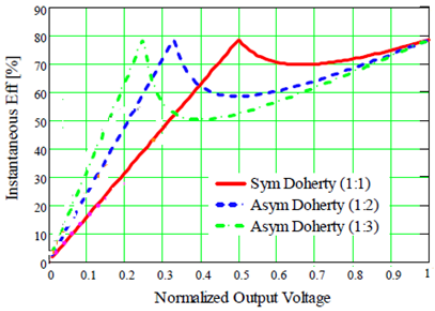
By driving the CA and the PkA by uneven power, (applying more power to the PkA, typically, 60-70% of the total input power) the load may be better modulated (by avoiding the overdriving of the CA). The amplifiers with uneven power drive show more linear and efficient operation, and produce more power than that with an even drive. Reported increases in drain efficiency ranges 10-13% [8], and 76% of drain efficiency has been reported [9]. In Fig. 4 (courtesy of NXP) it is presented the drain efficiency for different configurations of the asymmetrical power splitting. ACLR may be also improved by 5-7 dB. In [10] it is presented a DSP based solution, where the input signal power splitting is digitally controlled according to the signal statistics.

2) Multiway and multistage DPA

In multiway DPA the PkA is made by combining the output power of several power amplifiers, thus allowing increased linearity (larger OBO), while in multistage DPA the PkA is made with multiple Doherty structures working in a parallel configuration. It is usual the 3-stage DPA, where the first PkA modulates the load of the CA, and the second PkA modulates the load of the previous Doherty PkA [3]. It can be seen as a DPA where the PkA is an inner DPA. Multistage DPA produces a shift of the high efficiency region (see Fig. 4) to lower output voltage levels. In [11] it is faced the load-line modulation linearity problem associated with the three-stage Doherty (the load-line modulation of the CA stops at a certain power level, leaving the CA in deep saturation).

3) *Individually optimized matching circuits.*

The theoretical load of 100 Ω ($2R_{opt}$) for the CA is not actually the optimum load value because of the knee effect of the transistor, as well as the soft turn-on effect in the PkA [12].



Fig,4. Instantaneous efficiency for uneven drive

Because of lower bias point of the PkA, its matching circuit should be designed to have lower load impedance than

that of the CA [7]. Moreover, the matching circuits of both cells should be individually tuned to reduce IMD. Actually the success in the design of appropriate matching networks requires accurate simulation models of the power devices, as well as a further try-and-error procedure. In [13] we have constructed a DPA operating at the 2 GHz band. Power efficiency has been 47.5 %.

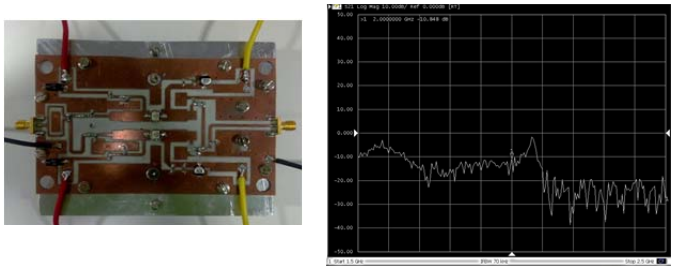


Fig. 5. Constructed DPA and S21 parameter (measured with a 10 dB atten).

In low power region the theoretical output impedance of 100Ω, becomes 92-43j (this problem with reactive parasitic components is also pointed in [14]). Conversely, the input impedance is not so divergent. This unexpected reactance produces maladjustments. I.e, the DPA has about 3 dB of gain fluctuation in the whole frequency band, which is 13dB at low power and 16.27 dB in the Doherty region. These results evidence the convenience of the offset-line already mentioned in Section II (the gain differences are due to the leakage of the output power from the CA to the PkA, thus reducing the gain in the low power region). The measured transmission coefficient is shown in Fig. 5.

On the other hand, if the CA is matched to 50 Ω, which is the ideal asymptotic impedance in Doherty region (this has been made just for experimenting impedance mismatches: it is not the right idea for practical designs), the power gain has a fluctuation of 6.7 dB, and the return loss of 9.4 dB. The gain fluctuation is usual in other published works, as well as the low gain; this fact confirms again the need of the offset-line.

4) Increased efficiency structures for both carrier and peaking amplifiers.

Overdriven amplifiers with harmonic-controlled matching topology [15][16][17], such as the class-F (generation of half-sinusoidal current and square-wave voltage waveforms) and inverse class-F (half-sinusoidal voltage and square-wave current) ones, are power efficient amplifiers which, if employed in the DPA, increases power efficiency in the range of 10-17% if compared to the typical configuration with class-B and class-C amplifiers. However, the ACLR is reduced by the order of 4-12 dB.

Another structure may be based on the combination of ET or PT and Doherty amplifiers [3], as shown in Fig. 6. However, the few published results point that, compared with the saturated DPA, the DPA with a drain modulator produces only slightly PAE, while the ACLR is degraded [18].

5) Bias circuit optimization or adaptation

Apart from its basic function for transistor operation, the design of bias circuit of the power amplifiers inside the Doherty structure should also cope with additional missions [19], such as to improve the linearity and the efficiency, to minimize the memory effects, and to maintain constant the gain in both low-power and Doherty regions. The trade-off is between linearity and gain versus power efficiency, as well as between gain and stability margins.

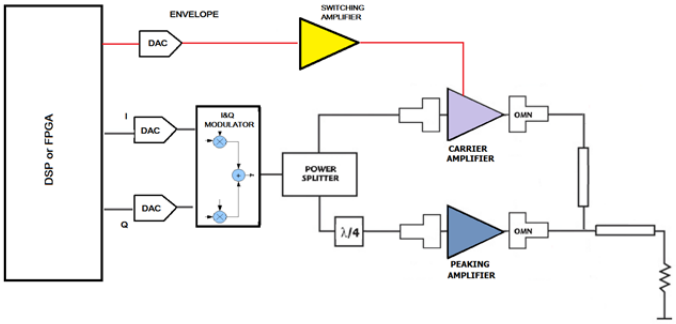


Fig.6. DPA with drain modulation

The design of the bias could be also considered as an alternative (or complement) to the uneven power drive. As stated above, the objective of the uneven power drive is to deliver more RF input power to the PkA rather than to the main. This fact allows the generation of enough current to the PkA to achieve a proper load modulation. This additional current may be also obtained and regulated by using different bias values. Additionally, the use of different biasing voltages for the CA and the PkA [20] should solve a usual drawback in the Doherty gain, which is the low gain performance.

In [14] the bias circuit is designed by also considering the minimization of the memory effects, trying to prevent the frequency dispersion even in the envelope impedance. The way to do that has been to reproduce, for all frequencies, the classical biasing structure composed by a quarter-wave line followed by decoupling capacitors, and inserting tantalum capacitors for also decoupling at the envelope frequencies. ACRL results better than -40 dBc at low and medium powers, rising to -30 dBc at high power. Compared with a power inefficient class-AB amplifier at the same operating conditions, the ACLR improvement is of the order of 4-6 dB.

In adaptive bias the idea is to increase linearity and efficiency by continuously modifying the gate voltage (and sometimes also the drain voltage) of the CA, the PkA, or both. The adaptive structure remembers the one of the EER, in this case with the envelope power levels controlling the gate bias voltage instead of the drain voltage.

In [21] the adaptive bias is applied to the PkA, being fixed the bias of the CA. The gate adaptation function is performed in DSP by using a mapping function. Below the break point, the gate voltage is constant. Above the transition point, a time-varying voltage is applied to the gate by using a mapping function which basically assures a minimum bias voltage that is enlarged according to a cubic polynomial which depends on the instantaneous envelope amplitude. This bias adaptation reduces around 10-15 dB the IMD3 component, and the ACLR is reduced by 3-5 dB at high power (no effects at low power). Similar experimentation and results are reported in [22].

A different approach may be found in [23], where the equation for the Statz model of the FET saturation drain current is used to compute the bias control according to input drive voltages. The adaptation is applied to both amplifiers.

What is presented in [24] is a dual bias control, where both the gate and drain voltages of the CA are continuously adjusted according to the input power level. Additionally, the linearity is improved by removing the 2nd harmonic using an

additional PBG (Photonic Band-Gap) structure as an offset-line, showing high return losses at harmonic frequencies. At 24.09 dBm, and with an efficiency of 36.28%, an IMD3 characteristic of -32.47 dBc is reported.

6) Use of linearizers in DPA

A 250W DPd based linearized DPA for GSM applications in the 1900 MHz band is reported in [25]. Results show a spectral regrowth ranging from 60 to 75 dB, being the efficiency over 45 % at maximum power for a single carrier GSM signal (5% of efficiency reduction for two-carriers).

In [26] a static gain postdistorter is experimented over a 22dBm DPA at the 40 GHz band, and a IMD3 reduction of 18 dB is reported. In [27] a DPD compensates both memoryless nonlinearities and low-level memory effects in a 100W DPA centered at 2.14 GHz. In a WCDMA waveform, the compensation of both effects reduces the ACLR in 30 dB, while the sole compensation of the memoryless nonlinearities produces a reduction of 24 dB. What is presented in [28] is a summary of different works where a DPA has been linearized by using a DPD. ACLR reductions because of the DPD operation range from 8 to 35 dB. And in [29] it is shown a technique based on a capacitor loaded to the CA quarter-wave line to increase linearity by compensating phase delays.

7) Broadband techniques

The need for higher BW in DPA is evident in multicarrier applications. For a single carrier, the typical 5-10% of fractional BW is enough for new solutions, including Advanced LTE (40 MHz). However, in multicarrier power stations, this improvement should be considered. Different approaches to the BW increase have been experimented. The *real frequency technique* that employs a nonlinear optimization simulator for the optimum matching over a given frequency band has been used in [30]. Other works reduces the Q-factor of the matching networks (or transmission lines), thus increasing the BW. A fractional BW of 35% is obtained in [31] by modifying the reflection coefficient of the transmission line (impedance inverter in the CA). In [32] a stepped impedance transformer (Vizmuller topology) in employed instead of the classical quarter-wave transformer, achieving a 12% of fractional BW.

IV. Conclusion

After a brief introduction of the DPA fundamentals, a review of the state of the art regarding design issues and solution approaches has been presented.

Acknowledgment

This work was supported by the Ministerio de Ciencia e Innovación (Spain), under grant TEC2011-29126-C03-02.

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