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Tunable active inductor-based second-order all-pass filter as a time delay cell for multi-GHz operation

Seyed Rasoul Aghazadeh · Herminio Martinez · Alireza Saberkari · Eduard Alarcon

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Abstract In this paper, a CMOS wide-band second-order voltage-mode all-pass filter as a time delay cell is proposed. The proposed all-pass filter is made up of solely two transistors as active elements and four passive components. This filter demonstrates a group delay of approximately 60 ps within a bandwidth of 5 GHz, achieving maximum delay-bandwidth-product (DBW). The proposed circuit is highly linear and has an input-referred 1-dB compression point P_{1dB} of 2 dBm. The power consumption of the proposed circuit is only 10.3 mW. On the other hand, an active inductor is employed in the all-pass filter instead of a passive RLC tank, thereby the three passive components are eliminated, in order to tune the time delay and improve the size. In this case, even though the power consumption increases, the time delay can be controlled across an improved bandwidth of approximately 10 GHz. Moreover, the circuit demonstrates a 1-dB compression point P_{1dB} of 18 dBm. The proposed all-pass filter is simulated in TSMC 180-nm CMOS process parameters.

Keywords All-pass filter · Delay · Wide-band · Delay-bandwidth-product · Linearity · Active inductor

S.R. Aghazadeh
Diagonal-Besòs Campus, Eastern Barcelona School of Engineering (EEBE), Eduard Maristany Avenue, $n^o 10 - 14E - 08019$, Barcelona, Spain
Tel.: +34-934137290
Fax: +34-934137401
E-mail: rasoul.aghazadeh@upc.edu

S.R. Aghazadeh · H. Martinez · E. Alarcon
Technical University of Catalonia−BarcelonaTech (UPC)

A. Saberkari
University of Guilan

1 Introduction

All-pass filters as delay stages have a large variety of applications and have been utilized in many different radio frequency (RF) and phase shift circuits like synchronizing ultra-wideband (UWB) impulse radios with locally generated reference pulses, equalizers, and analog/RF beamformers [1–4]. There are several both current- and voltage-mode all-pass filters in the literature [5–7], using one or more operational voltage or current amplifiers. Whereas, these filters suffer from low bandwidth due to the presence of high impedance nodes and have therefore low operating frequencies.

All-pass-filter-based time delays demonstrate better performance in terms of area-efficiency and loss than approaches relying on transmission lines or lumped LC delay lines, since these circuits occupy larger areas and are impractical for on-chip implementations. As a consequence, lots of delay stages, e.g., wide-band RF analog beamformers, realized by using all-pass-filter-based delay approximations, have been recently studied [8, 9]. Many reported delay stages are normally realized by cascading first-order all-pass filters, e.g., gm-(R)C filters, and these circuit topologies, however, suffer from limited bandwidths about up to 2.5GHz [9, 10]. As a suitable alternative, second-order all-pass filters can therefore be main components for realization of delay structures with nanosecond delay. Generally, high-order rational all-pass filters can be divided into several second-order all-pass filters with complex-conjugate poles and first-order all-pass filters. Most conventional reported wide-band second-order all-pass filters employed one or two passive inductors which are bulky, occupying a large area [11–14]. Among all, only the filter in [13] was capable of tuning time delay by using varactor diodes, since tunability is a good feature of signal processing and communication circuits, e.g., in phase shifters and beamformers.

This paper introduces a CMOS RF second-order all-pass filter which utilizes an active inductor, thereby not only time delay can be tuned but also the overall size will be reduced considerably compared with the conventional circuits. The proposed all-pass filter employs Padé approximation, approximating accurately to an ideal delay and demonstrating a flat group delay through a wide frequency range [11, 12]. To achieve maximum delay-bandwidth-product (DBW), a second-order all-pass filter using Padé technique is thus a better candidate than the cascade of two first-order all-pass filters for realization of a second-order delay circuit.

This paper is structured as follows. Section 2 presents the proposed all-pass filter and determines theoretical analyses. In Sect. 3, the tunability of the proposed second-order all-pass filter is provided. Simulation results are given in Sect. 4. Section 5 provides conclusions.

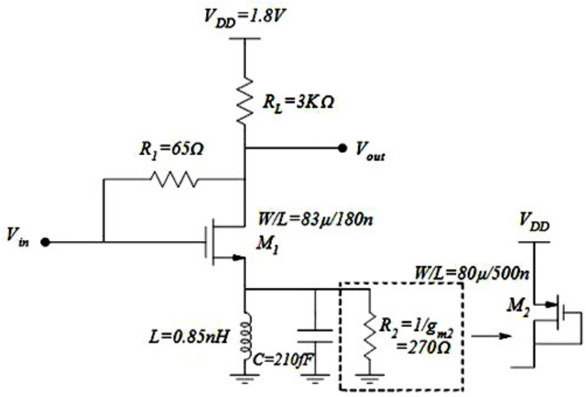

Fig. 1 Proposed second-order voltage-mode all-pass filter

2 Proposed second-order all-pass filter

The ideal transfer function of a second-order all-pass filter utilizing Padé approximation is expressed by

$$H(s) = \frac{s^2 - \frac{\omega_n}{Q}s + \omega_n^2}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \tag{1}$$

where ω_n is the natural frequency and Q is the quality factor of the all-pass filter. By changing the values of ω_n and Q, the position of poles and zeros in the complex plane is controlled and determined.

2.1 Circuit design

The proposed wide-band second-order all-pass filter as a time delay cell is indicated in Fig. 1. Assuming that $g_{m1,2} \gg g_{ds}$ and ignoring the parasitics of the transistors, the transfer function of the proposed second-order all-pass filter can be defined as

$$\frac{V_{out}}{V_{in}}(s) = -\frac{R_L(g_{m1}R_1 - 1)}{R_L + R_1} \cdot \frac{s^2 - \frac{1}{C}\left(\frac{g_{m1}+g_{m2}-g_{m1}g_{m2}R_1}{g_{m1}R_1-1}\right)s + \frac{1}{LC}}{s^2 + \frac{1}{C}(g_{m1}+g_{m2})s + \frac{1}{LC}} \tag{2}$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2, respectively. If the following conditions are satisfied:

$$g_{m1}R_1 = 2 \tag{3a}$$

$$R_L \gg R_1 \tag{3b}$$

$$g_{m1} + g_{m2} \gg g_{m1}g_{m2}R_1 \tag{3c}$$

an all-pass structure will be realized with the same frequencies of the left-plane poles and right-plane zeros, resulting in twice the phase and group delay responses of an all-pass circuit. Therefore, the transfer function in (2) can be rewritten as

$$\frac{V_{out}}{V_{in}}(s) \cong -\frac{s^2 - \frac{1}{C}(g_{m1}+g_{m2})s + \frac{1}{LC}}{s^2 + \frac{1}{C}(g_{m1}+g_{m2})s + \frac{1}{LC}}. \tag{4}$$

From (4), the natural frequency and quality factor of the proposed second-order all-pass filter are determined, respectively, as

$$\omega_n = \frac{1}{\sqrt{LC}} \tag{5}$$

$$Q = \frac{1}{g_{m1}+g_{m2}}\sqrt{\frac{C}{L}}. \tag{6}$$

The voltage gain of the all-pass filter is -1 at low frequencies, as the capacitor C and inductor L are considered as an open-circuit and sort-circuit, respectively. At high frequencies, the capacitor C shorts the source terminal of M_1 to ground and, hence, a voltage gain equal to -1 is obtained again. The pole/zero frequencies and phase response of the second-order all-pass filter can be expressed, respectively, by

$$|\omega_{p1,2}| = |\omega_{z1,2}| = \frac{L(g_{m1}+g_{m2}) \pm \sqrt{L^2(g_{m1}+g_{m2})^2 - 4LC}}{2LC} \tag{7}$$

$$\varphi(\omega) = -2\ tan^{-1}\left[L(g_{m1}+g_{m2}) \cdot \frac{\omega}{1-LC\omega^2}\right] \tag{8}$$

and, thus, group delay response is given as

$$\tau_g(\omega) = -\frac{\partial\varphi(\omega)}{\partial\omega} = 2L(g_{m1}+g_{m2}) \cdot \frac{1+LC\omega^2}{(1-LC\omega^2)^2 + ((g_{m1}+g_{m2})L\omega)^2} \tag{9}$$

where ω is the angular frequency. From (9), note that, the group delay is equal to $2Lg_{m1}$ at low frequencies and g_{m2} (i.e., $R_2 = 1/g_{m2}$) will be neglected, since the inductor L shorts the source of M_1 to ground at DC. At high frequencies, the resistor R_2 can be regarded as a source degeneration resistor, contributing to the linearity of the circuit.

When $Q < 0.5$, the all-pass filter has two real poles in the left-half plane, while for $Q > 0.5$ a complex conjugate pole-pair appears. When $Q = 1/\sqrt{3}$, the maximum flat delay will be achieved and Padé approximation is matched and, therefore, DBW will be guaranteed [11]. It can be noted that, the circuit can achieve larger delay over a wider bandwidth by choosing appropriate g_m, L, and C (low transconductance and small values of L and C) compared to the gm-(R)C filters, since the natural frequency of the proposed filter is $1/\sqrt{LC}$.

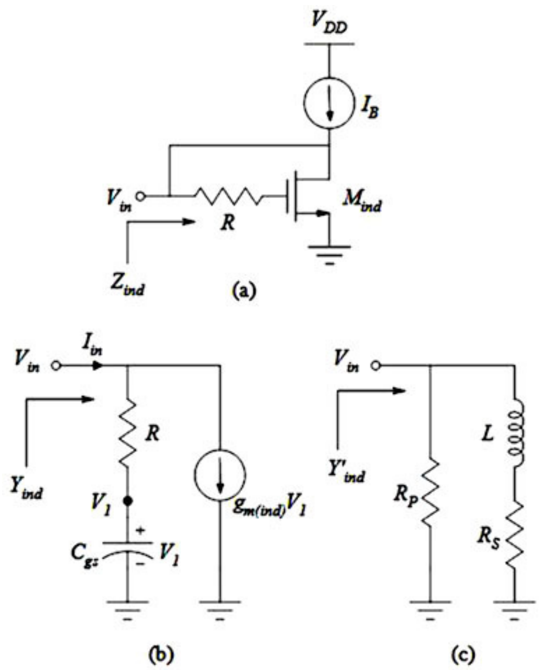

Fig. 2 (a) Active inductor and, (b) and (c) its equivalent models

2.2 Non-ideality consideration

We will now consider the effects of parasitic capacitors C_{gs} and C_{gd} on the performance of the proposed all-pass filter in Fig. 1. The parasitic pole stemmed from C_{gd} is almost equal to $1/R_1C_{gd}$. From (3), the value of resistor R_1 should be small. Hence, the effect of C_{gd} can be neglected, as its parasitic pole will be far beyond the dominant poles/zeros. Therefore, C_{gs} can be only assessed for the evaluation. Considering finite output impedance of M_1 and C_{gs} which affect the pole/zero frequencies and DC-gain, the transfer function of the second-order all-pass filter is given as

$$\frac{V_{out}}{V_{in}}(s) = -\frac{CR_L(g_{m1}R_1 - 1) - C_{gs}R_L(1 + R_1g_{ds})}{(C + C_{gs})(R_1 + R_L + g_{ds}R_1R_L)} \cdot \frac{s^2 - \left[\frac{(g_{m1}+g_{m2}+g_{ds})(1+R_1g_{ds})-(g_{m2}+g_{ds})(R_1(g_{m1}+g_{ds}))}{C(g_{m1}R_1-1)-C_{gs}(1+R_1g_{ds})}\right] s + \frac{g_{m1}R_1-1}{LC(g_{m1}R_1-1)-LC_{gs}(1+R_1g_{ds})}}{s^2 + \left[\frac{(g_{m1}+g_{m2}+g_{ds})(R_1+R_L)+g_{m2}g_{ds}R_1R_L}{(C+C_{gs})(R_1+R_L+g_{ds}R_1R_L)}\right] s + \frac{1}{L(C+C_{gs})}} \tag{10}$$

where g_{ds} is the output conductance of M_1. If $g_{m1,2} \gg g_{ds}$ and the conditions in (3) are satisfied, the transfer function can be rewritten as

$$\frac{V_{out}}{V_{in}}(s) \cong -\frac{C - C_{gs}}{C + C_{gs}} \cdot \frac{s^2 - \frac{g_{m1}+g_{m2}}{C-C_{gs}}s + \frac{1}{L(C-C_{gs})}}{s^2 + \frac{g_{m1}+g_{m2}}{C+C_{gs}}s + \frac{1}{L(C+C_{gs})}}. \tag{11}$$

As it can be observed, for $C \gg C_{gs}$, (4) and (11) will be the same. Further analysis shows that C_{gs} creates variations on the gain and group delay responses at high frequencies. Whereas, these variations can be adjusted by varying the resistor R_2 in the proposed all-pass filter. This will be discussed in Sect. 4.

3 The tunability of the proposed second-order all-pass filter

An active inductor can be an attractive option for tuning time delay in the proposed second-order all-pass filter, since they offer a variety of advantages, e.g., small chip area, large and tunable inductance value and self-resonant frequency, and also compatibility with standard CMOS technology [15].

3.1 Active inductor

Fig. 2(a) shows a one-port grounded active inductor [16,17], which is used in the proposed second-order all-pass filter. Assuming for simplicity that $g_{m(ind)} \gg g_{ds(ind)}$, the input admittance of the active inductor, i.e., $Y_{ind}(= 1/Z_{ind})$, can be easily obtained by using its small signal equivalent circuit shown in Fig. 2(b) as

$$Y_{ind} = \frac{sC_{gs} + g_{m(ind)}}{sRC_{gs} + 1} = \frac{1}{R} + \frac{1}{s\frac{R^2C_{gs}}{Rg_{m(ind)}-1} + \frac{R}{Rg_{m(ind)}-1}} \tag{12}$$

where the pole and zero frequencies of the input admittance are $\omega_p = g_{m(ind)}/C_{gs}$ and $\omega_z = 1/RC_{gs}$, respectively. The active inductor exhibits an inductive behavior in the frequency range of $\omega_z < \omega < \omega_p$.

The input admittance achieved in (12) can therefore be modeled by a parallel RL circuit, which is shown in Fig. 2(c) as

$$Y'_{ind} = G_P + \frac{1}{sL + R_S} \tag{13}$$

where $G_P = 1/R_P$ is determined as parallel and R_S as series resistance with inductor L. From (12) and (13), the parameters of the RL equivalent circuit can be expressed by

$$R_P = R \tag{14a}$$

$$L = \frac{R^2C_{gs}}{Rg_{m(ind)} - 1} \tag{14b}$$

$$R_S = \frac{R}{Rg_{m(ind)} - 1}. \tag{14c}$$

Note that, the R_P is here a passive resistor which by varying its value, the L and R_S will change accordingly as well. Moreover, the values of L and R_S will change with the frequency, since they are active elements.

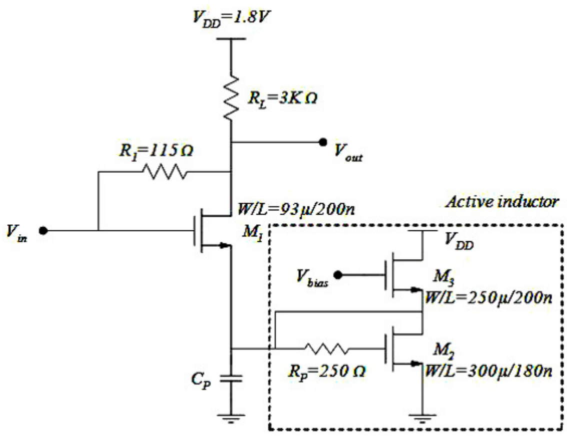

Fig. 3 Proposed second-order voltage-mode active inductor-based all-pass filter

3.2 Proposed all-pass filter employing an active inductor

Fig. 3 illustrates the proposed all-pass filter exploiting an active inductor in order to tune the delay, and to that end, we replaced the active inductor shown in Fig. 2(a) with the parallel RLC circuit in Fig. 1. Capacitor $C_P = C_{sb1} + C_{db2} + C_{gs3} + C_{sb3}$ is the total parasitic capacitances at the source terminal of M_1, depending on MOSFET technology, transistor size, and frequency. Therefore, the overall area can be improved, as there is not any passive capacitor at this node. The new transfer function of the proposed circuit is determined by

$$\frac{V_{out}}{V_{in}}(s) = -\frac{R_L(g_{m1}R_1 - 1)}{R_L + R_1}\cdot \frac{s^2 - \left[\frac{g_{m1}R_PL+L+C_PR_PR_S-g_{m1}R_1(L+C_PR_PR_S)}{LC_PR_P(g_{m1}R_1-1)}\right]s + \frac{(g_{m1}R_1-1)(R_P+R_S)-g_{m1}R_PR_S}{LC_PR_P(g_{m1}R_1-1)}}{s^2 + \left[\frac{g_{m1}R_PL+L+C_PR_PR_S}{LC_PR_P}\right]s + \frac{g_{m1}R_PR_S+R_P+R_S}{LC_PR_P}}. \tag{15}$$

If $L + C_PR_PR_S \ll g_{m1}R_PL$, $g_{m1}R_S \ll 1$, and conditions in (3a)-(3b) are satisfied, the transfer function can be rewritten as

$$\frac{V_{out}}{V_{in}}(s) \cong -\frac{s^2 - (\frac{g_{m1}}{C_P})s + \frac{1}{LC_P}}{s^2 + (\frac{g_{m1}}{C_P})s + \frac{1}{LC_P}} \tag{16}$$

which is nearly the same as that in (4).

4 Simulation results

The proposed second-order all-pass filter is designed in 180nm TSMC CMOS parameters and simulation is performed using HSPICE and Virtuoso Cadence.

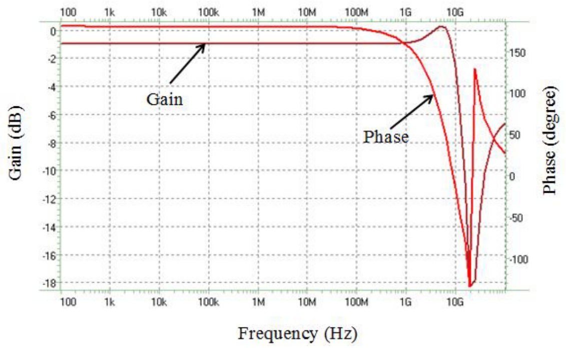

Fig. 4 Gain and phase responses of the proposed second-order all-pass filter

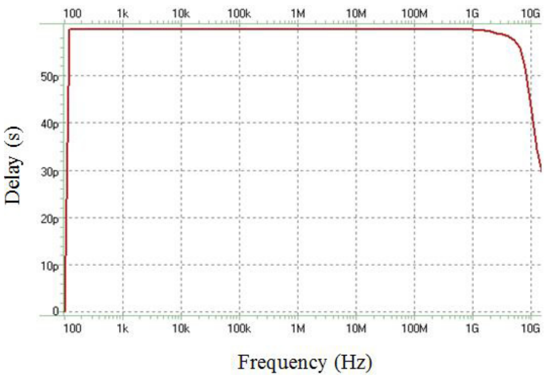

Fig. 5 Group delay response of the proposed second-order all-pass filter

We will simulate both the proposed second-order all-pass filters depicted in Figs. 1 and 3, without and with active inductor respectively, to demonstrate their overall performance. First, the proposed circuit shown in Fig. 1 is simulated with $g_{m1} = 31.5\text{mA/V}$, $g_{m2} = 3.7\text{mA/V}$, and $Q = 1/\sqrt{3}$ (for maximum DBW). This proposed filter consumes only 10.3mW power.

In Fig. 4 the gain and phase responses of the second-order all-pass filter (without active inductor) are shown. The gain roll-off is due to the existence of parasitic effects of the transistors and also due to the fact that the DC gain of the all-pass filter is less than unity (refer to (2)). The group delay response of the proposed all-pass filter is shown in Fig. 5, indicating a flat group delay equal to 59.8ps over an approximately 5GHz bandwidth, which is very close to the theoretical value in (9) with an error of about 11.5%. Fig. 6 shows the gain and group delay responses of the second-order all-pass filter under different values of $R_2 (= 1/g_{m2})$. It is obvious that by varying g_{m2}, flat gain and group delay responses are achieved at higher frequencies, and implies that g_{m2} is proportional to the group delay (refer to (9)).

The input-referred noise response of the proposed second-order all-pass filter is shown in Fig. 7, demonstrating an input-referred noise of around

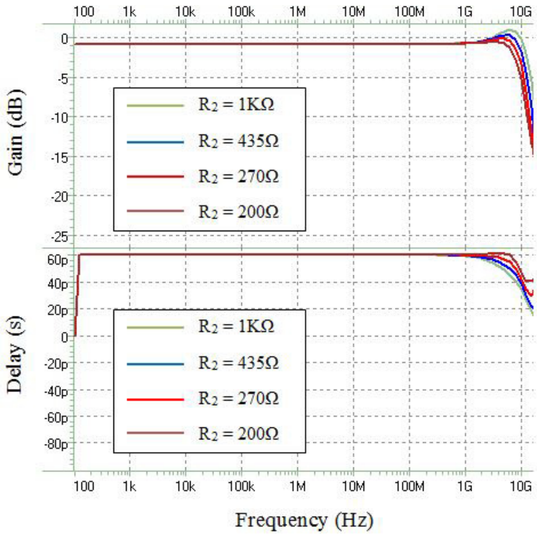

Fig. 6 Gain and group delay responses of the proposed second-order all-pass filter for different values of $R_2 = 1/g_{m2}$

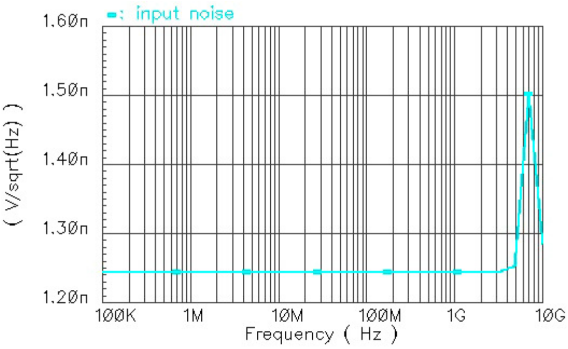

Fig. 7 Input-referred noise response of the proposed second-order all-pass filter

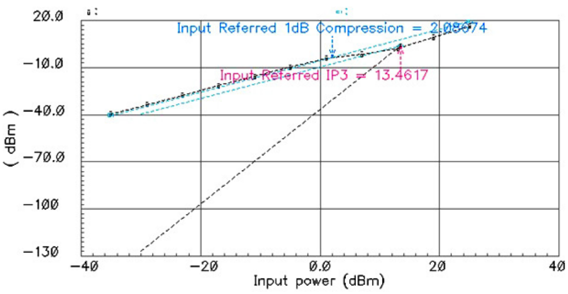

Fig. 8 Input-referred P_{1dB} and input-referred IIP3 responses of the proposed second-order all-pass filter

Table 1 The performance summary of the simulated second-order all-pass filter without active inductor

Technology	Mode	Number of L	Bandwidth (GHz)	Delay (ps)	P_{1dB} (dBm)	IIP3 (dBm)	Power (mW/V)
180 nm	Voltage	1	5	60	2	13.5	10.3/1.8

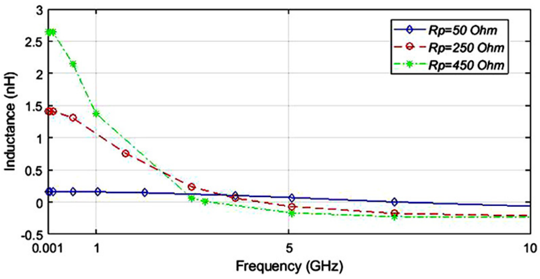

Fig. 9 Simulated inductance under different values of R_P in active inductor

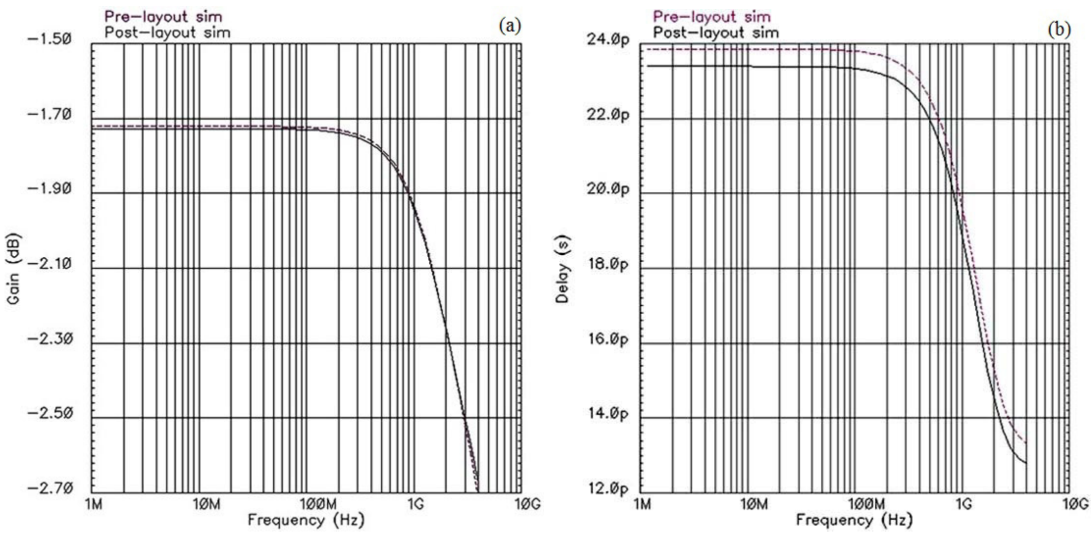

Fig. 10 Pre- and post-layout simulation results for (a) gain response and (b) group delay response of the proposed second-order all-pass filter with active inductor

1.25nV/sqrt(Hz) by the frequency of 3GHz. The input-referred 1-dB compression point (P_{1dB}) and input-referred third-order intercept point (IIP3) responses of the proposed second-order all-pass filter are shown in Fig. 8. The input-referred P_{1dB} and IIP3 are approximately 2dBm and 13.5dBm at 5GHz, respectively. The main reason of this high linearity of the proposed all-pass filter is the high drain current of M_2 at the price of higher power consumption.

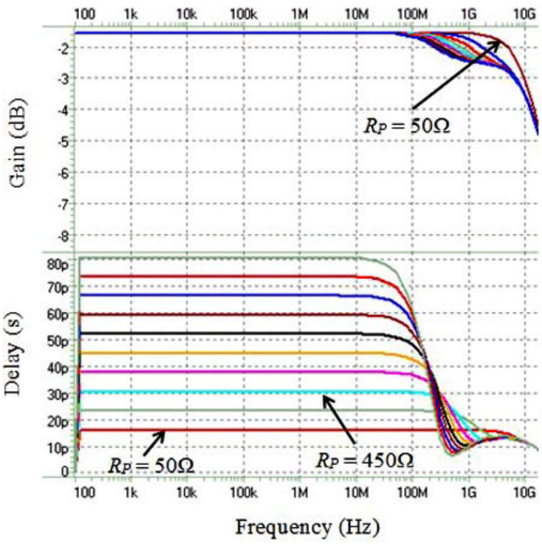

Fig. 11 Gain and group delay responses of the proposed second-order all-pass filter with active inductor for different values of R_P ($50\Omega \sim 1.85K\Omega$)

Table 1 summarizes the performance of the proposed second-order all-pass filter shown in Fig. 1.

Finally, the proposed all-pass filter using an active inductor shown in Fig. 3 is simulated with g_{m1} = 18mA/V and g_{m2} = 117mA/V. The transconductance of the active inductor ($g_{m2} = g_{m(ind)}$) is considered large enough to lower down the values of L and R_S (refer to (14)), improving the linearity of the circuit, however the overall power consumption will increase. The active inductor-based all-pass filter consumes around 33.3mW power from a 1.8V supply voltage. The value of resistor R_S (see Fig. 2) is very small and, therefore, can be ignored. From (14c) and $R_P = 250\Omega$, we find $R_S = 8.8\Omega$. To find the value of active inductance L, we simulated only the active inductor (the part inside the dotted box) shown in Fig. 3 with the same parameters required as the entire circuit. Fig. 9 shows this simulated inductance L for different values of R_P.

Pre- and post-layout simulation results for the gain and group delay responses of the proposed active inductor-based all-pass filter with $R_P = 250\Omega$ are shown in Fig. 10, indicating small differences in the obtained responses. As shown, the value of group delay for the post-layout simulation is nearly 23.4ps. The gain and group delay responses of the proposed circuit under different values of R_P (R_P is swept between $50\Omega \sim 1.85K\Omega$ with the steps of 200Ω), which are based on typical case are shown in Fig. 11. As it can be seen, delay can be tuned (fine-tuned) over an improved frequency range up to around 10GHz by varying the passive resistor R_P. The fine-tuning can be easily performed by a binary weighted resistor bank (switched-resistors) instead of the R_P in Fig. 3. In Fig. 12, the post-layout input-referred noise response

Table 2 Performance comparison between wide-band second-order all-pass filters

Reference	Technology	Mode	Number of L	Bandwidth (GHz)	Delay (ps)	P_{1dB} (dBm)	IIP3 (dBm)	Power (mW/V)
[11]/Sim.	–	Voltage	2	10	60	–	–	–
[12]/Sim.	130 nm	Current	1	10	60	−1.5	–	16.5/1.5
[13]/Meas.	*SiGe2RF* HBT	Voltage	2	3−10	75	−1	–	38.8/2.5
[14]/Meas.	130 nm	Voltage	1	6	55	−5.5	2	18.5/1.5
[18]/Meas.	180 nm	Voltage	0	3−12	6	14.6	22.6	12/1.8
This work /Post sim.	180 nm	Voltage	0	10	Fine-tuning	18	22.7	33.3/1.8

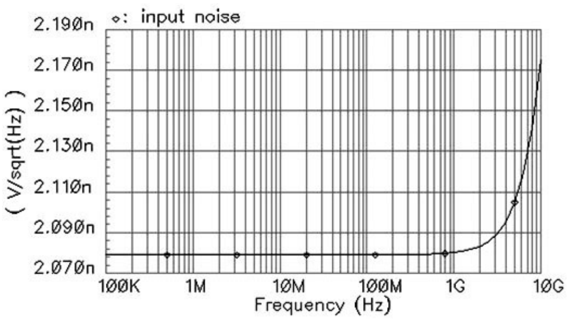

Fig. 12 Post-layout input-referred noise response of the proposed second-order all-pass filter with active inductor

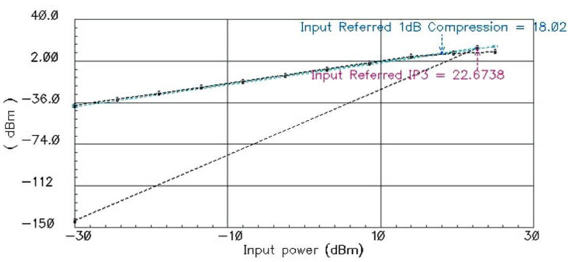

Fig. 13 Post-layout input-referred P_{1dB} and input-referred IIP3 responses of the proposed second-order all-pass filter with active inductor

of the proposed all-pass filter is shown, which indicates an input-referred noise of nearly 2.1nV/sqrt(Hz) by the frequency of 1GHz, with $R_P = 250\Omega$. The post-layout input-referred P_{1dB} and IIP3 responses of the proposed circuit are shown in Fig. 13. The input P_{1dB} and IIP3 are 18dBm and 22.67dBm at 500MHz with $R_P = 250\Omega$, respectively.

Table 2 compares the proposed second-order voltage-mode active inductor-based all-pass filter with some other reported wide-band second-order circuits. As it can be observed, the proposed all-pass filter demonstrates a higher lin-

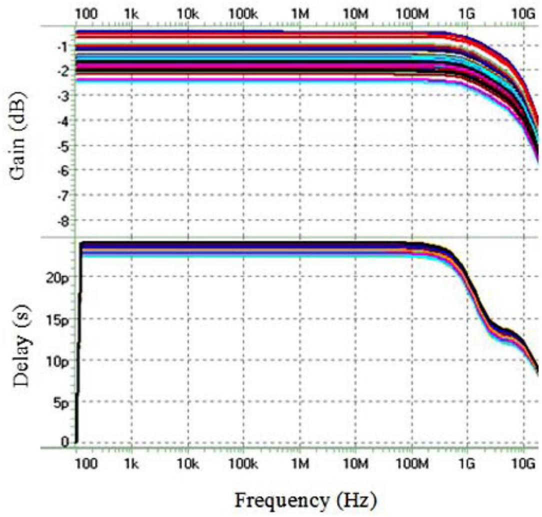

Fig. 14 Monte Carlo simulation results for (a) gain response and (b) group delay response of the proposed second-order all-pass filter with active inductor

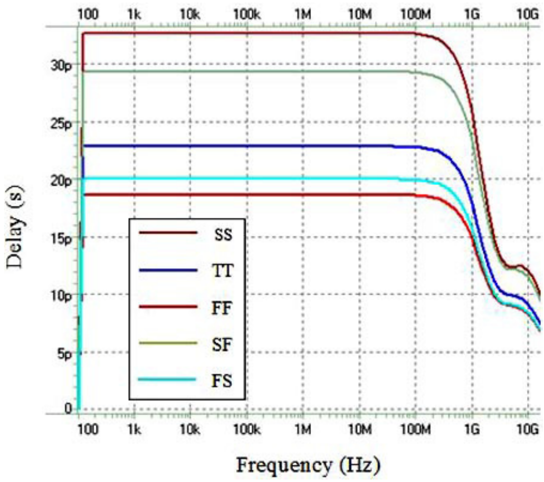

Fig. 15 Corner analysis results for group delay response of the proposed second-order all-pass filter with active inductor

earity than the other filters. Moreover, there is not any passive inductor, which is bulky and area-consuming, in the proposed filter compared to the circuits using one or two passive inductors. It can also be mentioned that the proposed filter is capable of achieving more delay over a wider frequency range (see Fig. 11) than the filter in [18], however at a higher power consumption.

For further analysis, Monte Carlo and corner analyses are carried out on the circuit in Fig. 3 and results are shown in Figs. 14 and 15 respectively, with $R_P = 250\Omega$. The Monte Carlo simulation results are performed with a Gaus-

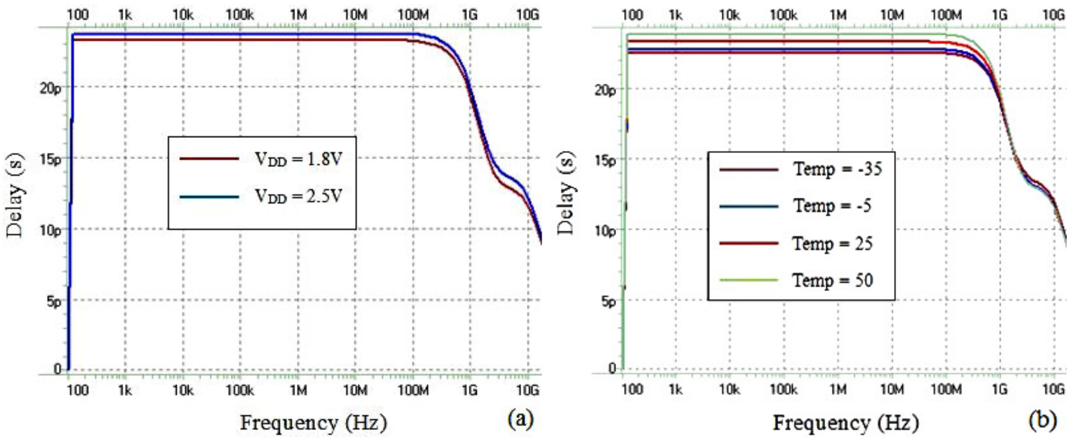

Fig. 16 Group delay responses of the proposed second-order all-pass filter with active inductor for (a) different supply voltages and (b) different temperatures

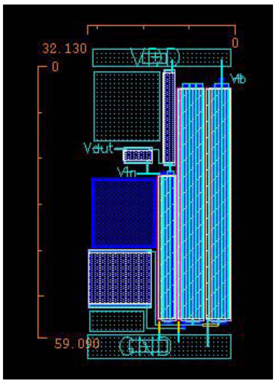

Fig. 17 Layout of the proposed second-order all-pass filter with active inductor

sian distribution and 50 iterations, which are based on typical case. In this case, maximum variation on the group delay of the proposed all-pass filter over the frequency band due to the mismatch is just 4.8%. Since process, voltage, and temperature (PVT) variations may affect the gain and thus the group delay response, the proposed active inductor-based all-pass filter is simulated under these variations. Fig. 16 indicates the group delay responses under different supply voltages and temperatures, with $R_P = 250\Omega$. As shown, the obtained responses due to PVT have small differences. Fig. 17 shows the layout of the proposed second-order voltage-mode active inductor-based all-pass filter. The core area is approximately $32\mu\text{m}\times59\mu\text{m}$.

5 Conclusion

This paper presents a tunable wide-band second-order voltage-mode all-pass filter as a time delay cell. The proposed all-pass filter shows a flat group delay of 60ps over a 5GHz bandwidth, which achieves maximum delay-bandwidth-product (DBW). This filter consumes only 10.3mW power and proves a higher linearity than the other published second-order all-pass filters using just one grounded inductor. Additionally, an active inductor is utilized in order to control the time delay of the proposed second-order all-pass filter and to decrease the overall area. In this condition, the proposed active-inductor-based all-pass filter consumes around 33.3mW power, while its time delay is varied for different values of tunable resistor in the active inductor. The proposed filter achieves an input-referred 1-dB compression point P_{1dB} of 18dBm.

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References

1. Schwartz, J., Arnedo, I., Laso, M., Lopetegi, T., Azana, J., Plant, D.: An electronic UWB continuously tunable time-delay system with nanosecond delays. IEEE Microw. Wireless Compon. Lett. 18, 103-105 (2008)
2. Buckwalter, J., Hajimiri, A.: An active analog delay and the delay reference loop. in Proc. IEEE RFIC Symp. Dig. (2004), pp. 17-20
3. Gurun, G., Zahorian, J.S., Sisman, A., Karaman, M., Hasler, P.E., Degertekin, F.L.: An analog integrated circuit beamformer for high frequency medical ultrasound imaging. IEEE Trans. Biomedical Circuits Syst. 6, 454-467 (2012)
4. Liu, W., Weiss, S.: Wideband Beamforming Concepts and Techniques. John Wiley and Sons, New York (2010)
5. Toker, A., Ozoguz, S., Cicekoglu, O., Acar, C.: Current-mode allpass filters using current differencing buffered amplifier and a new high-Q bandpass filter configuration. IEEE Trans. Circuits Syst. 47, 949-954 (2000)
6. Cakir, C., Cam, U., Cicekoglu, O.: Novel allpass filter configuration employing single OTRA. IEEE Trans. Circuits Syst. II: Express Briefs 52, 122-125 (2005)
7. Chang, C.M.: Current mode allpass/notch and bandpass filter using single CCII. Electron. Lett. 27, 1812-1813 (1991)
8. Wijenayake, C., Xu, Y., Madanayake, A., Belostotski, L., Bruton, L.: RF analog beamforming fan filters using CMOS all-pass time delay approximations. IEEE Trans. Circuits Syst. I: Regular Papers 59, 1061-1073 (2012)
9. Garakoui, S.K., Klumperink, E.A.M., Nauta, B., van Vliet, F.E.: Compact cascadable gm-C all-pass true time delay cell with reduced delay variation over frequency. IEEE J. Solid-State Circuits 50, 693-703 (2015)
10. Garakoui, S.K., Klumperink, E.A.M., Nauta, B., van Vliet, F.E.: Frequency limitations of first-order gm-RC all-pass delay circuits. IEEE Trans. Circuits Syst. II: Express Briefs 60, 572-576 (2013)
11. Zhou, L., Safarian, A., Heydari, P.: CMOS wideband analogue delay stage. Electron. Lett. 42, 1213-1214 (2006)
12. Ahmadi, P., Taghavi, M.H., Belostotski, L., Madanayake, A.: 10-GHz current-mode 1st-and 2nd-order allpass filters on 130nm CMOS. in Proc. IEEE Int. Midwest Symp. Circuits Syst. (MWSCAS) (2013), pp. 1-4
13. Ulusoy, A., Schleicher, B., Schumacher, H.: A tunable differential all-pass filter for uwb true time delay and phase shift applications. IEEE Microw. Wireless Compon. Lett. 21, 462-464 (2011)

14. Ahmadi, P., Maundy, B., Elwakil, A.S., Belostotski, L., Madanayake, A.: A new 2nd-order all-pass filter in 130-nm CMOS. IEEE Trans. Circuits Syst. II: Express Briefs 63, 249-253 (2016)
15. Saberkari, A., Ziabakhsh, S., Martinez, H., Alarcon, E.: Active inductor-based tunable impedance matching network for RF power amplifier application. Integr. VLSI J. 52, 301-308 (2016)
16. Carreto-Castro, F., Silva-Martinez, J., Murphy-Arteaga, R.: RF low-noise amplifiers in BiCMOS technologies. IEEE Trans. Circuits Syst. II: Analog Digital Signal Process. 46, 974-977 (1999)
17. Saberkari, A., Kazemi, Sh., Shirmohammadli, V., Yagoub, M.C.E.: Gm-boosted flat gain UWB low noise amplifier with active inductor-based input matching network. Integr. VLSI J. 52, 323-333 (2016)
18. Chen, Y., Li, W.: An ultra-wideband pico-second true-time-delay circuit with differential tunable active inductor. Analog Integr. Circuits Signal Process. 91, 9-19 (2017)