Voltage Balancing of a Five-level Flying Capacitor Converter Using Optimum Switching Transitions

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***Abstract*- The flying capacitor (FC) multilevel converter has attracted quite significant attention in the recent years. One of the reasons is because it is easier to extend the topology to a high number of levels (n>3) when compared to its counterpart, namely the diode-clamped converter (DCC). This is due to the difficulties of achieving capacitor voltage balance for the DCC. On the other hand, the voltages in the capacitors of the FC converter can be controlled due to the availability of redundant switching states. The main focus of this paper is to develop a voltage balancing scheme for a five-level FC converter based on phase disposition pulse-width modulation (PD-PWM) using transitions that produce the minimum number of switching events. This strategy will be called optimal-transition voltage balancing (OTVB) scheme. Since there are multiple optimum switching transitions between two consecutive voltage levels, such a redundancy is used to regulate the FC voltages at their desired levels. The selection of the optimal transition sequence is performed by minimizing a cost function. Those transitions that produce much more switching events are avoided in the proposed modulation scheme. The simulation results show a significant reduction of the average switching frequency as compared to the use of the optimal-state voltage balancing (OSVB) scheme, while maintaining the balance of the FC voltages. Moreover, the proposed PD-PWM voltage balancing strategy is robust to static and dynamic loading conditions.**

I. INTRODUCTION

Due to recent advances in semiconductor devices, the interest of using voltage source converters (VSCs) have significantly increased for high power/voltage applications [1]. However, the conventional two-level VSC fails to meet optimum system performance and efficiency such as filter size, losses, total harmonic distortion (THD), etc. The solution to improve the performance and efficiency for high voltage systems is to use multilevel VSCs that allow high power handling capability with reduced harmonics and lower switching losses [2]. Among the multilevel converter topologies, the most popular ones are the cascaded multi-modular converter [3], the diode-clamped converter (DCC) [4] and the flying capacitor (FC) converter [5]. The three-level DCC is also known as neutral-point-clamped (NPC) converter.

The main challenge associated with multilevel converters is the voltage balancing of the individual capacitors. Although the NPC topology has been widely used by industry, the main issue with this topology is the proper regulation of the neutral-point (NP) potential. The NP voltage maintains balance in the steady state as long as the average current injected into the NP is zero. Yet, still some current deviations may be seen when looking over a switching period; hence appearing some low-frequency NP voltage oscillations. Some modulation strategies can avoid such ripples [6], but they increase the switching frequency in the power devices and the distortion in the output voltages. Furthermore, the voltage balancing control of n-level DCC topologies with a high number of levels (n>3) becomes complex and impractical.

In the three-level FC converter, the control of the voltages in the flying capacitors is relatively simple; it can be performed independently per each phase by simply alternating the available two redundant switching states. A similar voltage balancing technique can be applied to FC topologies with a higher number of levels (n>3). However, in this case there are more redundant states to deal with, and also more flying capacitors to be controlled. Each redundant state produces different effects on the capacitor voltages. Subsequently, controlling the voltages across the capacitors becomes a challenge.

The balancing schemes listed in [7], [8] are based on rotating the carriers for different switches and are valid only under certain load conditions. Moreover, the control becomes more complex for converters with a higher number of voltage levels, as different triangular functions for individual switches have to be arranged at different voltage levels. In [9], the natural balancing effect was discussed using phase-shifted pulse-width modulation (PS-PWM), and in [10] the addition of a passive filter was used to accelerate the voltage balancing process of the flying capacitors using phase disposition pulse width modulation (PD-PWM). Also, an optimal modulation of FC using state machine is implemented and the natural balancing characteristics are discussed in [11]. The voltage balancing schemes shown in [7]-[11] use open loop strategies and are mostly based on modifying the carrier phases in the PS-PWM and PD-PWM schemes. The FC voltages, however, fail to retain their desired levels when there are disturbances due to nonlinearities or asymmetries in the system. Therefore, additional compensation based on a feedback control algorithm is required to balance the FC voltages.

There are several approaches using the feedback control algorithm discussed in [12]-[15]. They are based on changing the switching pattern for the control of the FC voltages. In [14], the algorithm uses redundant switching states to adjust the time of the switching function; however, the algorithm is

based on PS-PWM, which is spectrally sub-optimal. In [15], the voltage balancing control is based on space-vector modulation (SVM) by selecting the appropriate redundant switching states. This voltage balancing scheme seems to be very effective. The authors however do not perform any switching frequency analysis for the proposed voltage balancing strategy and neither evaluates the spectrum of the output voltages. Finally, in [16], a proportional-integral (PI) controller is used to compensate for the voltage errors in the FCs. However, the dynamic of the system for balancing capacitor voltages is slower using PI controllers than by selection of optimal redundant states in the modulation [15]. Furthermore, the tuning of the PI parameters is required [17], and it becomes difficult for converters with a high number of levels. Additionally, for converters with a number of levels higher than three (n>3), the authors of [16] suggest delaying the measured capacitor voltage signals to regulate the flying capacitor voltages, yet this scheme is based on a trial and error strategy.

The majority of the solutions discussed above do not analyze the effect of the voltage balancing schemes on the switching frequencies in the power devices. This paper presents a capacitor voltage balancing scheme that uses only optimum switching transitions. PD-PWM is applied and voltage balance is performed by a proper selection of the redundant switching transitions by using a cost function. The switching frequencies of the power devices are evaluated and compared to another voltage balancing scheme, which is based on optimizing the switching states independently and it does not avoid the critical switching transitions. This modulation strategy is called optimal-state voltage balancing (OSVB) scheme. The modulation strategy proposed in this paper that optimizes the transitions between consecutive states is called optimal-transition voltage balancing (OTVB) scheme. The analysis shows that by using the OTVB method, a significant reduction in the switching frequencies can be achieved as compared to OSVB. The voltage ripples in the FCs are also analyzed for the two voltage balancing modulation strategies.

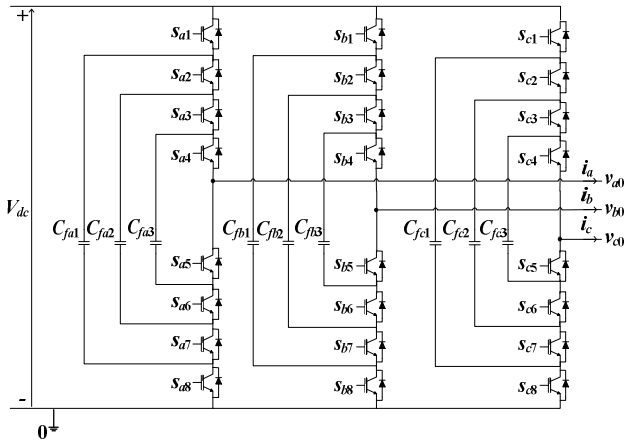

Fig. 1. Circuit Diagram of a five-level FC VSC.

The rest of the paper is organized as follows. Section II describes the operating principle of a five-level FC converter and the OSVB scheme. Section III introduces the OTVB scheme for reducing the switching frequencies in the power devices. Section IV presents some simulation results to verify the effectiveness of the proposed voltage balancing scheme on a five-level FC topology. In this section, switching frequencies on the power devices and capacitor voltage ripples are compared with those produced by the OSVB strategy. Finally, the conclusions are summarized in Section V.

II. Operating Principle of the FC Converter and the OSVB Scheme

Fig. 1 shows a schematic diagram of a three-phase five-level FC VSC, in which three FCs are integrated in each phase. During normal operation, the mean voltages of the FCs C_{fx1}, C_{fx2}, and C_{fx3}, should be maintained at $3V_{dc}/4$, $V_{dc}/2$, and

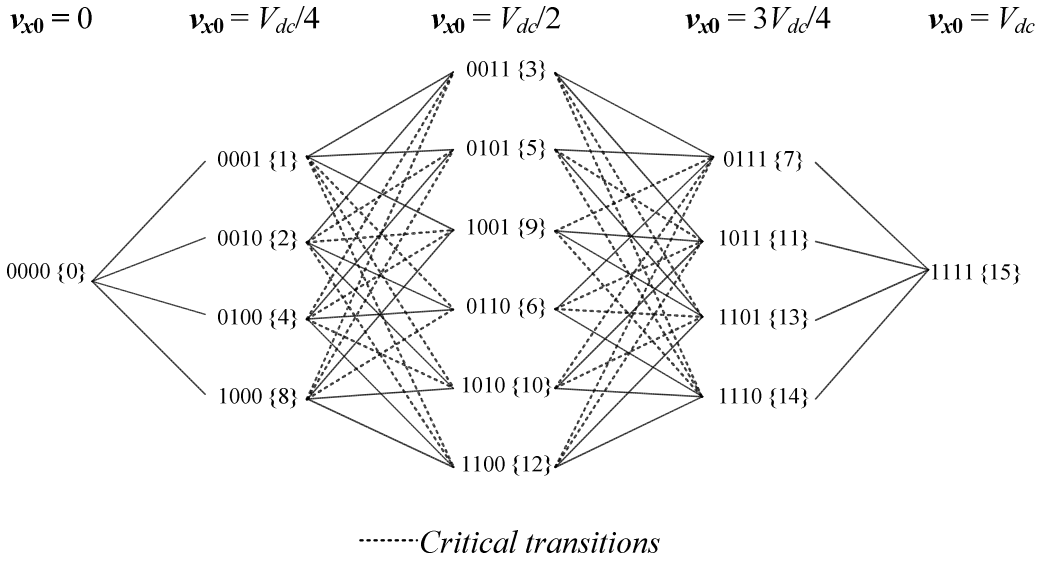

Fig. 2. Switching transitions between consecutive voltage levels.

V_{dc}/4, respectively, where the subscript 'x' is used for the phase identification x={a, b, c}, and 'V_{dc}' is the voltage of the dc bus. Consequently, the voltage across each switch is only one quarter of the dc-link voltage. The switch control functions are defined as s_{xy}, where 'y' is used to identify the particular switch in the phase leg of the FC converter (y=1,…,8). The control functions can take two values s_{xy}={0,1}, meaning "0" for switch off and "1" for switch on. The switch pairs in each phase leg s_{x1}-s_{x8}, s_{x2}-s_{x7}, s_{x3}-s_{x6} and s_{x4}-s_{x5}, operate in a complementary manner. Each phase can generate five output voltage levels, with respect to the dc negative rail "0", i.e. 0, V_{dc}/4, V_{dc}/2, 3V_{dc}/4 and V_{dc}. Using Kirchhoff's voltage and current laws, the line-to-ground voltage v_{x0} and the currents through the FCs (i_{Cx1}, i_{Cx2} and i_{Cx3}) can be written as:

$$v_{x0} = s_{x1}V_{dc}+(s_{x2}-s_{x1})v_{Cx1}+(s_{x3}-s_{x2})v_{Cx2}+(s_{x4}-s_{x3})v_{Cx3}, \quad (1)$$

$$i_{Cx1} = (s_{x1}-s_{x2})i_x , \quad (2)$$

$$i_{Cx2} = (s_{x2}-s_{x3})i_x, \quad \text{and} \quad (3)$$

$$i_{Cx3} = (s_{x3}-s_{x4})i_x . \quad (4)$$

Based on these fundamental equations, the line-to-ground voltage and the currents in the FCs are determined for all switching states and shown in Table I. The switching states are indicated by binary notation representing the control functions of the upper switches of the leg. As it can be seen in this Table I, the redundant switching states for the voltage levels 3V_{dc}/4, V_{dc}/2, and V_{dc}/4 define different current paths through the FCs. Fig. 2 shows the possible transitions between consecutive voltage levels considering the sixteen switching states of a leg. The binary notation of the switch control functions is also represented by its decimal number in curly brackets, as shown in Table I.

TABLE I
FIVE-LEVEL FC CONVERTER; VOLTAGE LEVELS, FC CURRENTS, AND SWITCHING STATES

Output Voltage Level (v_{x0})		Switching States					FC Currents			FC Voltages		
		s_{x1}	s_{x2}	s_{x3}	s_{x4}	*St.#*	i_{Cx1}	i_{Cx2}	i_{Cx3}	v_{Cx1}	v_{Cx2}	v_{Cx3}
5	V_{dc}	1	1	1	1	{15}	0	0	0	x	x	x
4	3V_{dc}/4	1	1	1	0	{14}	0	0	i_x	x	x	↑
		1	1	0	1	{13}	0	i_x	-i_x	x	↑	↓
		1	0	1	1	{11}	i_x	-i_x	0	↑	↓	x
		0	1	1	1	{7}	-i_x	0	0	↓	x	x
3	V_{dc}/2	1	1	0	0	{12}	0	i_x	0	x	↑	x
		1	0	1	0	{10}	i_x	-i_x	i_x	↑	↓	↑
		0	1	1	0	{6}	-i_x	0	i_x	↓	x	↑
		1	0	0	1	{9}	i_x	0	-i_x	↑	x	↓
		0	1	0	1	{5}	-i_x	i_x	-i_x	↓	↑	↓
		0	0	1	1	{3}	0	-i_x	0	x	↓	x
2	V_{dc}/4	1	0	0	0	{8}	i_x	0	0	↑	x	x
		0	1	0	0	{4}	-i_x	i_x	0	↓	↑	x
		0	0	1	0	{2}	0	-i_x	i_x	x	↓	↑
		0	0	0	1	{1}	0	0	-i_x	x	x	↓
1	0	0	0	0	0	{0}	0	0	0	x	x	x

Note: The charging/discharging effects in the FC is given assuming that i_x is positive (i_x>0) with the following notation;
↑ = capacitor voltage is charging
↓ = capacitor voltage is discharging
x = no change on the capacitor voltage

PD-PWM requires four carriers of the same amplitude, frequency and phase, which are arranged into contiguous bands that fully occupy the linear modulation range. A reference sinusoidal modulation signal is compared with the four triangular carriers to define the voltage levels that have to be generated at the output. This strategy is spectrally superior to other carrier layouts because it produces large harmonic concentration at some specific frequencies that cancels in the line-to-line voltages, hence reducing the output harmonic distortion [10]. However, the PD-PWM does not provide natural capacitor voltage balance. Therefore, an active balancing scheme is required to stabilize the flying capacitors voltages to the desired levels.

The OSVB scheme is based on minimizing a cost function, which is given as follows [14]:

$$J_{xz} = \frac{1}{2}\sum_{j=1}^{n-2} C_{fxj}(v_{Cxj} - v_{Cxj}^*)^2 , \quad (5)$$

where 'x' identifies the phase, and 'z' is the switching state z={0,…,15}; for example, J_{a12} is the cost function calculated for phase a and the switching state {12}, i.e. s_{a1}=1, s_{a2}=1, s_{a3}=0, and s_{a4}=0 (or 1100). 'j' is the index used for the identification of each flying capacitor j={1,2,3}, being C_{fxj} a particular flying capacitor, 'V_{Cxj}^*' its reference voltage, and 'n' is the number of levels (n=5 in this paper). This cost function is positive defined and if all the FC voltages equal their reference value, it becomes zero. Therefore, this cost function has to be minimized at any switching period to attain voltage balance. One of the methods for minimizing the cost function is through differentiation of (5), as follows:

$$\frac{d}{dt}J_{xz} = \frac{d}{dt}\frac{1}{2}\sum_{j=1}^{n-2} C_{fxj}(v_{Cxj} - V_{Cxj}^*)^2 = \sum_{j=1}^{n-2}(\Delta v_{Cxj} i_{Cxj}) \le 0 \quad (6)$$

where Δv_{cxj} is the voltage deviation of a flying capacitor (Δv_{Cxj}=v_{Cxj}-V_{Cxj}^*), and i_{Cxj} is the current in each FC, which depends on the selected redundant switching state and load current, as shown in Table I.

When the modulator defines two particular voltage levels for the following switching period, the cost function is evaluated for all redundant switching states available for each of those levels. Based on the calculated values, a single switching state is selected for each level, which are the ones that provide the minimum value to the cost function. They are therefore used to define the gating signals.

It should be remarked that the optimal switching states between two consecutive voltage levels are selected independently one from another. This might not be optimal from the point of view of voltage balancing. Furthermore, the OSVB does not avoid the critical transitions, thus resulting in higher switching frequencies for the power devices.

III. SWITCHING TRANSITIONS AND OTVB SCHEME

Fig. 2 shows the switching transitions between consecutive voltage levels of all the possible combinations of switching states from '0000{0}' to '1111{15}'. The transitions between two switching states shown by solid lines are called optimum transitions, as those transitions involve changing only one bit. As a result, they produce the minimum number of switching events. On the other hand, the transitions between two

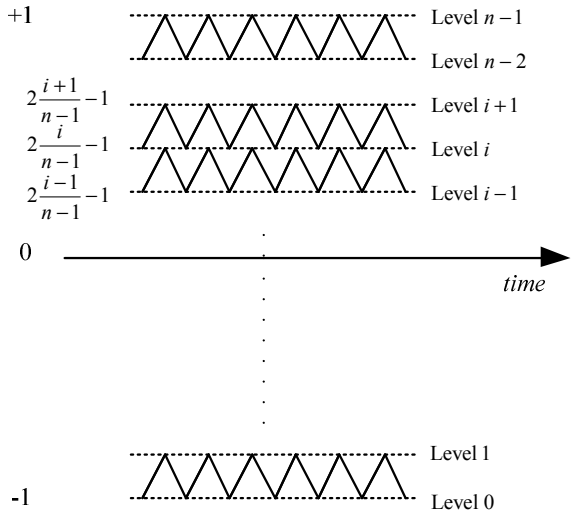

Fig. 3. Carriers in PD-PWM Strategy.

switching states represented by dotted lines are critical, as the change between two states may occur in two bits or more. For example, an optimal transition is produced when switching between the states '0001{1}' and '0101{5}' (see Fig. 2), while the transition between the states '0001{1}' and '0110{6}' is a critical one. Hence, if the critical transitions are chosen, the switching frequencies of the power devices increase.

Additional switching events can be produced due to the transitions within the same voltage level. Nevertheless, those transitions can be avoided by using sawtooth-shaped carriers. The switching frequencies of the power devices can be further reduced by avoiding the critical transitions between consecutive levels. However, avoiding the critical transitions will worsen the FC voltage balance. This effect can be attenuated by using a modulation scheme that chooses the optimal sequence between consecutive states, and not only the optimal states separately. As a result, the FC voltage balance will improve.

The cost function in (5) is modified to select the optimum switching transitions between two states of different voltage level and is given as:

$$J_{xsn1-sn2}=\sum_{j=1}^{n-2}(J_{x,sn1}d_{i1}+J_{x,sn2}d_{i2}) \tag{7}$$

where 'x' identifies the phase (x={a,b,c}), '$sn1$' is the first state, '$sn2$' is the second state, 'd_{i1}' ∈ [0,1] is the duty cycle of first state and 'd_{i2}' ∈ [0,1] is the duty cycle of the second state.

As shown in Fig. 3, the duty cycle of an output voltage level in a PD-PWM can be obtained as follows:

$$\text{for} \quad 2\frac{i}{n-1}-1\le v_{mx}\le 2\frac{i+1}{n-1}-1:$$

$$d_i=(i+1)-(n-1)\frac{v_{mx}+1}{2}, \tag{8}$$

$$\text{and for} \quad 2\frac{i-1}{n-1}-1\le v_{mx}\le 2\frac{i}{n-1}-1:$$

$$d_i=(n-1)\frac{v_{mx}+1}{2}-(x-1), \tag{9}$$

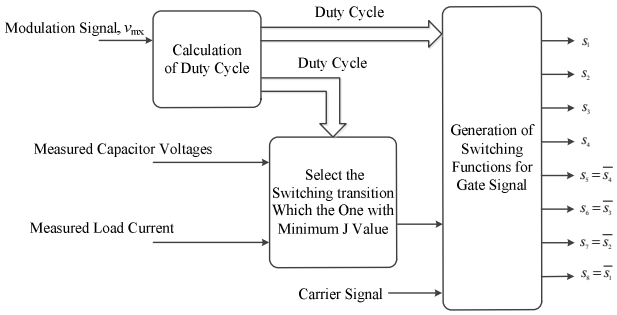

Fig. 4. Block diagram of five-level FC capacitor voltage balancing implementation scheme using phase disposition modulation for single phase.

where 'v_{mx}' is the modulation signal that ranges in the interval [-1,1] under linear operation mode.

The cost function of the transitions between two different voltage levels is positive defined, and if all the FC voltages are regulated at their reference value, it becomes zero. Hence, in order to achieve voltage balance, this cost function needs to be minimized at any switching period using differentiation. Differentiating (7), we get:

$$\frac{d}{dt}j_{xsn1-sn2}=\sum_{j=1}^{n-2}\Delta v_{Cxj}(i_{Cxj,sn1}d_{i1}+i_{Cxj,sn2}d_{i2})\le 0\,, \tag{10}$$

where '$i_{Cxj,sn}$' and '$i_{Cxj,sn+1}$' are the capacitor currents of the corresponding states. They depend on the load currents and the redundant switching states, as shown in Table I. 'Δv_{Cxj}' are the voltage deviations of the FCs ($\Delta v_{Cxj}=v_{Cxj}-V_{Cxj}^{*}$).

When the modulator defines two particular voltage levels for the following switching period, the cost function is evaluated for all the redundant optimum switching transitions available for those levels. Based on the calculated values, the switching transition that provides the minimum value to the cost function is selected. In order to avoid over-switching, all the critical transitions are skipped in the selection process. Once the switching transition is selected, the two consecutive switching states are determined. Then, they are used to define the gating signals of the transistors. Fig. 4, shows a block diagram for the implementation of the proposed voltage balance scheme.

IV. Performance Evaluation and Analysis

In this section, the modulation strategy with the proposed voltage balancing scheme is applied to a five-level FC VSC in MATLAB/Simulink using PLECS Blockset. In the simulations, the dc voltage is V_{dc}=8 kV and a Wye R-L load rated at 1 MVA with cosφ=0.99 is connected to the converter output. The value of the FCs is C=100 uF. The fundamental and the carrier frequencies are f=50 Hz and f_s=2.5 kHz, respectively.

The dynamic response of the closed loop voltage balancing scheme is shown in Fig. 5. In this simulation, the initial capacitor voltages were V_{Ca1}=8 kV, V_{Ca2}=3 kV and V_{Ca3}=1 kV, and regulated to the desired voltages, i.e. 6 kV, 4 kV, and 2 kV, respectively. It can be observed that the capacitor voltages reach their reference values in about 25 ms. Once in

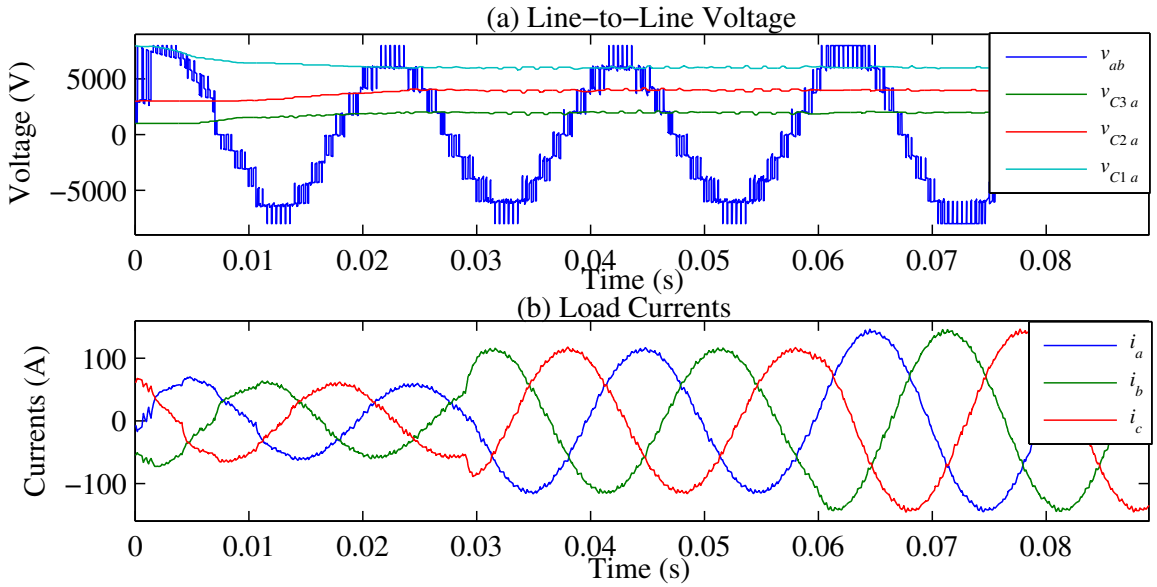

Fig. 5. Five-level FC line-line voltage under different load condition: (a) line-line voltage 'v_{ab}' and FC voltages of phase 'a', (b) three phase load current under different load conditions.

the steady state condition, there is a step change in the load (the resistor value changes from 64 to 32 Ohm), and later, at t=60 ms, the modulation index changes from m=0.8 to m=1. Observe that during the transients the voltages in the FCs remain unaffected. Hence, the proposed voltage balance control proves to be robust not only in the steady state but also under dynamic operating conditions.

Fig. 6 shows the average switching frequency of the power devices using the OTVB scheme. All possible relative current phase angles and modulation indices have been considered. In order to achieve the maximum amplitudes of the output voltage fundamentals under linear mode, a zero sequence has been added to the modulation signals of the three-phase system. The zero sequence is given by $v_o = -(v_{max}+v_{min})/2$, where v_{max} and v_{min} are the maximum and minimum values of the modulation signals of the three-phase system, respectively. As it can be noticed from Fig. 6, the output current phase angle does not significantly affect the switching frequency. On the other hand, large modulation indexes produce less switching frequencies than low modulation indices.

Fig. 7 shows the switching frequency ratio of both voltage balancing strategies, i.e. OTVB over OSVB, for all modulation indices and load power factors. It can be remarked that with the OTVB strategy there is a reduction of the switching frequency of about 10% on average for large modulation indices. Such a reduction in the switching frequency is even larger for low modulation indices.

Fig. 8 shows the FC voltage ripples ratio OTVB over OSVB. It can be remarked that with the OTVB strategy there is an increase in voltage ripples of about 10 to 15% on average for large modulation indexes. Such an increase in the voltage ripples becomes larger for low modulation indexes.

In summary, using the OTVB scheme can save about 10% of the switching frequencies in the power devices for large modulation indices at the expense of slightly increasing the FC voltage ripples.

V. CONCLUSION

This paper has presented a voltage balancing strategy for multilevel FC converters using an optimum switching transition scheme, so-called OTVB. This scheme is based on calculating a cost function considering the FC voltage deviations and the output currents. The proposed cost

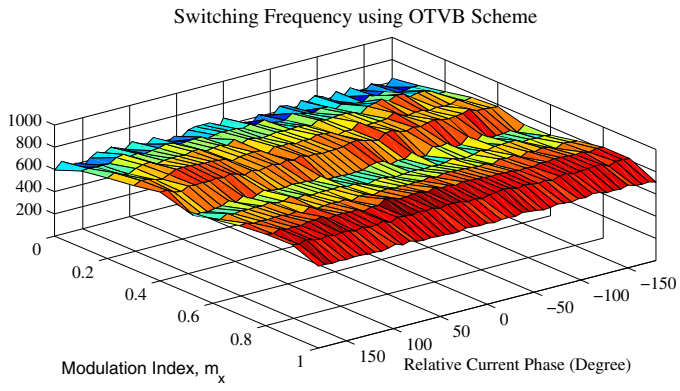

Fig. 6. Average switching frequency of power devices using OTVB modulation.

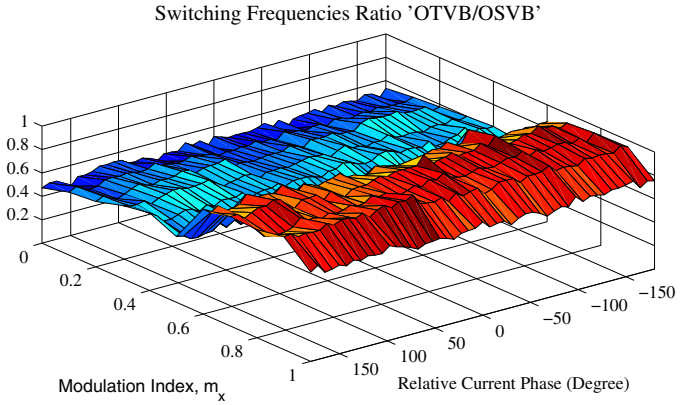

Fig. 7. Average switching frequencies ratio OTVB/OSVB of the power devices.

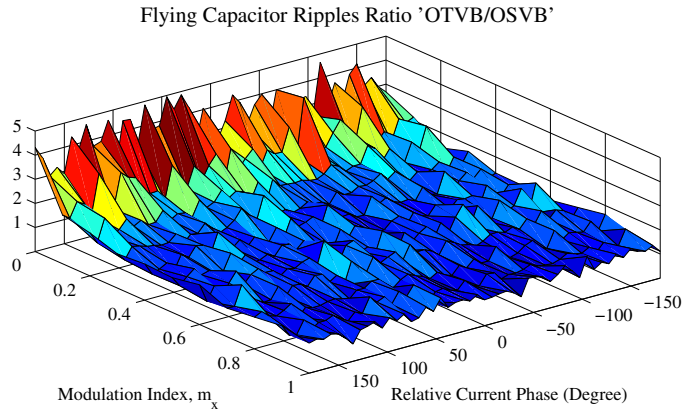

Fig. 8. FC voltage ripples ratio OTVB/OSVB.

function evaluates the switching sequences instead of the switching states, i.e. the two consecutive states between consecutive levels. Only the optimum switching transitions are evaluated and the one that gives the lower value to the cost function is selected. The proposed voltage balancing method is implemented in a five-level FC converter and tested against static and dynamic load conditions. It performs very well in regulating the FC voltages to the desired levels.

The results have been compared with a modulation strategy that does not avoid critical transitions and optimizes switching states instead of transitions, i.e. OSVB. Simulation results showed that, for large modulation indices, the average switching frequencies of the devices are reduced by about 10% when using the proposed OTVB modulation technique. This reduction comes at the cost of increasing the FC voltage ripples. Hence, a tradeoff between the switching frequency reduction and the increase of FC voltage ripples has to be considered.

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