Characterization and modelling of EMI susceptibility in integrated circuits at high frequency

Ignacio Gil* and Raúl Fernández-García
Department of Electronic Engineering
UPC. Barcelona Tech
Colom 1, 08222 Terrassa, Spain
*e-mail: ignasi.gil@upc.edu

***Abstract*—In this paper an alternative method for characterizing and modelling the EMI susceptibility in integrated circuits at frequencies above 1 GHz is presented. The PCB layout design is focused on the optimization of the impedance mismatch losses on the radio frequency interference injection path. The PCB has been tested with several commercial operational amplifiers and the methodology is validated through both electrical transmission line simulations and electromagnetic cosimulations.**

Keywords-Immunity to Electromagnetic Interferences; Integrated Circuits; Operational Amplifier

I. INTRODUCTION

Over recent years, due to the increasing demand for multi-functional, multi-band wireless operation electronic devices, a significant expansion in terms of the frequency range of transceivers has been produced. This fact has created a severe and complex electromagnetic (EM) pollution environment. Therefore, the immunity to Electromagnetic Interferences (EMI) has become a more important constraint for integrated circuit designers. In fact, current EMC roadmaps include frequency increasing as one of the major constraints in the evolution of the immunity of integrated circuits (ICs), due to technology trend toward higher operation bandwidths provoked by customer pressure [1]. Nowadays, the most mature IC susceptibility measurement method concerning radio frequency interference (RFI) corresponds to the IEC 62132-4 Direct RF Power Injection [2]. This standard method is defined in the frequency range 150 kHz-1 GHz. However, modern communication systems operation frequencies exceed the 1 GHz limit. Recently, several works have been focused on the frequency range expansion for DPI testing above 1 GHz [3-4]. On the other hand, many works have been devoted to the study of the susceptibility of analog ICs (the most sensitive circuits to RFI) and, particularly, the Operational Amplifiers (OpAmps) [5-8], since they are found in a wide range of circuits where they are used to amplify and condition signals. Although, most of the proposed setups consider EMI frequencies above 1 GHz, the distributed effects of transmission lines are not deeply addressed. In this paper an alternative susceptibility characterization and modelling method for ICs is proposed in order to take into account high frequency effects and minimize their impact, such as impedance mismatches, ohmic and dielectric losses etc.

The paper is organized as follows: in Section II the proposed PCB test and measurement setup are presented. In Section III the transmission line model of the PCB as well as electrical simulation schematics and electromagnetic cosimulation layouts are provided. In Section IV the main experimental results are discussed and compared with both electrical model and electromagnetic simulations. Finally, in Section V some conclusions are summarized.

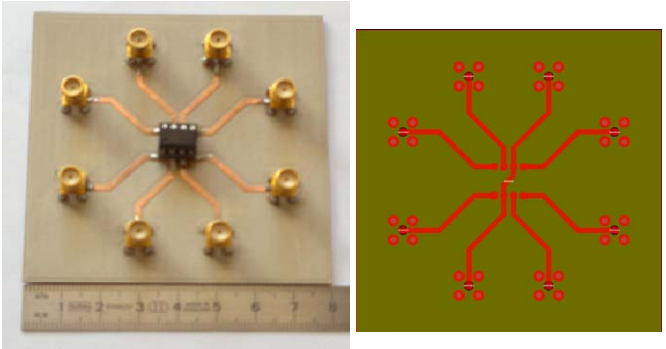
II. TEST PCB AND EXPERIMENTAL SETUP

A. Test printed circuit board and layout criteria

Fig. 1 shows the experimental PCB as well as the designed layout. The board (with overall dimensions 8x8 cm^2) is performed by means of a symmetrical layout based on 8-pin microstrip traces with characteristic impedance. Z_0=50 Ω, and the same electrical length in order to present identical behavior for all injection ports. In order to investigate the RFI immunity level of several commercial OpAmps, a follower topology has been selected, as a worst EMI case [5]. Moreover, all the devices under test (DUT) are mounted on a DIP-8 package in combination with an 8 pin dual in line IC socket (808-AG11D-ESL-LF). The aim of this configuration is to have a worst case in terms of mismatching impedance and parasitic effects at high frequencies in order to test the injection effectiveness of the PCB. The prototype has been fabricated on the *Rogers RO3010* substrate (dielectric constant ε_r=10.2, thickness h=1.27 mm, tanδ =0.0023), with high performance up to 10 GHz.

B. Experimental setup

Fig.2a illustrates the experimental setup. It consists of a RF signal generator (providing the RFI disturbance up to 3.2 GHz) directly connected to a directional coupler in order to measure



(a) (b)

Fig. 1. (a) PCB test. (b) Designed layout.

This work was supported by the Spanish Government-MINECO under Project TEC2010-18550 and AGAUR 2009 SGR 1425.

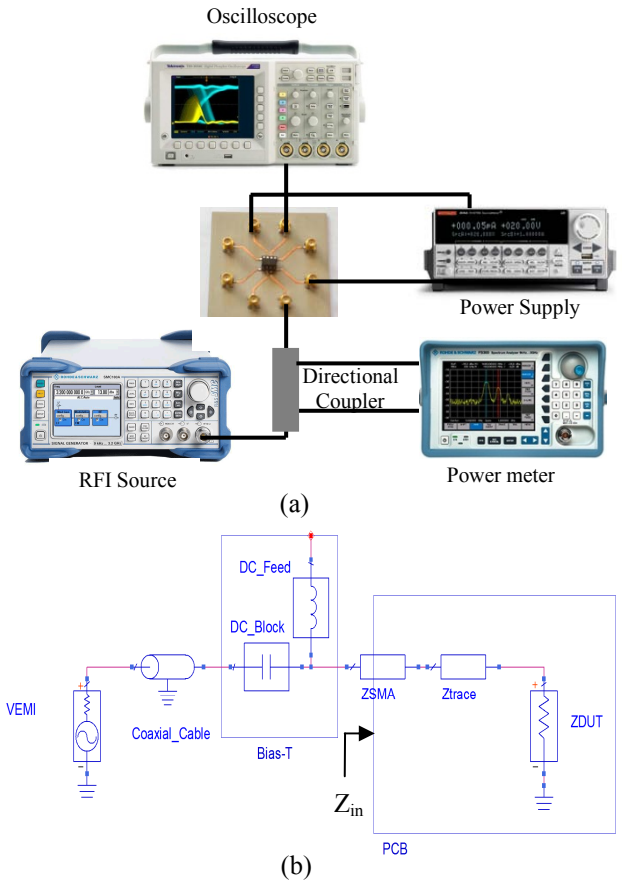


Fig. 2. (a) Experimental setup. (b) RFI input signal path.

the actual level of power injected into the DUT. Since the RF signal injection is applied at the noninverting input of the OpAmp (with no significant DC component) and no RF amplifier is used, it is optional to use a bias tee as a DC block. In case of RFI injection at a bias pin, the bias tee becomes mandatory in order to prevent DC supply from getting RF power. Fig. 2b details the RF input signal path by taking into account all the impedance transmission line stages. The injection RFI signal will inevitably experience multiple impedance mismatches and reflections along this path, unless a good matching is performed in all intermediate stages. The objective of the test PCB is to preserve an excellent 50 Ω injection path in all the system. In this case, the reflected power corresponds only to the mismatch due to the difference between the characteristic impedance of the traces, Z_0, and the input impedance of the pin *j* of the IC, Z_{DUTj}. Moreover, the rest of second order effects such as the frequency response of the directional coupler, ohmic losses, etc., have been de-embedded in order to obtain the actual value of injected power into Z_{DUTj}.

C. Experimental methodology

From the experimental return losses at the injection *j*-th SMA connector, S_{jj}, measured by means of a vector network analyzer, it is possible to calculate the experimental input impedance Z_{inj}. In fact, for a one-port network, S_{jj} , is given by [9]:

$$S_{jj} = \frac{Z_{in_j} - Z_0}{Z_{in_j} + Z_0} \ . \tag{1}$$

In that case, by solving (1) for Z_{inj} , we obtain:

$$Z_{in_j} = Z_0 \frac{1 + S_{jj}}{1 - S_{jj}} \ . \tag{2}$$

By considering the RFI injection path as a lossless transmission line at Z_0 (a good approximation in case of all the intermediate stages, depicted in Fig. 2b, matched at Z_0), the equivalent transmission line impedance equation is given as follows:

$$Z_{in_j} = Z_0 \frac{Z_{DUT_j} + jZ_0 tan\beta l}{Z_0 + jZ_{DUT_j} tan\beta l} \ , \tag{3}$$

where β, corresponds to the phase constant and *l* is the length of the transmission lines (*l*=29 mm for the designed PCB). From measured S_{jj} and (3), we can determine Z_{DUTj} according to:

$$Z_{DUT_j} = Z_0 \frac{Z_0 \tan \beta l - Z_{in_j}}{Z_{in_j} \tan \beta l - Z_0} \ , \tag{4}$$

where:

$$\beta = \frac{2\pi}{\lambda} \ ; \quad \lambda = \frac{c}{f\sqrt{\varepsilon_r}} \ , \tag{5}$$

being λ and *f* the wavelength and frequency of the propagated RFI signal and *c* the vacuum velocity of light.

Fig. 3 depicts the methodology followed in both the measurements and simulations in order to determine Z_{DUTi}, and therefore, the actual degree of mismatching. The procedure is based on the application of the RFI injection port (identified as port 1) at the SMA connector corresponding to the PCB trace loaded with the noninverting input of the OpAmp (Z_{DUT}). Then, by measuring S_{11} and by applying equations (2-5), experimental Z_{DUT} is obtained. The immunity setup is used to measure the offset voltage level at the output of the OpAmp in order to evaluate the susceptibility impact of the RFI in terms of power level and frequency. In this sense, the effectiveness of the matching in all the intermediate stages of Fig. 2b is critical in order to avoid any reflection (toward the source) in the PCB except in the case of the input IC stage (intrinsic mismatching). If so, the lack of an RF amplifier in the experimental setup would be justified.

III. Modelling and Simulation

A. Simulation methodology

The simulation methodology is based in the obtained results from electromagnetic simulation of the PCB with the aim to perform an accurate electrical model of the transmission lines involved in the test PCB. First of all, the overall PCB layout without the IC (Fig. 1b) is electromagnetically simulated by means of the *Agilent Momentum* commercial software based on the well-known method of moments. An S-parameter simulation is performed by considering all ports (including SMA connectors and inputs of the IC footprint) terminated at

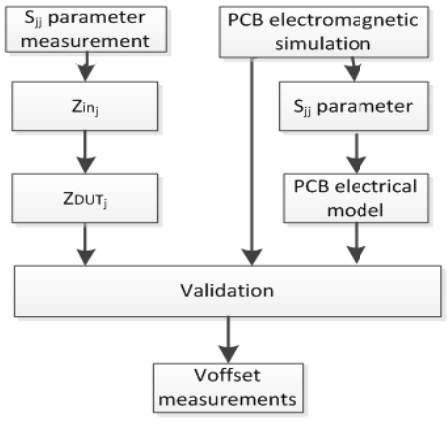


Fig. 3. Experimental and simulation methodology.

50 Ω. This simulation provides the return losses (S_{11}) and insertion losses (S_{21}) in order to determine the degree of matching of the RFI injection path. The actual width dimension of the microstrip traces (w=1.2 mm) is extracted by means of a commercial transmission line calculator (*Agilent LineCalc*) by taking into account the specifications of the substrate, detailed in Section II.

From the electromagnetic simulations it is possible to achieve the required parameters in order to develop the lumped-element equivalent-circuit model of the PCB traces. In fact, assuming lossless transmission lines, the main design equations are [9]:

$$v_p = \frac{1}{\sqrt{LC}} \quad ; \quad Z_0 = \sqrt{\frac{L}{C}} \tag{6}$$

Where L and C are the per-section inductance and capacitance of the transmission line cells and v_p is the phase velocity, which can be computed from the simulated phase of S_{21}, $\phi(S_{21})$, according to:

$$v_p = \frac{2\pi l f}{\phi(S_{21})} \tag{7}$$

Once the PCB is modeled, the IC is included in the overall simulation system by including the experimental extracted Z-parameters of Z_{DUTj} (according to procedure detailed in Section II-C) as loads in the different transmission lines. In fact, two kinds of simulations have been performed. On the one hand, the electrical simulations of the lumped model in combination with Z_{DUTj} and in the other hand, the electromagnetic cosimulation of the PCB loaded with Z_{DUTj}.

B. Simulation setup and modelling

Fig. 4 depicts the equivalent T-circuit model for the test PCB including the IC used in the electrical simulations, where L_{jk}, C_{ik} and Z_{DUTj} model the inductance, capacitance and IC's impedance of the *j-th* PCB trace, respectively. Table I reports the extracted per-section inductances and capacitances on the board. Notice that traces 1 and 8, 2 and 7 and so on, present the same values due to the symmetry of the PCB. Anyway, the calculated values according to electromagnetic simulations are very similar because of the overall symmetry in all traces.

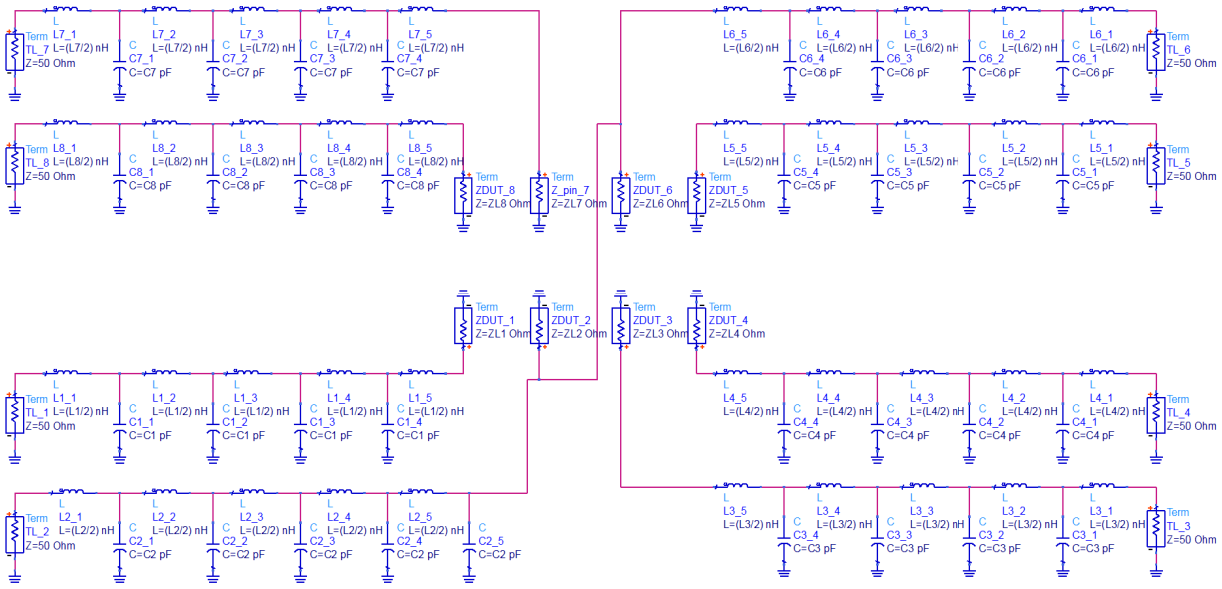


Fig. 4. Lumped equivalent circuit model for the PCB and IC used in electrical simulation.

TABLE I. LUMPED EQUIVALENT CIRCUIT ELEMENTS OF THE PCB

PCB Trace	L_j (nH)	C_j (pF)
1,8	3.265	1.306
2,7	3.204	1.282
3,6	3.242	1.297
4,5	3.433	1.245

Fig. 5 illustrates the cosimulation setup for the noninverting input of the OpAmp. In this case, the PCB is electromagnetically simulated in combination with the electrical model of the injection port and the experimental Z-parameters obtained experimentally for Z_{DUTj}. In the next Section, both electrical and cosimulation results are compared with measurement data.

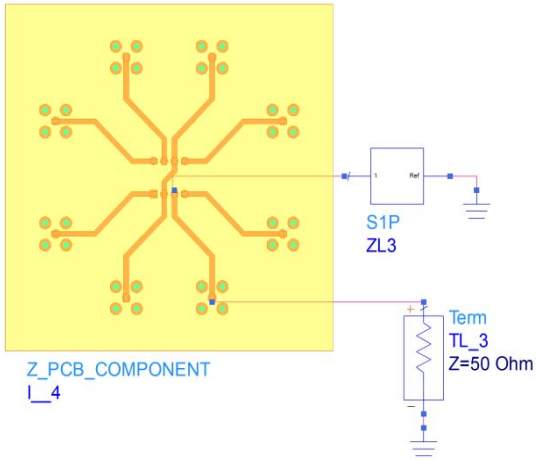


Fig. 5. Cosimulation setup (PCB+IC).

IV. RESULTS AND DISCUSSION

Figs. 6 and 7 include the comparison of insertion and return losses between the electrical and the electromagnetic simulations corresponding to the noninverting input injection path of the PCB terminated with 50 Ω. As can be observed, a good degree of matching is achieved in the PCB design for the infection frequency range (10 MHz-3 GHz) with return losses lower than -20 dB. Therefore, the main source of mismatch will be only due the IC, as it is desired. In order to test the setup and the degree of immunity, two commercial OpAmps with different technologies have been measured, a LM741 based on bipolar transistors and TL081 based on JFET technology. After including the OpAmps, the experimental S_{11} is determined as shown in Fig. 8. It is observed the usual behavior at low frequencies where a high reflection level is produced due to the high impedance of the OpAmp. At f>100 MHz, distributed effects arise and S_{11} presents the corresponding behavior depending on the frequency. Obviously, a degradation of the matching is measured due to Z_{DUTj}. Nevertheless, S_{11} levels lower than 10 dB can be achieved in some frequencies ranges above 1 GHz.

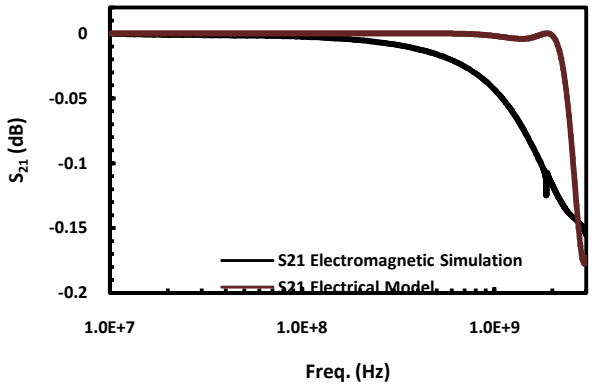


Fig. 6. Simulated insertion losses concerning the injection path of the noninverting input of the OpAmp, terminated at 50 Ω (with no IC).

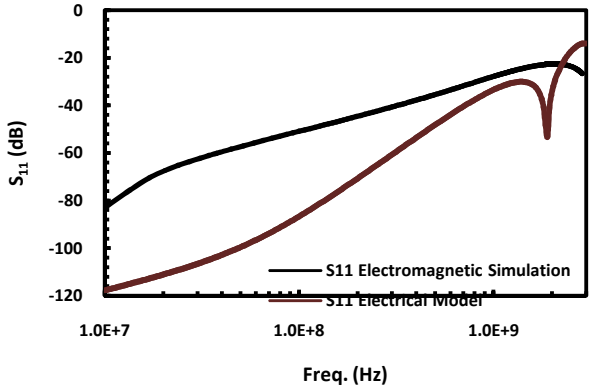


Fig. 7. Simulated return losses concerning the injection path of the noninverting input of the OpAmp, terminated at 50 Ω (with no IC).

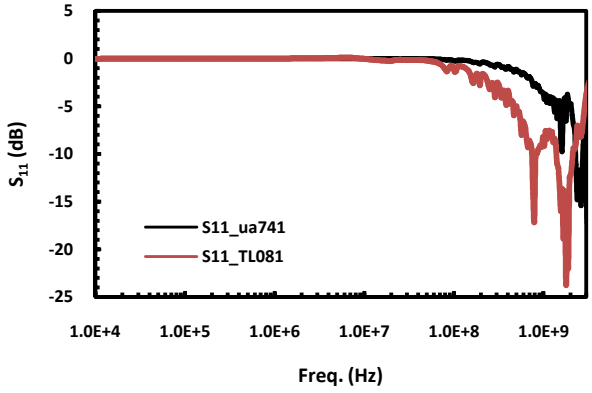


Fig. 8. Experimental return losses for the noninverting input of the PCB loaded with the tested OpAmps.

By using equations (2-4) we can determine experimental input impedance of the DUT as shown in Fig. 9. Figs. 10 and 11 show the comparison between the measured input impedance Z_{in} and simulated results by means of the electrical model and the electromagnetic cosimulation setup explained in the

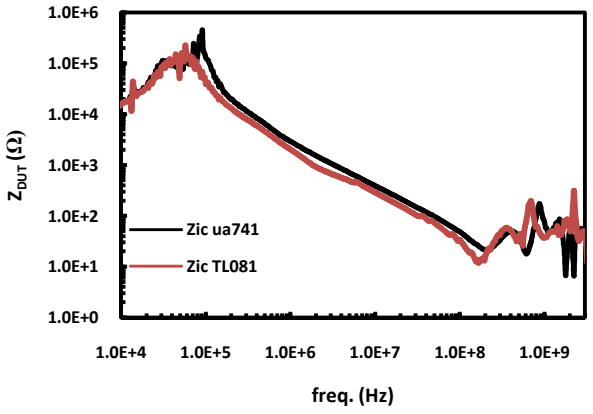


Fig. 9. Experimental Z_{DUT} of both tested OpAmps.

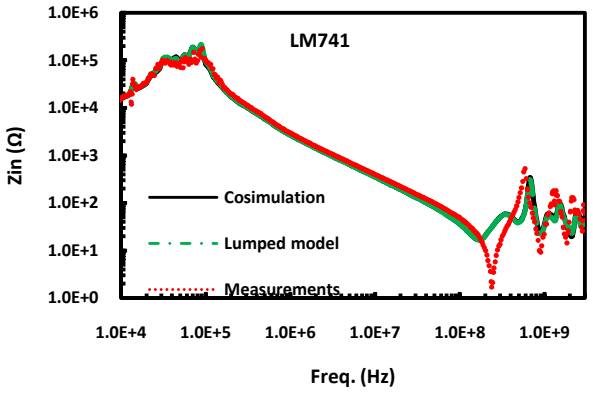


Fig. 10. Input impedance measured at the injection port SMA of the PCB in comparison with lumped model simulation and electromagnetic cosimulation for the LM741 OpAmp.

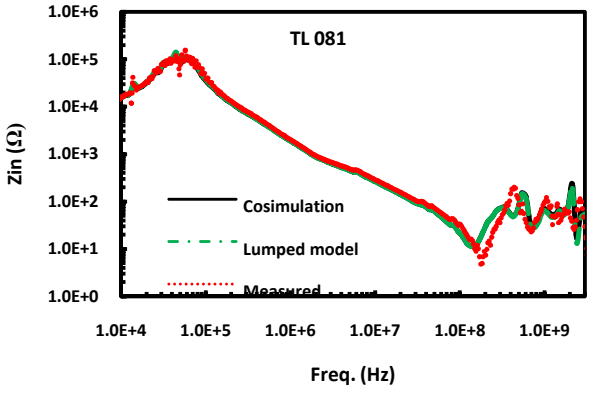


Fig. 11 . Input impedance measured at the injection port SMA of the PCB in comparison with lumped model simulation and electromagnetic cosimulation for the TL081 OpAmp.

previous Section. A good degree of accuracy is achieved between both simulations and experimental data. Since the lumped model is obtained from the electromagnetic

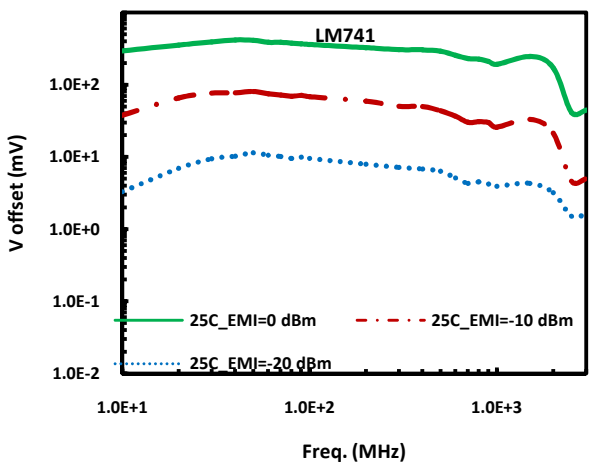


Fig. 12 . Effect of RFI injected at the input SMA of the PCB loaded with the LM741 OpAmp at room temperature.

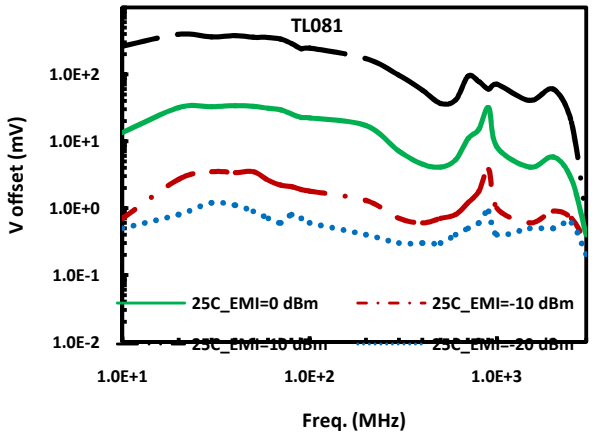


Fig. 13 . Effect of RFI injected at the input SMA of the PCB loaded with the TL081 OpAmp at room temperature.

simulations, an excellent accuracy between both simulation results is achieved. Therefore, the level of accuracy between simulations and experimental is achieved thanks to the good performance of the electromagnetic simulations. These results validate the modeling and simulation process with regard to the proposed experimental setup. In order to test the proposed experimental setup, the offset voltage level of both OpAmps has been measured at the output pin of the corresponding ICs. Figs. 12 and 13 depict the frequency impact of the offset by injecting several levels of RFI power at room temperature. It is observed that high levels of voltage offset are reached. For instance, for the LM741 an offset level higher than 100 mV is achieved for a 0 dBm RFI power. According to measured conventional offset level (measured value is 1.2 mV), a susceptibility impact of the EMI case higher than 2 order of

magnitude is observed. In the case of the TL081 OpAmp, similar results are obtained. In fact, the free EMI case offset corresponds to 0.8 mV whereas a maximum value for a 10 dBm RFI power imply an offset in the order of 100 mV. In all cases, the losses and mismatching have been de-embedded in the experimental setup. Therefore, the proposed setup prove experimentally that RF amplifier is not required if a good matching is achieved on RFI injection port for the tested ICs.

V. CONCLUSION

In this work a matched an symmetrical test PCB has been presented in order to characterize the RFI susceptibility at frequencies above 1 GHz. The system consists of minimizing the mismatching in all the stages of the injection path in order to simplify the overall experimental setup by not considering a RF Amplifier. Both electrical simulations and electromagnetic cosimulations validate the experimental results concerning measured impedances. Moreover, the method has been checked for the susceptibility impact into 2 commercial OpAmps by implementing a follower topology.

REFERENCES

[1] M. Ramdani, E. Sicard, A. Boyer, S. Ben Dhia, J.J. Whalen, T.H. Hubing, M. Coenen and O. Wada, "The electromagnetic compatibility of integrated circuits-past, present and future", *IEEE Transactions on Electromagnetic Compatibility*, Vol. 51, pp. 78–100, February 2009.

[2] EN IEC 62134-4, Integrated Circuits – Measurement of electromagnetic immunity, 150 kHz to 1 GHz – Part4: Direct RF Power injection method.

[3] J. Catrysse, D. Pissoort and F. Vanhee, "Expanding the frequency range for DPI testing of IC's above 1 GHz: an alternative proposal", *Proc. of the EMC Europe 2011*, pp. 400–404, September 2011, York, UK.

[4] S. Buntz, M. Blatter, H. Leier, S. Fuchs, D. Gwissdalla and W. Menzel, "Direct power injection immunity measurements at frequencies above 1 GHz", *Proc. of the EMC Europe 2006*, vol. 2, pp. 882–887, September 2006, Barcelona, Spain.

[5] A. Richelli, "Measurements of EMI susceptibility in ultra-low-voltage OpAmps", *Proc. of the EMC Compo 2011*, pp. 13–17, November 2011, Dubrovnik, Croatia.

[6] F. Fiori, "Design of an Operational Amplifier Input Stage Immune to EMI," *IEEE Transactions on Electromagnetic Compatibility,* vol.49, no.4, pp.834-839, November 2007.

[7] J. Gago, J. Balcells, D. Gonzalez, L. Lamich, J. Mon, A. Santolaria, "EMI Susceptibility Model of Signal Conditioning Circuits Based on Operational Amplifiers," *IEEE Transactions on Electromagnetic Compatibility,* vol.49, no.4, pp.849-859, November 2007

[8] J.-M. Redoute, M. Steyaert, "Measurement of EMI induced input offset voltage of an operational amplifier," *Electronics Letters* , Vol.43, no.20, pp.1088-1090, September 2007.

[9] D.M. Pozar, "Microwave Engineering, 4th Edition", John Wiley & Sons, 2012.