Voltage Divider for Self-Limited Analog State Programing of Memristors

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Abstract— Resistive switching devices - memristors - present a tunable, incremental switching behavior. Tuning their state accurately, repeatedly and in a wide range, makes memristors well-suited for multi-level (ML) resistive memory cells and analog computing applications. In this brief, the tuning approach based on a memristor-resistor voltage divider (VD) is validated here experimentally using commercial memristors from Knowm Inc. and a custom circuit. Rapid and controllable multi-state SET tuning is shown with an appreciable range of different resistance values obtained as a function of the amplitude of the applied voltage pulse. The efficiency of the VD is finally compared against an adaptive pulse-based tuning protocol, in terms of circuit overhead, tuning precision, tuning time, and energy consumption, qualifying as a simple hardware solution for fast, reliable, and energy-efficient ML resistance tuning.

Index Terms—memristor, resistive switching, ReRAM, multi- level memory, voltage divider, Knowm, Digilent AD2

I. Introduction

EVER since 2008 and the first demonstration of the TiO_2- based device by Hewlett-Packard Laboratories (HP Labs) [1], both academia and industry turned their attention to the emerging technology of resistive switching devices, i.e. nanoscale, nonvolatile, two-terminal devices whose resistance changes depending on the applied input. Such devices are generally referred to as memristors or memristive devices, owing to the corresponding theory of the fourth fundamental circuit element postulated by L. Chua [2], and its connection with practice via the HP Labs´ invention in 2008 [1].

Some memristors that have been reported switch rapidly and in a binary fashion between a low and a high resistance, while others can have their resistance controlled in an analog manner [3]. Such unique incremental state tuning ability, combined with other prominent performance and technological features such as small integration area and post- CMOS processing compatibility, have given rise to several potential applications of memristors [4], [5]. Nevertheless, the switching variability —both from device to device but mainly for the same device upon cycling— is still an ongoing research topic. The final achieved resistance is generally a function of the applied pulse polarity, amplitude, and duration. However, owing to variability and the stochastic nature of internal resistive switching phenomena [6], it is difficult to drive the device accurately and repeatedly to a specific desired state just by applying a single well-calculated pulse. Thus, several strategies/circuits and different adaptive pulsing protocols/algorithms have been proposed in the literature to improve the controllability of multi-level (ML) resistive states [7]-[11] and enable single-cell ML resistive storage systems.

The main drawbacks of most such tuning approaches are associated to the long time required until the desired state can be reached and/or the necessary hardware (HW) for external processing of the pulsing properties, comparators for real-time state-monitoring, etc. Another way the memristors can be programmed is through the use of a series access transistor that allows variable state programming through compliance current limiting [12].

However, a novel concept published in [13] proposed exploiting the incremental threshold-type switching behavior of memristors (i.e. the fact that change-rate is significant only above a voltage threshold) in a memristor-resistor voltage divider (VD) configuration [see Fig. 1(a)] for rapid and accurate multi-state tuning. This was not the first time that the VD concept was visited in the literature. Jo et al. [14] observed ML switching in nanoscale a-Si devices by applying the exact same pulse but with a different series resistor. Kim et al. [15] demonstrated a self-limited switching property achieved via a series resistor (and an additional threshold switch) integrated in the same memory cell. In both [14] and [15], the devices were overdriven by large voltages to have sufficient voltage (higher than a threshold) to trigger the switching but minimize any excess voltage that could harm the device. Indeed, the series resistor is an excellent “excess voltage absorber” as it prevents from overstressing and thus improves device endurance [16]. Some more recent works also studied the VD impact in bidirectional tuning circuits with a FET transistor as resistive element [17].

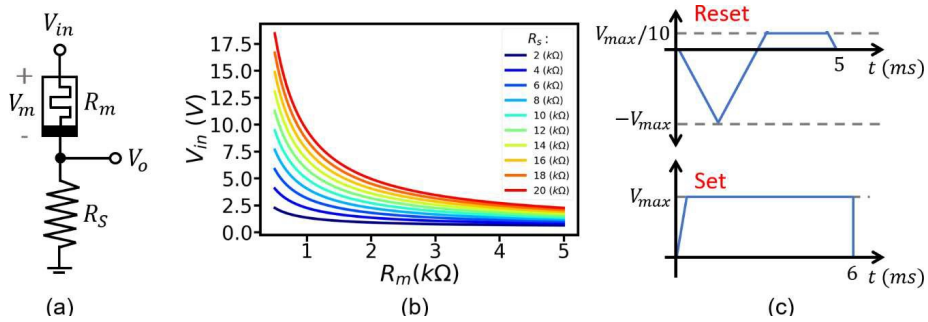


Fig. 1. (a) Circuit schematic of the memristor-resistor voltage divider. (b) Plot of (1) showing the required V_{in} amplitude for a range of desired final resistance R_m. From bottom (dark blue line) to top (dark red line) we simulate (1) for different R_S values between 2kΩ and 20kΩ using V_{SET}=0.45V and $R_m \in$ [0.1, 5]kΩ. (c) Shape of the applied input voltage (V_{in}) for RESET and SET processes. For RESET, a negative triangular pulse was applied immediately followed by a small positive pulse for initialization purposes. The SET pulse rise time was 0.25ms.

So, convinced about its utility and ease of use, in the work reported in this brief we build upon the theoretical analysis presented in [13] and demonstrate an experimental verification of the VD approach for accurate SET resistance tuning of memristors. The sensitivity of the VD approach to the V_{SET} threshold variability was investigated and an appreciable range of different average resistance values was observed, as a function of the applied V_{in} voltage, in agreement with the simulation-based analysis in [13]. The efficiency of the VD tuning approach was finally compared with an adaptive pulse-based accurate tuning protocol [11] in terms of: (i) circuit complexity/overhead, (ii) tuning precision, (iii) tuning time, and (iv) energy consumption. The experimental results confirm the potential of the VD approach to be used for fast and reliable ML SET tuning, using simple and cheap HW.

II. Memristor-Resistor Voltage Divider: Topology

which determines the SET ($R_{OFF} \rightarrow R_{ON}$) transition. R_m is initially RESET in a high resistive state (R_{OFF}) by applying a negative triangular pulse with a fixed negative limit. RESET is a self-reinforced process in this circuit since the higher the R_m gets, the larger V_m becomes, which could cause stack-at-OFF faults [21]. So a triangular pulse was preferred instead of a rectangular pulse to reduce the time during which the device has a large voltage drop [see Fig. 1(c)]. For the SET process to work, by selecting $R_S < R_{OFF}$ it should be $V_{in} \gg V_{SET}$ so that $V_m > V_{SET}$ to trigger the SET switching. As R_m decreases, so does V_m owing to the redistribution of the applied voltage on the two resistive elements induced by the VD effect, until it becomes $V_m = V_{SET}$, which is when the SET process is self- interrupted. At this moment, assuming $V_m = V_{SET}$, using the Kirchhoff's Current Law (KCL) we can interpret the applied voltage as a function of the target (final) resistance as follows:

DESCRIPTION & TARGET DEVICE CHARACTERISTICS

All measurements were carried out in a fully automated manner using the digital oscilloscope and function generator of the Digilent Analog Discovery 2 (AD2) instrumentation to AD2. The RS devices used were BS-AF-W discrete self- directed-channel bipolar memristors with tungsten (W) dopant [19], developed and commercialized in 16-pin ceramic DIP packages by Knowm Inc. [20]. Such devices operate primarily through the electric field-induced generation of metal ions that move through a multilayer chalcogenide material stack. Once the ions reach to the lower potential electrode, they are reduced to their metallic form and eventually form a conductive pathway that spans the active material layer.

A. Voltage Divider Basics

We shortly provide the basics about the memristor-resistor voltage divider (VD) tuning concept [15]. The circuit schematic is shown in Fig. 1(a). The circuit consists of a resistor R_S in series with a memristor, whose resistance (memristance) is $R_m \in [R_{ON}, R_{OFF}]$. V_{in} is the voltage applied to the VD. V_m is the instant voltage drop on R_m, which will decrease when it is $V_m>0$, as shown in Fig. 1(a).

The resistance change-rate of the memristor is much more significant above a SET voltage threshold V_{SET} (see Fig. 2), $\forall R_m \in [R_{MIN}, R_{MAX}]$ there is a unique voltage calculated as $V_{in} = f(R_m)$ which will SET the memristor precisely to this R_m (assuming ideally a hard threshold V_{SET} and no variability). From (1) it can be figured out that R_S affects the shape of $f(\cdot)$. This is better seen in Fig. 1(b) where we plot (1) for ten different R_S values. Higher R_S values lift up the curve of $f(\cdot)$ locally changing its shape, but the required V_{in} range also increases. Ideally, the slope of (1) should not be very sharp in the desired R_m range. Depending on the resolution of V_{in}, i.e. on how small the applied voltage change Δv can be, there is a difference in the tuning precision; ΔR_m is lower for R_m values closer to R_{ON} and higher for R_m values near R_{OFF}.

B. Target Memristor Device Considerations

For the VD tuning approach to be valid, the target memristor devices should demonstrate incremental threshold- based switching behavior. Figure 2 confirms that the commercial bipolar devices used in this study comply with this requirement. Specifically, we show the average final resistance as a result of a sequence of 10-ms wide SET pulses of gradually increasing amplitude, applied separately to a

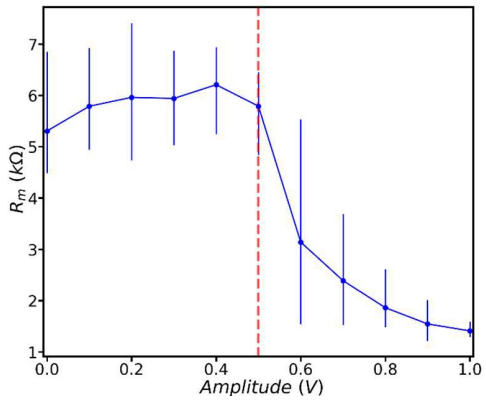


Fig. 2. Average final resistance R_m as a result of the application of a sequence of 10 consecutive SET pulses of fixed width (10ms) and gradually increasing amplitude by 100mV. After every SET pulse [see pulse properties in Fig. 1(c)], a 0.5ms-wide read pulse was applied. Pulse separation was 0.5ms. The experiment was repeated 5 times and dots correspond to mean values, whereas vertical lines denote the entire R_m value range for every pulse amplitude. The red dashed line is a guide to the eye for the V_{SET} threshold. For this experiment R_s was removed and compliance current I_{CC} = 600uA was applied instead.

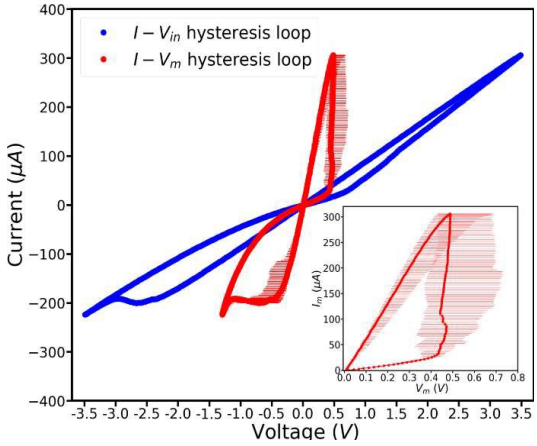


Fig. 3. i-v characteristics for a triangular V_{in} voltage of amplitude 3.5V and frequency 80Hz applied to the memristor-resistor VD. The blue line shows the current against V_{in}, whereas the red line shows the same current against the voltage drop on the memristor V_m. Data correspond to mean values of 50 cycles with R_S = 10kΩ. Horizontal lines for the red curve indicate the range of voltages when a particular current value was reached while cycling. Inset shows enlarged the positive part of the red i-v curve for clarity.

memristor without the series resistor. In-between such pulses, a 0. stor state. We performed 5 iterations of the experiment, each time af tate around 6kΩ. By observing the results, we notice a separation (appı that hardly affect the device state and those that have a more imm ude exceeds such threshold, there is almost no significant effect on the lse. However, resistance switching is highly device/material- depen · to- cycle variability. For instance, variability in switching threshold ices used in our study do not have a hard V_{SET} threshold.

So, given that VD tuning accuracy is highly dependent on

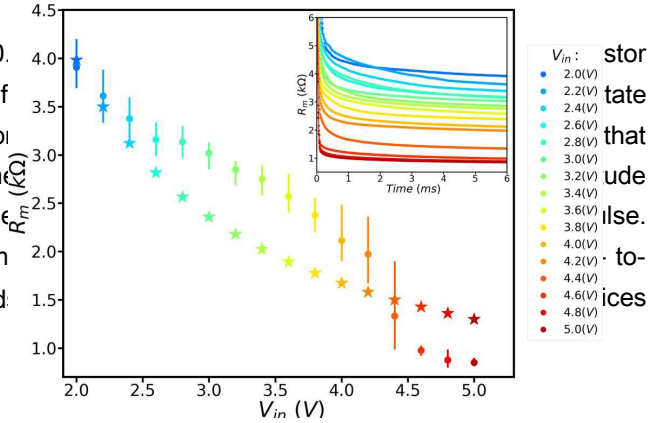


Fig4. Experimental demonstration of the $R_m = f(V_{in})$ range of achieved resistance for each applied input voltage, for a target resistance range $R_m \in [1, 4]$kΩ and different V_{in} values between 2-5V with R_s = 10kΩ. For every V_{in} the device was RESET above 7kΩ and the tuning process was repeated 50 times. The dots (experimental) correspond to mean final R_m values, whereas the vertical lines show the cycle to cycle R_m dispersion and stars (theoretical) indicate the expected R_m according to (1) using V_{SET} = 0.55V. The SET process lasted 6ms. The inset shows the mean R_m-t evolution for each applied V_{in}.

V_{SET}, its variability was tested experimentally. Figure 3 shows results for 50 i-v cycles of the VD configuration. The plot shows the measured current against the applied voltage V_{in} across the series combination of the two devices (blue curve), and also against the voltage on the memristor V_m separately. The redistribution of voltage on the two resistive elements during the switching process is evident. It can be figured out that a valid V_{SET} value is around 450-550mV (in accordance with results in Fig. 2). However, we also show the range of V_m values when a specific current value was reached while cycling (horizontal red lines; see inset of Fig. 3 for clarity), indicating the variability in V_{SET} and thus in the overall switching behavior. This is important to be considered in the VD tuning approach since it implies variability in the final R_m for a specific input V_{in}; (see Fig. 4).

III. Voltage Divider in Action

A. Tuning Performance Evaluation

In Fig. 4 we show experimental results of memristance tuning by applying different V_{in} values between 2-5V. For every V_{in} value, a triangular RESET pulse was first applied having the same negative limit with the V_{in} of the last applied SET pulse [see pulse properties in Fig. 1(c)], to initialize the device above 7kΩ. The initial R_{OFF} range is not present in (1)

so it should theoretically not affect the SET tuning result. For each V_{in} value the tuning was repeated 50 times. The dots in Fig. 4 correspond to mean final R_m values for every V_{in} after 6ms, whereas the vertical lines denote the entire R_m value range for the 50 experiments. We arbitrarily assumed the SET process was complete after 6ms, by observing the R_m-t evolution in the inset of Fig. 4, in which we also appreciate that for higher V_{in} (thus higher induced V_m-V_{SET} difference) the switching rate dR_m/dt at the beginning of the process is faster.

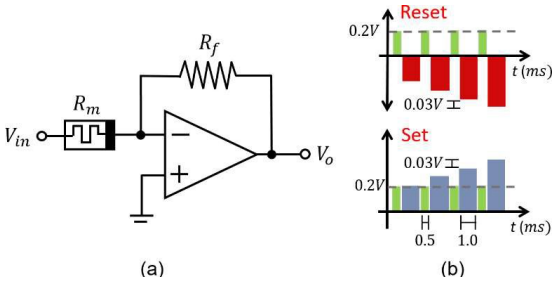
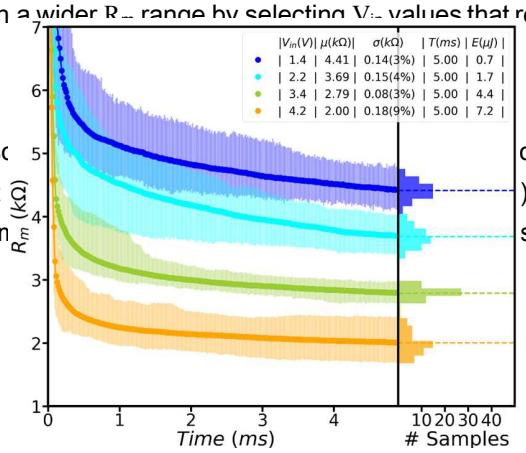


Fig. 5. (a) The circuit topology used to implement the adaptive pulse-based tuning protocol. Such transimpedance amplifier [22] used a MIC 7122YMM operational amplifier, compatible with the ±5V voltage supply provided by the Digilent AD2, and a feedback resistor R_f = 8.3kΩ to limit the current at I_{cc} = 600uA. (b) Explanation of the programming pulse properties for SET and RESET while tuning the memristor state. Read (green) pulses were 0.5-ms wide and had 0.2V amplitude. Programming SET (blue)/RESET (red) pulses were 1-ms wide and started at 0.2V, gradually increasing their amplitude by |0.03V| after every reading. Pulse separation was arbitrarily set at 0.01ms.

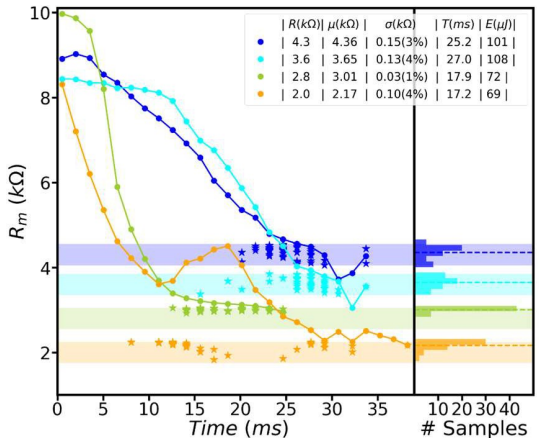
Some of the obtained R_m ranges overlap. However, by taking a closer look at Fig. 4 we figure out that: (i) the obtained ranges for every R_m are really small, highlighting the very good precision and repeatable results achieved with the VD tuning approach besides the variability in the device switching behavior; (ii) for almost the entire range of V_{in} values, we get a very good "almost linear" relation between R_m and V_{in}, which is generally desirable for ML memory and neuromorphic applications. Consequently, even for such a short R_m window, a number of easily separable ML states can be found. For a large number of separable ML states, the device can be operated in a wider R_m range by selecting V_{in} values that result in non-overlapping R_m distributions.

B. Comparison witha Pulse-Based Programming Strategy

We compared experimentally the efficiency of the VD tuning sc ccurate tuning protocol [11] in terms of the following four metrics: (i) circuit) tuning time, and (iv) energy consumption. Such protocol is based on the assun ses



(a)



(b)

Fig. 6. Tuning comparison. The plots on the left side show the average memristance evolution with time for 50 experiments carried out for every different target level (different colours), and on the right side the distribution of the final achieved state, using (a) the voltage divider and (b) the pulse-based tuning

protocol [11]. For all distributions the mean μ and standard deviation σ were calculated (% of μ is also shown), along with the average energy consumption E. Energy was computed by integrating $V_{in} \times I_{in}$ over time and in (b) includes the energy used by the op-amp. In the insets, T is tuning time.

we approach a desired R_m faster but at cruder precision, whereas smaller pulses of gradually increasing amplitude are preferred for fine tuning. In-between the gradually growing SET/RESET pulses, the device state is checked via a small read pulse. The process continues until we reach the target R_m within an acceptable distance which we arbitrarily defined as ±250Ω. However, if we overshoot the target R_m, the fine tuning starts over with pulses of opposite polarity, as explained in Fig. 5(b) for SET and RESET.

We implemented this protocol using a custom PCB and a transimpedance amplifier [22], as shown in Fig. 5(a). The V_{in} and V_o nodes are

directly connected to the Digilent AD2. For a known resistor R_f, the current is computed by measuring the output voltage V_o. In both cases, tuning started after initializing the device to a high resistive starting point above 7kΩ. For our comparison, four separable resistance ranges were selected after using first the VD. In Fig. 6(a) the left part shows the average R_m evolution with time for 50 experiments carried out for every V_{in}. The far right part presents the distribution of the achieved R_m after 5ms. The inset presents these results in the following order: applied input voltage, mean final R_m, standard deviation, tuning time (which is the same for all cases) and energy consumption.

Based on the VD tuning results, the same target R_m values were selected for the alternative tuning protocol. The results are shown in Fig. 6(b). The plots have the same form to facilitate comparison, presenting on the left side the average resistance evolution for 50 tuning experiments carried out for every target R_m, and the final R_m distribution shown on the far right side. The inset shows the tuning statistics as mentioned previously for Fig. 6(a). The only difference is that in Fig. 6(b) the first column shows the target R_m, which was purposely selected close to the mean final R_m achieved with the VD. With a more transparent tone, as a guide to the eye, we show the acceptable precision zones we defined arbitrarily for every target R_m. The dots correspond to average R_m read in-between the programming pulses. Stars denote the moment when R_m entered the target zone in every one of the 50 experiments.

By observing Fig. 6(b) we notice that the longer the distance to cover from the initial state to the desired R_m, the earlier the stars appear in the target zone. Thus the goal was achieved earlier due to the higher amplitude of the applied pulses reached through gradual increment. However, the tuning time sometimes resulted nearly 8× longer than the maximum time required by the VD to reach the same target with a very similar precision. Comparing both tuning schemes w.r.t. the selected metrics, we observe: (i) the VD is the simplest in terms of HW requirements; (ii) the precision of the pulse-based protocol is similar to that of the VD, although it could be improved by modifying the programming pulse properties. On the contrary, the VD precision is difficult to improve; (iii) the VD tuning time is much shorter compared to that required by the pulse-based protocol; (iv) the average energy consumption is very small in the VD. The largest energy observed using the VD (7.2μJ) is more than 9× smaller than the smallest energy required by the rival approach (69μJ). The latter includes the energy consumed by the op-amp.

IV. Conclusions

This brief demonstrated experimentally the validity of the memristor-resistor voltage divider (VD) for memristance tuning. The VD outperformed a pulse-based fine tuning protocol in terms of HW simplicity, tuning time and energy consumption, while achieving similar tuning precision. So, it qualifies as a simple solution for fast, reliable, and energy-efficient ML tuning for ML resistive storage systems.

Acknowledgment

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References

[1] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," Nature, vol. 453, pp. 80 - 83, 2008

[2] L. O. Chua, "Memristor - The Missing Circuit Element," IEEE Trans. Circuit Theory, vol. 18, no. 5, pp. 507-519, 1971

[3] G. Sassine, et al., "Interfacial versus filamentary resistive switching in TiO_2 and HfO_2 devices," J. Vac. Sci. Technol. vol. B34 (012202), 2016

[4] M. A. Nugent, T. W. Molter, "Thermodynamic-RAM technology stack," Int. Journal of Parallel, Emergent and Distributed Systems, vol. 33, no. 4, pp. 430-444, 2018

[5] M. Prezioso, et al., "Spike-timing-dependent plasticity learning of coincidence detection with passively integrated memristive circuits," Nature Comm., vol. 9 (5311), 14 December 2018

[6] S. Menzel, U. Böttger, M. Wimmer, and M. Salinga, "Physics of the Switching Kinetics in Resistive Memories," Adv. Funct. Mater., vol. 25, pp. 6306-6325, 2015

[7] K.-H. Jo, C.-M. Jung, K.-S. Min, and S.-M. Kang, "Self-Adaptive Write Circuit for Low-Power and Variation-Tolerant Memristors," IEEE Trans. Nanotechnol., vol. 9, no. 6, pp. 675-678, 2010

[8] R. Berdan, T. Prodromakis and C. Toumazou, "High precision analogue memristor state tuning," IET Electronics Letters, vol. 48, no. 18, pp. 1105-1107, 2012

[9] W. Yi, et al., "Feedback write scheme for memristive switching devices," Appl Phys A, vol. 102, no. 4, pp. 973–982, 2011

[10] O. A. Olumodeji, and M. Gottardi, "A pulse-based memristor programming circuit," 2017 IEEE Int. Sym. Circuits and Systems (ISCAS), Baltimore, MD, USA, May 28-31

[11] F. Alibart, L. Gao, B. D. Hoskins, and D. B. Strukov, "High precision tuning of state for memristive devices by adaptable variation-tolerant algorithm," Nanotechnology, vol. 23 (075201), 2012

[12] K. Campbell, R. Bassine, Md. Faisal Kabir, and J. Astle, "An Optically Gated Transistor Composed of Amorphous M + Ge_2Se_3 (M = Cu or Sn) for Accessing and Continuously Programming a Memristor," ACS Appl. Electron. Mater., vol. 1, no. 1, pp. 96–104, 2019

[13] I. Vourkas, et al., "Exploring the Voltage Divider Approach for Accurate Memristor State Tuning," 2017 IEEE Latin American Symp. Circuits and Syst. (LASCAS), Bariloche, Argentina, Feb. 20-23

[14] S. H. Jo, et al., "Programmable Resistance Switching in Nanoscale Two-Terminal Devices," Nano Lett., vol. 9, no. 1, pp. 496-500, 2009

[15] K. M. Kim, S. R. Lee, S. Kim, M. Chang, and C. S. Hwang, "Self- Limited Switching in Ta2O5/TaOx Memristors Exhibiting Uniform Multilevel Changes in Resistance," Adv. Funct. Mater., vol. 25, no. 10, pp. 1527–1534, 2015

[16] K. M. Kim et al., "Voltage divider effect for the improvement of variability and endurance of TaOx memristor," Sci. Reports, vol. 6 (20085), 2016

[17] T. Bunnam, A. Soltan, D. Sokolov, and A. Yakovlev, "An Excitation Time Model for General-purpose Memristance Tuning Circuit," 2018 IEEE Int. Sym. Circuits and Systems (ISCAS), Florence, Italy, May 27- 30

[18] Analog Discovery 2, "A high performance, all-in-one portable oscilloscope & instrumentation system," [Online]. Available: https://analogdiscovery.com

[19] K. Campbell, "Self-directed channel memristor for high temperature operation," Microelectron. J., vol. 1, no. 1, pp. 10–14, 2017

[20] Knowm Inc., "Neuromemristive Artificial Intelligence," [Online]. Available: https://knowm.org

[21] S. Kannan, N. Karimi, R. Karri, and O. Sinanoglu, "Modeling, Detection, and Diagnosis of Faults in Multilevel Memristor Memories," IEEE Trans. Computer-Aided Design of Integrated Circ. and Syst., vol. 34, no. 5, pp. 822-834, 2015

[22] J. Gomez, I. Vourkas, A. Abusleme, and G. Ch. Sirakoulis, "Experimental Measurements on Resistive Switching Devices: Gaining Hands-on Experience," 2018 Int. Conf. on Modern Circuits and Syst. Technol. (MOCAST), Thessaloniki, Greece, May 07-09