Analysis of Voltage Balancing Limits in Modular Multilevel Converters

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***Abstract*—The modular multilevel converter (MMC) is one of the most promising converter topologies for high-voltage applications, especially for high-voltage direct-current (HVDC) transmission systems. One of the most challenging issues associated with the MMC is the capacitor voltage variations, which if not properly controlled, result in large circulating currents flowing through the converter legs. This paper develops a mathematical model to formulate and analyze capacitor voltage variations and the circulating currents within the MMC legs. Based on the developed model, the limits to the capacitor voltage balancing task are derived and graphically presented. A set of simulation results conducted in MATLAB/Simulink environment are presented to verify the accuracy of the mathematical analysis.**

I. Introduction

Multilevel converters have attracted significant interests for medium/high power applications. Among various multilevel converter topologies [1], [2], the Modular Multilevel Converter (MMC) [3], [4] offers several salient features which make it a potential candidate for various applications including High-Voltage Direct Current (HVDC) transmission systems [5], [6], Flexible AC Transmission System (FACTS) controllers [7], and motor drives [8].

The main salient features of the MMC are the following [9], [10]:

- It is structurally scalable and can theoretically meet any voltage level requirements.
- It does not have the drawbacks of other multilevel converters, e.g., the capacitor voltage balancing task is relatively simpler and there is no requirement for isolated dc sources.

Proper operation of the MMC necessitates an active voltage balancing scheme to carry out the voltage balancing task among the capacitors of each leg. Although the capacitor voltage balancing of the MMC does not have the limitations and complexities associated with other multilevel converters [6], it still remains the main technical challenge of the MMC. The capacitor voltage balancing problem is mutually coupled with the circulating currents within each leg of the MMC, which if not properly controlled, can have adverse impact on semiconductor ratings and losses.

Research on the MMC has been mainly focused on (i) the development of Pulse-Width Modulation (PWM) techniques to carry out the voltage balancing tasks [11], (ii) analysis and control of the circulating currents flowing within each leg of the MMC [12], and (iii) steady-state and dynamic modeling/studies [13], [14]. The amplitudes of the capacitor voltage fluctuations and their impacts on the limits to the capacitor voltage balancing task have yet to be reported in the open technical literature.

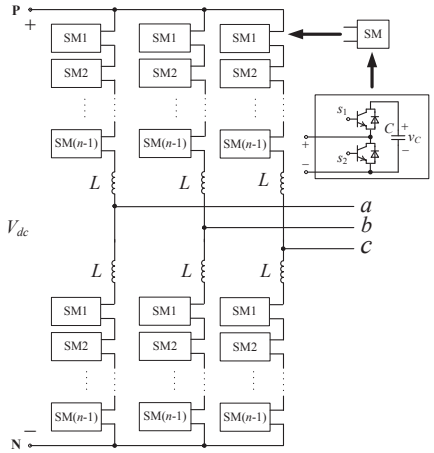

Fig. 1. Schematic representation of an n-level MMC.

The main objective of this paper is to develop a mathematical model to formulate and analyze the amplitude of the capacitor voltage fluctuations of the MMC. Based on the developed model, the limits to the capacitor voltage balance are determined. A set of simulation studies in the MATLAB/SIMULINK environment are presented to confirm the accuracy of the mathematical analysis.

The rest of this paper is organized as follows. Section II introduces the principles of operation of the MMC and develops a mathematical model. In Section III the mathematical model is used to analyze the current limits of the capacitors. In Section IV, a capacitor voltage balancing strategy is included into the mathematical model. Section V determines capacitor voltages fluctuations in a five-level MMC. Section VI reports the study results and Section VII concludes this paper.

II. MMC Structure and Basic Operation

Fig. 1 shows a circuit representation of a general n-level MMC. The MMC consists of six arms where each arm includes $n-1$ series-connected, identical, half-bridge

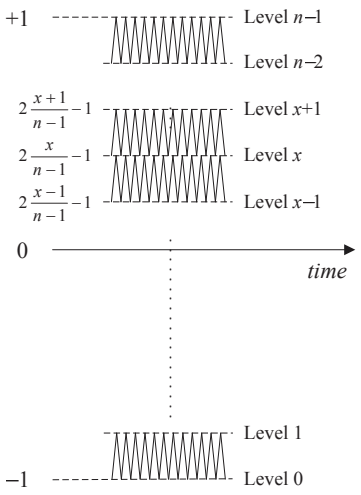

Fig. 2. Level-shifted carriers of an SPWM strategy.

SubModules (SMs). Reactors L are to provide current control within the phase arms and to limit the fault currents. The output voltage of each SM is either equal to its capacitor voltage (v_C) or zero, depending on the switching states of the switch pairs s_1 and s_2 in each SM.

To synthesize an n-level waveform at the ac-side of the converter, a phase disposition Sinusoidal PWM (SPWM) strategy is applied. The SPWM technique requires $n-1$ in-phase carrier waveforms displaced symmetrically with respect to the zero-axis [6], as depicted in Fig. 2. At any instant, out of the $2n-2$ SMs in each leg, $n-1$ modules are on. By comparing a sinusoidal reference waveform with the $n-1$ carrier waveforms, the output voltage level $x=\{0,1,...,n-1\}$ at the ac-side of the MMC is determined. The voltage level specifies the number of SMs that should be switched on in the upper and lower arms of the MMC [6].

A. MMC Analysis with an Infinite Number of SMs

To analyze the circulating currents within the MMC legs, it is assumed that the number of SMs within each arm, and consequently the number of voltage levels n, is very large. The equivalent circuit of one leg of the MMC can be represented by Fig. 3 which consists of two variable capacitors in the upper and lower arms, i.e., C_p and C_n, respectively. In this first analysis, without loss of generality and for the sake of simplicity, the inductors L and resistors R are assumed to be very small and negligible.

The value of the capacitors depends on the number of switched on SMs per each arm and, consequently, on the instantaneous value of the output voltage provided at the output of the leg ($v_{a0} \in [-\frac{V_{dc}}{2}, \frac{V_{dc}}{2}]$), where point "0" represents the dc-side mid-point. Subsequently, the values of C_p and C_n are expressed by:

$$\begin{cases} C_p = \frac{2C}{(n-1)(1-\frac{v_{a0}}{V_{dc}/2})} & \text{and} \\ C_n = \frac{2C}{(n-1)(1+\frac{v_{a0}}{V_{dc}/2})}, \end{cases} \tag{1}$$

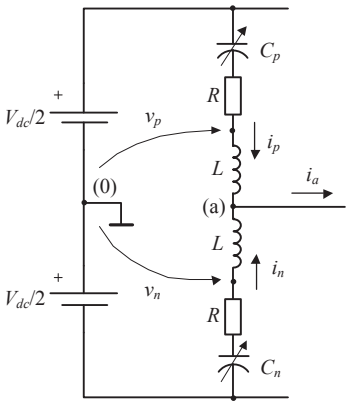

Fig. 3. Equivalent circuit of each phase of the MMC.

where C is the capacitance value of each SM capacitor. Since n is assumed to be large, the output voltage can be approximated by a continuous waveform. Thus, the following assumption can be made:

$$\frac{v_{a0}}{V_{dc}/2} \approx v_{am}, \tag{2}$$

where $v_{am} \in [-1,1]$ is the modulation signal of the leg. Substituting for $\frac{v_{a0}}{V_{dc}/2}$ from (2) in (1) yields

$$\begin{cases} C_p = \frac{2C}{(n-1)(1-v_{am})} & \text{and} \\ C_n = \frac{2C}{(n-1)(1+v_{am})}. \end{cases} \tag{3}$$

The phase current i_a is shared between the upper and the lower arms based on the following equation:

$$\begin{cases} i_p = i_a \frac{C_p}{C_n+C_p} & \text{and} \\ i_n = i_a \frac{C_n}{C_n+C_p}. \end{cases} \tag{4}$$

Substituting for C_p and C_n from (3) in (4), the capacitor currents can be represented by:

$$\begin{cases} i_p = i_a \frac{1+v_{am}}{2} & \text{and} \\ i_n = i_a \frac{1-v_{am}}{2}. \end{cases} \tag{5}$$

The sinusoidal modulation signal v_{am} and phase current i_a are expressed by:

$$v_{am} = m_a cos(\omega t) \quad \text{and} \tag{6}$$

$$i_a = \hat{I_a} cos(\omega t + \phi), \tag{7}$$

where m_a represents the converter modulation index.

Substituting for v_{am} and i_a from (6) and (7) into (5), the capacitor currents are expressed as

$$i_p = \frac{\hat{I_a}}{2} cos(\omega t + \phi) + \frac{m_a \hat{I_a}}{4} cos(2\omega t + \phi) + \frac{m_a \hat{I_a}}{4} cos(\phi), \tag{8}$$

and

$$i_n = \frac{\hat{I_a}}{2} cos(\omega t + \phi) - \frac{m_a \hat{I_a}}{4} cos(2\omega t + \phi) - \frac{m_a \hat{I_a}}{4} cos(\phi). \tag{9}$$

The first term in (8) and (9) is equal to half of the phase current. Therefore, the upper and lower arms share the output current i_a equally. The second and the third terms in (8) and (9) represent a circulating current and a dc current within the upper and lower arms, respectively. The dc component is the only component associated with active power exchange between the dc-side and the ac-side of the MMC.

The instantaneous power at the dc side of the MMC is:

$$p_{dc} = V_{dc} i_p. \tag{10}$$

The real power is calculated by:

$$P_{dc} = \frac{1}{T}\int_0^T p_{dc} dt = \frac{m_a \frac{V_{dc}}{2}}{\sqrt{2}} \frac{\hat{I_a}}{\sqrt{2}} cos(\phi), \tag{11}$$

or equivalently,

$$P_{dc} = V_{arms} I_{arms} cos(\phi) = P_{ac}, \tag{12}$$

where V_{arms} and I_{arms} are the rms values of the ac-side voltage and current, respectively.

In case of a balanced three-phase operation, the extracted current from the dc side of the MMC will be a dc component and the circulating currents within the three-phase legs are cancelled out.

B. MMC Analysis with a Finite Number of SMs

This section analyzes the leg currents based on the assumption that the MMC has $2n-2$ SMs per leg, where n is a finite number. In this analysis, arm inductors with intrinsic series-connected resistors are considered. Fig. 3 shows the equivalent circuit of each phase of the MMC. The following expressions give the current in the upper and lower arms, respectively:

$$i_p = \frac{i_a}{2} + \frac{1}{2L}\int_0^t (v_p - v_n) dt + I_{p0} \quad \text{and} \tag{13}$$

$$i_n = \frac{i_a}{2} - \frac{1}{2L}\int_0^t (v_p - v_n) dt + I_{n0}, \tag{14}$$

where I_{p0} and I_{n0} are the initial values of the arm currents i_p and i_n, respectively. The voltages v_p and v_n in (13) and (14) are calculated as follows:

$$v_p = \frac{V_{dc}}{2} - \sum_{j=1}^{n-1} (v_{Cpj} s_{pj}) - R i_p \quad \text{and} \tag{15}$$

$$v_n = -\frac{V_{dc}}{2} + \sum_{j=1}^{n-1} (v_{Cnj} s_{nj}) - R i_n \tag{16}$$

where s_{pj} and s_{nj} are the switching functions of the SMs in the upper and lower arms, respectively, and are equal to unity when the corresponding SM is activated; otherwise, they are zero. The state of the switching functions is determined by the particular modulation strategy used in the converter. v_{Cpj} and v_{Cnj} represent the capacitor voltages of the upper and lower SMs and are given by:

$$v_{Cpj} = \frac{1}{C}\int_0^t i_p s_{pj} dt + V_{Cp0j} \quad \text{and} \tag{17}$$

$$v_{Cnj} = \frac{1}{C}\int_0^t (-i_n) s_{nj} dt + V_{Cn0j}, \tag{18}$$

where V_{Cp0j} and V_{Cn0j} are the initial values of the capacitor voltages.

By applying the locally-averaged operator to the arm current equations in (13) and (14), we deduce:

$$\overline{i_p} = \frac{\overline{i_a}}{2} + \frac{1}{2L}\int_0^t (\overline{v_p} - \overline{v_n}) dt + I_{p0} \quad \text{and} \tag{19}$$

$$\overline{i_n} = \frac{\overline{i_a}}{2} - \frac{1}{2L}\int_0^t (\overline{v_p} - \overline{v_n}) dt + I_{n0}. \tag{20}$$

The locally-averaged voltages $\overline{v_p}$ and $\overline{v_n}$ can be expressed as:

$$\overline{v_p} = \frac{V_{dc}}{2} - \sum_{j=1}^{n-1} (\overline{v_{Cpj}} d_{pj}) - R\overline{i_p} \quad \text{and} \tag{21}$$

$$\overline{v_n} = -\frac{V_{dc}}{2} + \sum_{j=1}^{n-1} (\overline{v_{Cnj}} d_{nj}) - R\overline{i_n}, \tag{22}$$

where $d_{pj} \in [0,1]$ and $d_{nj} \in [0,1]$ are the duty cycles of the respective SMs and are determined by the modulation strategy. Finally, the locally-averaged capacitor voltages can be calculated as follows:

$$\overline{v_{Cpj}} = \frac{1}{C}\int_0^t \overline{i_p} d_{pj} dt + V_{Cp0j} \quad \text{and} \tag{23}$$

$$\overline{v_{Cnj}} = \frac{1}{C}\int_0^t (-\overline{i_n}) d_{nj} dt + V_{Cn0j}. \tag{24}$$

Equations (19) and (20) in conjunction with (21) to (24), define the locally-averaged model of the MMC. These equations can be used to determine the currents going through the upper and lower arms of the converter, and also to analyze the capacitor voltage fluctuations.

It should be pointed out that the system dynamic of the averaged model changes according to a parameter k, which is defined as:

$$k = \omega^2 LC. \tag{25}$$

It can be demonstrated that all the systems with the same value of k will perform equally, provided that the value of the resistor R is negligible. k is a parameter that will be defined to demonstrate the results associated with the dynamic behavior of the MMC.

III. SM Capacitor Current Control

In order to determine the capability of the system to control the current flowing through each of the SM capacitors, and consequently the capacitor voltage of each SM, two extreme conditions are considered and discussed in this Section. Those extreme conditions happen when the current flowing through a capacitor of a particular SM is either at its maximum or minimum value.

First, assume the case that the upper arm current is positive, i.e., $\overline{i_p} > 0$, within the time interval from t_0 to t_1. Under this condition, if any of the SMs within the upper arm is

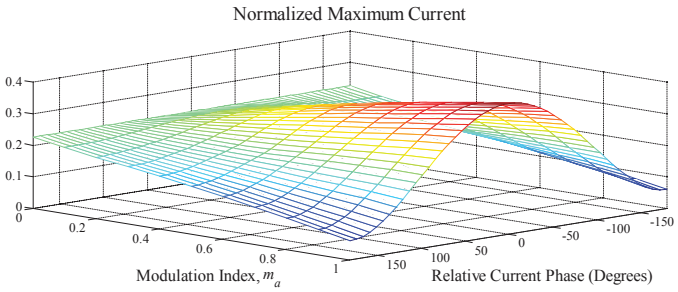

Fig. 4. Normalized maximum average current in a SM capacitor of a five-level converter calculated over one fundamental period (T) and for $k = 0.00987$.

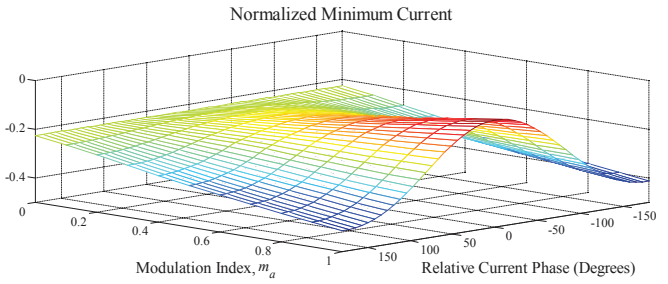

Fig. 5. Normalized minimum average current in a SM capacitor of a five-level converter calculated over one fundamental period (T) and for $k = 0.00987$.

switched on, the upper arm current $\overline{i_p}$ will flow through the SM capacitor. Consequently, the average value of the SM capacitor current over one fundamental period is calculated as follows:

$$I_{Cpmax} = \frac{1}{T}\int_{t_0}^{t_1} \overline{i_p} dt \tag{26}$$

where $\overline{i_p}$ is given by (19).

Fig. 4 illustrates the normalized maximum average current that can flow through each SM capacitor in a five-level converter, for all of the possible operating conditions in terms of the modulation index and ac-side power factor. The vertical axis of Fig. 4 represents the current which is normalized with respect to the rms value of the ac-side current, i.e., I_{Cpmax}/I_{arms}. The values of L and C are chosen such that parameter k is set at $k = 0.00987$. Fig. 4 illustrates the capability of the system to impose a positive current into the SM capacitor. As depicted, the current is always positive, which means that increasing the voltage of a SM capacitor is possible under any operating condition of the MMC. This figure quantifies the maximum average current that can be imposed into an SM capacitor for voltage balancing purposes.

Similarly, Fig. 5 shows the results when the conditions to achieve the minimum current in an upper-cell capacitor are imposed. In this case, the average SM capacitor current over a fundamental period is calculated as follows:

$$I_{Cpmin} = \frac{1}{T}\int_{t_1}^{t_2} \overline{i_p} dt, \tag{27}$$

being $[t_1, t_2]$ the time interval when $\overline{i_p} < 0$.

Observe that in this case an average negative current is achieved for any operating conditions. Fig. 4 and Fig. 5 show that, if properly controlled, the system is stable.

IV. Voltage Balancing Task

Assuming that the switching frequency of the MMC is high, the SM voltages balancing task is achieved if all of the individual SMs in the upper arm are switched on with equal duty cycles. Since for the majority of voltage levels, there are switching redundancies, to achieve the voltage balancing task, all of the possible switching combinations must be used which, practically, from the standpoint of the switching frequency of the switches, is not desired. However, this facilitates the voltage balancing task among the SMs. Based on this assumption, all of SMs in the upper arm will be switched on with the same duty cycle ($d_{pj} \approx d_p$), and the same happens to the SMs in the lower arm of the leg ($d_{nj} \approx d_n$). Consequently, the voltages and currents of the SM capacitors can be considered approximately the same within each arm of the leg:

$$v_{Cpj} \approx v_{Cp}, v_{Cnj} \approx v_{Cn}, i_{Cnj} \approx i_{Cn}, \text{ and } i_{Cpj} \approx i_{Cp}. \tag{28}$$

Equations (21) and (22) become:

$$\overline{v_p} \approx \frac{V_{dc}}{2} - (n-1)\overline{v_{Cp}} d_p - R\overline{i_p} \quad \text{and} \tag{29}$$

$$\overline{v_n} \approx -\frac{V_{dc}}{2} + (n-1)\overline{v_{Cn}} d_n - R\overline{i_n}, \tag{30}$$

with

$$\overline{v_{Cp}} = \frac{1}{C}\int_0^t \overline{i_p} d_p dt + V_{Cp0} \quad \text{and} \tag{31}$$

$$\overline{v_{Cn}} = \frac{1}{C}\int_0^t (-\overline{i_n}) d_n dt + V_{Cn0}. \tag{32}$$

The duty cycles of the modules are given by:

$$d_p = \sum_{x=1}^{n-1} d_x p_{px} \quad \text{and} \tag{33}$$

$$d_n = \sum_{x=1}^{n-1} d_x p_{nx}, \tag{34}$$

where $d_x \in [0, 1]$ is the duty cycle of an output voltage level x. In an SPWM-based n-level MMC, as depicted in Fig. 2, the duty cycle d_x can be obtained as follows:

for $2\frac{x}{n-1} - 1 \leq v_{am} \leq 2\frac{x+1}{n-1} - 1$:

$$d_x = (x+1) - (n-1)\frac{v_{am}+1}{2}, \tag{35}$$

and for $2\frac{x-1}{n-1} - 1 \leq v_{am} \leq 2\frac{x}{n-1} - 1$:

$$d_x = (n-1)\frac{v_{am}+1}{2} - (x-1). \tag{36}$$

The variables p_{px} and p_{nx} in (33) and (34) are the probabilities that a specific module in the upper and lower arms,

respectively, is turned on when the converter provides an output level x. Under the assumption of the same duty cycle for the SM within the upper arm and the lower arm, these probabilities depend on the switching redundancies and the number of switching combinations, and are given by:

$$p_{px} = \frac{\binom{n-2}{n-2-x}}{\binom{n-1}{n-1-x}} = \frac{n-1-x}{n-1} \quad \text{and} \tag{37}$$

$$p_{nx} = \frac{\binom{n-2}{x-1}}{\binom{n-1}{x}} = \frac{x}{n-1}. \tag{38}$$

Therefore, (33) and (34) become:

$$d_p = \frac{1}{n-1}\sum_{x=1}^{n-1} d_x(n-1-x) = \frac{1-v_{am}}{2} \quad \text{and} \tag{39}$$

$$d_n = \frac{1}{n-1}\sum_{x=1}^{n-1} d_x x = \frac{1+v_{am}}{2}. \tag{40}$$

Considering (39) and (40), from (29) to (32) are re-written as

$$\overline{v_p} \approx \frac{V_{dc}}{2} - (n-1)\overline{v_{Cp}}\frac{1-v_{am}}{2} - R\overline{i_p}, \tag{41}$$

$$\overline{v_n} \approx -\frac{V_{dc}}{2} + (n-1)\overline{v_{Cn}}\frac{1+v_{am}}{2} - R\overline{i_n}, \tag{42}$$

$$\overline{v_{Cp}} = \frac{1}{C}\int_0^t \overline{i_p}\frac{1-v_{am}}{2}dt + V_{Cp0}, \quad \text{and} \tag{43}$$

$$\overline{v_{Cn}} = \frac{1}{C}\int_0^t (-\overline{i_n})\frac{1+v_{am}}{2}dt + V_{Cn0}. \tag{44}$$

Equations (41) to (44), together with (19) and (20), represent the locally-averaged mathematical model that includes an active capacitor voltage balancing strategy.

V. Capacitor Voltages Balancing Limits

The proposed locally-averaged model with the voltage balancing strategy can be used to evaluate the amplitude of the capacitor voltage fluctuations of each SM. Optimal balancing conditions are considered since all the SMs are activated with equal duty cycles while providing any specific output voltage level. Therefore, any voltage unbalance is shared among all the capacitors equally. To analyze and demonstrate the SM capacitor voltage fluctuations, a set of studies are conducted on a five-level converter.

The amplitude of the capacitor voltage fluctuations, $\Delta V_{NP}/2$, is normalized with respect to the capacitor value (C), the rms value of the phase current I_{arms}, and the output frequency f, as follows:

$$\frac{\Delta V_{NPn}}{2} = \frac{\Delta V_{NP}/2}{I_{arms}/fC}. \tag{45}$$

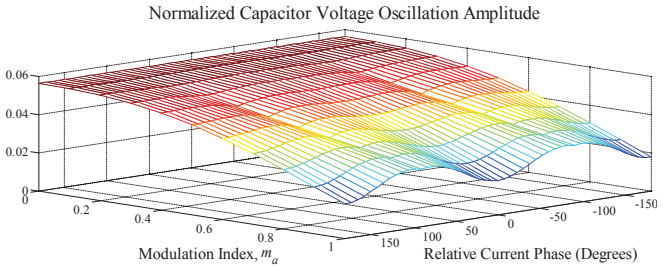

Fig. 6. Normalized amplitude of the capacitor voltages fluctuations of a five-level converter.

The capacitor voltage variations/fluctuations are determined for all of the possible operating conditions in terms of the modulation index and the ac-side power factor. Fig. 6 shows the variations of the capacitor voltages in a five-level converter for $k = 0.00987$. As depicted in Fig. 6, for the operating conditions with high modulation indices, the amplitude of the capacitor voltage fluctuations is smaller. When the MMC operates with a high modulation index, the ac-side voltage is synthesized mostly with the highest and the lowest voltage levels. Consequently, the upper and lower extreme voltage levels with large duty cycles are generated. To synthesize any of those voltage levels, all of SMs either in the upper or lower arms are bypassed and the ac-side terminal is directly connected to the upper or lower dc-side terminal, respectively. Therefore, the SMs are bypassed and no current flows through the SM capacitors. In contrast, when the converter synthesizes the middle voltage level at the ac-side terminal, i.e, zero voltage at the output which is equal to the dc-side mid-point voltage, out of $n-1$ SMs in each arm, half of them are switched on and the ac-side current flows through them. As illustrated in Fig. 6, this is the worst case scenario in terms of the capacitor voltage variations of the capacitor voltages.

VI. Simulation Results

To demonstrate the accuracy of the analytical MMC model, a set of simulation studies have been conducted on a five-level converter in MATLAB-SIMULINK environment. The dc side of the converter is supplied by a constant dc source and, the ac-side current is provided by a single-phase current source. The switching frequency is f_{sw} =4 kHz.

Figs. 7 and 8 show the SM current and capacitor voltage variations under the operating conditions corresponding to m_a=1 and the ac-side power factors of unity and zero (pure real and reactive power exchange), where $k = 0.00987$ and $k = 0.789$, respectively. Each figure depicts the analytical (in blue color) and exact (in red color) simulation-based current and capacitor voltage waveforms.

The analytical waveforms closely match with their corresponding exact simulation. Therefore, the simulation results verify the accuracy of the mathematical analysis.

VII. Conclusion

This paper analyzes the capacitor voltage variations of the MMC. The paper develops a mathematical model to formulate

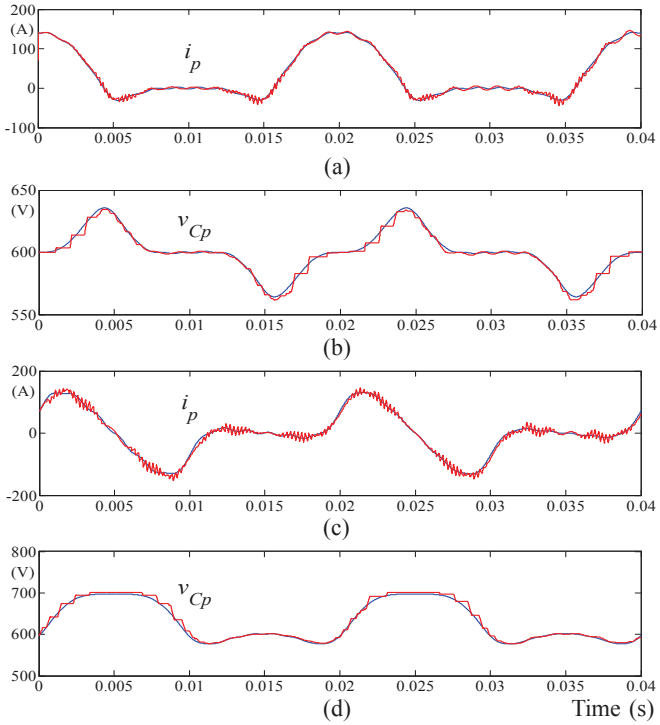

Fig. 7. Simulation results of a five-level converter with $k = 0.00987$ under the operating condition of m_a=1: (a,b) analytical and exact results at unity power factor operation, and (c,d) analytical and exact results at zero power factor operation.

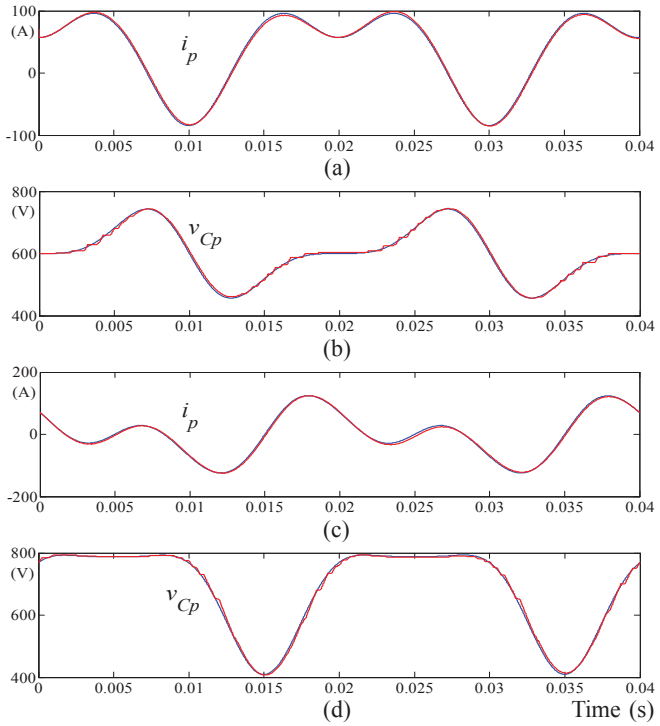

Fig. 8. Simulation results of a five-level converter with $k = 0.789$ under the operating condition of m_a=1: (a,b) analytical and exact results at unity power factor operation, and (c,d) analytical and exact results at zero power factor operation.

the capacitor voltage variations of the MMC. Based on the developed model, the limits to the capacitor voltage balancing task are determined and investigated. A set of simulation studies in the MATLAB/Simulink environment are presented to confirm the accuracy of the mathematical analysis.

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