

Ring oscillator switching noise under NBTI wearout

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Abstract—In this paper the switching noise of a CMOS ring oscillator has been analysed when their pFETs are subjected to negative bias temperature instability (NBTI). The impact of pFET under NBTI has been experimentally quantified whereas CMOS ring oscillator frequency and the switching noise has been analysed by means of electrical full-model simulation. The results show that the impact on the electromagnetic compatibility behaviour increases with NBTI wearout.

Keywords: Switching Noise, EMC prediction, CMOS circuits, NBTI

I. INTRODUCTION

The continuous scaling of CMOS circuit has set the MOSFET transistor in the nanoelectronic era. In this context, the functionality and complexity of integrated circuits (IC) are growing up. However, the operation voltage is reduced. The higher complexity of current ICs has allowed including electronic system in a lot of safety critical applications (*i.e.*, automotive, aeronautics and/or medical application). Therefore, the functionality of the electronic equipment must be assured and the risk of electromagnetic interference (EMI) must be reduced during their lifetime.

Nowadays, circuits' robustness to electromagnetic interference is checked in a burn-in component [1], without taking into account the impact of the natural devices' aging. However, shrunk dimensions cause the appearance of several time dependent failure mechanisms, which can limit the functionality of the circuits and modify their electromagnetic behaviour. Therefore, the time dependence of electromagnetic behaviour, which is known as Electromagnetic Robustness or Electromagnetic Reliability (EMR) [1], should be evaluated.

Negative bias temperature instability (NBTI) is one of the main time dependent reliability problems. It is mainly accepted that NBTI is ascribed to the formation of Si/SiO₂ interface states and the oxide positive charge [2]. Regarding to this problem, the dominating work has been concentrated on discrete transistor parameter shift, rather than on circuit performance. At device level, it has been demonstrated that NBTI effect on pFET is manifested as a gradually increase of the threshold voltage (V_{th}). Therefore, the drive current is reduced [3]. The NBTI under static and dynamic conditions has also been reported. These investigations show that the voltage threshold shift (ΔV_{th}) under dynamic stress is almost half of DC case, due to the recovery properties of NBTI [4]. At circuit level, the NBTI effects have not been deeply investigated. However, some works have pointed out that NBTI provoke a

signal noise margin (SNM) reduction on SRAM cell [5]. Therefore a certain impact on the electromagnetic compatibility (EMC) behaviour of circuits based on CMOS technology should be expected.

The switching noise is probably one of the main EMC emission problems in CMOS circuits. It is well known that switching noise is a common impedance coupling [6]. Therefore, an evaluation of switching noise under wearout mechanisms is required in order to know whether the circuits can hold his functionality along their lifetime. In this paper, the impact of NBTI on the switching noise behaviour of a ring oscillator has been analysed.

The paper is structured as follows: in Section II the impact of this failure mechanism on a single pFET is obtained experimentally and the voltage threshold shift is experimentally quantified. In Section III, the impact of NBTI on the ring oscillator behaviour and switching noise has been evaluated through electrical simulation, using the data measured on Section II. In Section IV, the conclusions are summarized.

II. MEASURING THE IMPACT OF NBTI ON pFET

First of all, the experimental procedure starts by measuring the voltage threshold shift (ΔV_{th}) due to NBTI on a single pFET. In order to proceed, a stress-measure-stress sequence has been followed in the experiment, with exponential increasing periods of time. During the test stage, the I_D - V_{GS} pFET (aspect ratio $2\mu\text{m}/0.13\mu\text{m}$) characteristic has been measured. During the NBTI stress phase, a constant voltage of 0V has been applied to the pFET gate and the rest of the terminals have been biased at 2V. In order to accelerate the NBTI effects the experiments have been done at 125°C

In Fig. 1 the I_D - V_{GS} pFET behaviours at different stress time is plotted. As it is shown, a voltage threshold shift (ΔV_{th}) is produced in the transistor due to NBTI effect. The ΔV_{th} time dependence shows a power law dependence with slope 1/6, as depicted in Fig. 2, according to expression (1), which matches with the theoretical prediction [2].

$$\Delta V_{TH} = 12 \cdot 10^{-3} \cdot t^{\frac{1}{6}} \quad (1)$$

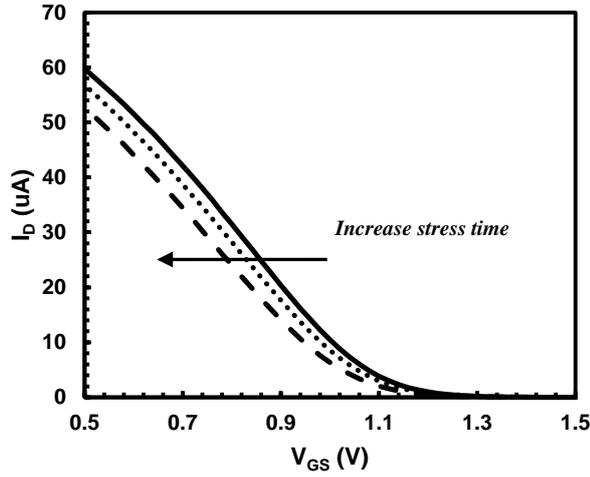


Fig. 1. I_D - V_{GS} behaviour of pFET for different stress time

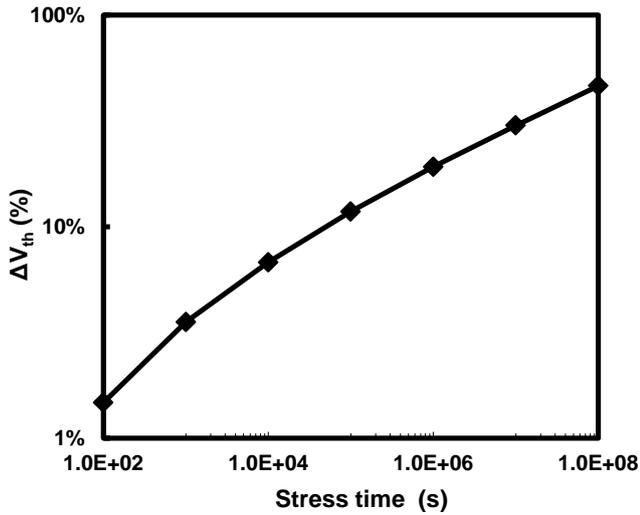


Fig. 2. ΔV_{th} of single pFET against NBTI stress time.

III. RING OSCILLATOR BEHAVIOUR UNDER NBTI

A. Schematic set-up

The schematic of the ring oscillator under evaluation is depicted in

Fig. 3. The oscillator is based on 40 inverters and 2 input NAND gate (the NAND gate is included as enable). The aspect ratios for the CMOS inverters are $1.0\mu\text{m}/90\text{nm}$ and $3\mu\text{m}/90\text{nm}$ for nFET and pFET, respectively. Moreover a standard RLC network has been included on V_{CC} and GND in order to model the parasitic package effect. The ring oscillator has been simulated with commercial *Agilent ADS* software. The BSIM4 model extracted from PTM website [7] has been used and the voltage threshold shift of the pFET has been shifted following the time dependence response obtained experimentally (Fig. 2).

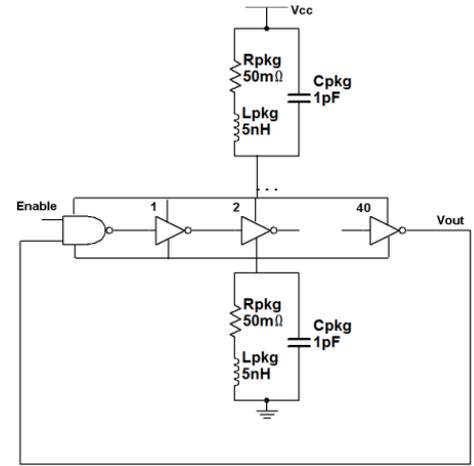


Fig. 3. Schematic of the ring oscillator under evaluation.

B. Oscillation frequency

In order to validate the proposed methodology, the ring oscillator functionality has been evaluated under different stress times. Fig. 4 shows the ring oscillator output voltage without stress and after applying stress during 10^8 seconds. Although in both cases the ring oscillator is working, the frequency oscillation is reduced about 10%, from 1.56GHz to 1.36GHz after stress. In Fig. 5 the ring oscillator reduction against stress time is shown.

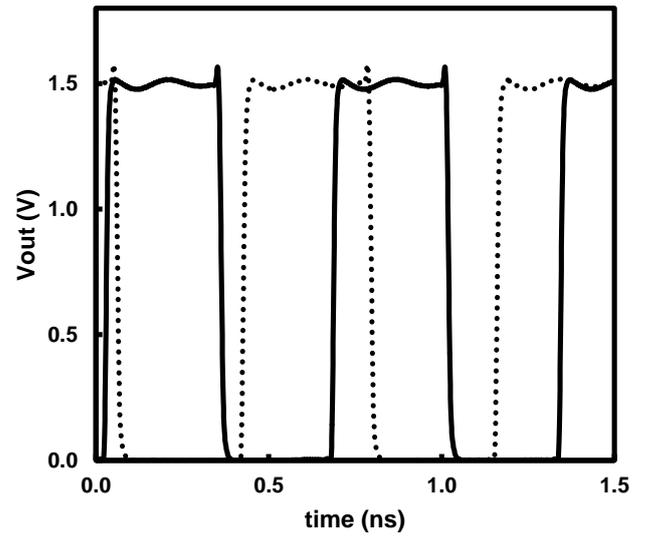


Fig. 4. Voltage output of ring oscillator behaviour before (continuous line) after 10^8 s stress (dot line).

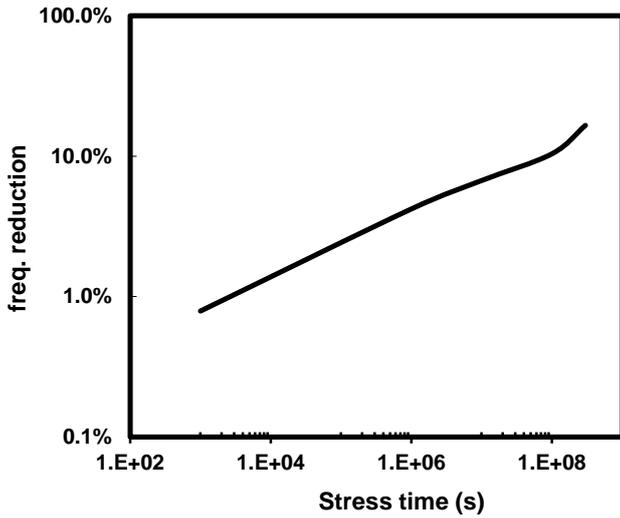


Fig. 5. Ring oscillator frequency reduction with regard to fresh device against stress time.

C. Switching Noise

Due to the CMOS inverter switching and his common impedance, the ring oscillator provokes a fluctuation on current consumption, which can affect other parts of the circuits. In Fig. 6 the ring oscillation current consumption is shown without stress and after applied 10^8 seconds stress. A reduction in the average current consumption is observed after applied stress, which is expected theoretically due the ring oscillator frequency reduction. Moreover, the current consumption presents fluctuations due to the switching noise. In order to evaluate the impact of NBTI on theses fluctuations the maximum fluctuation (I_{CC_PP}) has been used has a figure of merit. In Fig. 7 the maxim fluctuation, (*i.e.*, peak to peak current consumption) against stress time is shown. The peak to peak current consumption remains roughly constant with stress time. However, due to the reduction on the average current consumption (Fig.7) the ratio between fluctuation and average current is increased with stress time, which is plotted in Fig.8. Specifically after 3 years working, the weight of the fluctuation current over the average consumption current ratio is increased in a 10%. Therefore, the aging of these kinds of CMOS circuits has to be taken into account in order to predict their EMC behaviour during its lifetime.

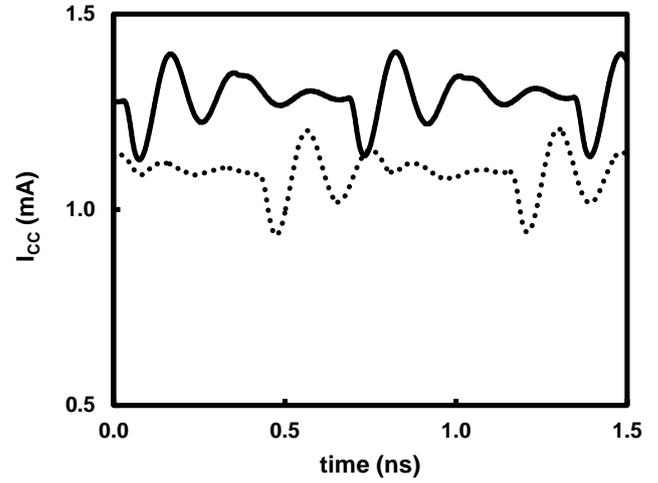


Fig. 6. Ring oscillator current consumption before (continuous line) after 10^8 s stress (dot line).

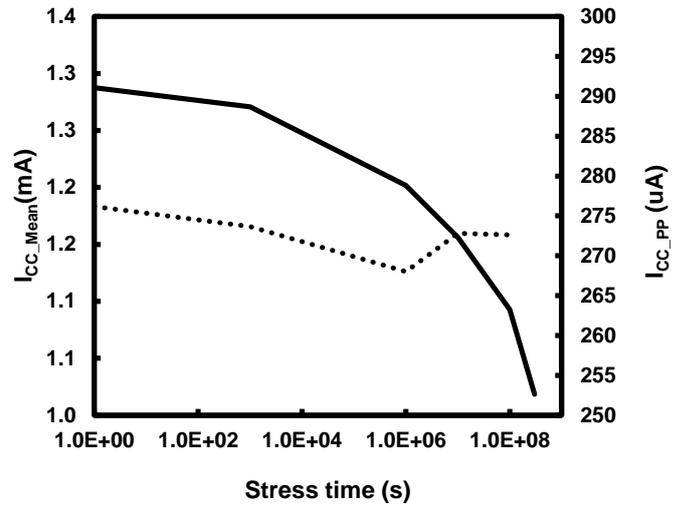


Fig. 7. Ring oscillator current consumption against stress time. Continuous line: mean current consumption (I_{CC_mean}). Dot line: maximum peak to peak current consumption (I_{CC_PP}).

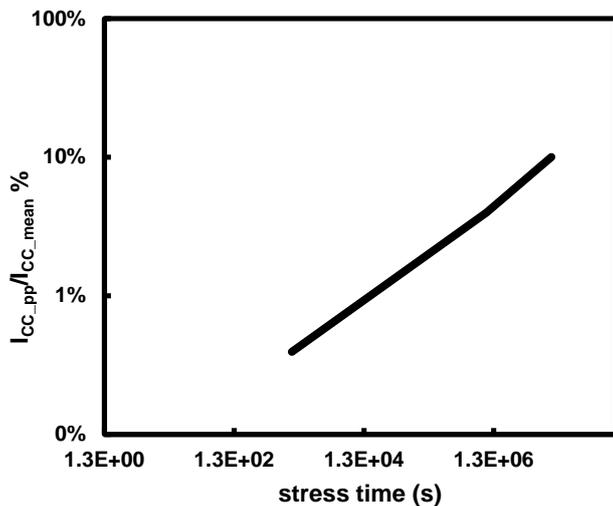


Fig. 8. Peak to peak current-mean current ratio against stress time.

IV. CONCLUSIONS

In this paper, the ring oscillator behaviour under NBTI wearout has been evaluated.. Specifically, the NBTI effect on switching noise has been evaluated. After 3 years NBTI stress, the ring oscillator is still working, with a reduction about 10% of the oscillation frequency. Therefore, a current consumption reduction is observed. Since the average current consumption is reduced with stress time whereas the peak to peak fluctuation remains constant, the impact on the electromagnetic compatibility behaviour increases with NBTI wearout.

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REFERENCES

- [1] Ben Dhia, S.; Ndoye, A.C.; Boyer, A.; Guillot, L.; Vrignon, B., "IC emission spectrum drifts after burn-in cycles," *Electromagnetic Compatibility and 19th International Zurich Symposium on Electromagnetic Compatibility*, 2008. APEMC 2008. Asia-Pacific Symposium on, vol., no., pp.255-258, 19-23 May 2008.
- [2] M. A. Alam, S. Mahapatra, A comprehensive model of PMOS NBTI degradation, *Microelectronics Reliability*, Volume 45, Issue 1, January 2005, Pages 71-81.
- [3] J.H. Stathis, S. Zafar, The negative bias temperature instability in MOS devices: A review, *Microelectronics and Reliability*, Volume 46, Issues 2-4, February-April 2006, Pages 270-286.
- [4] R. Fernandez, B. Kaczer, A. Nackaerts, S. Demuynck, R. Rodriguez, M. Nafria, G. Groeseneken; AC NBTI studied in the 1 Hz ý 2 GHz range on dedicated on-chip CMOS circuits, *IEDM Tech. Digest*, p. 1 (2006).
- [5] K. Kang, H. Kufluoglu, K. Roy, M. Alam ; Impact of Negative-Bias Temperature Instability in Nanoscale SRAM Array: Modeling and Analysis, *Computer-Aided Design of Integrated Circuits and Systems*, *IEEE Transactions on* , vol.26, no.10, pp.1770-1781, Oct. 2007
- [6] S. Ben Dhia, M. Ramdani, E. Sicard, *Electromagnetic Compatibility of Integrated Circuits*, Springer, 2005, ISBN 0-387-26600-3
- [7] <http://www.eas.asu.edu/~ptm>