

An Enhanced Switching Policy for Buck-Derived Multi-Level Switching Power Amplifiers

Albert Garcia i Tormo, Alberto Poveda, Eduard Alarcón
 Department of Electronic Engineering
 Technical University of Catalunya
 08034 Barcelona, Spain
 E-mail: agarcia@eel.upc.edu

Henk Jan Bergveld, Berry Buter, Ravi Karadi
 NXP Semiconductors, Corporate I&T, Research
 High Tech Campus 32
 5656AE Eindhoven, The Netherlands

Abstract—This work proposes a switching policy for multi-level full-bridge switching power converters and analyses their performance by driving them with a multi-level PWM modulation, targeting high-efficiency power amplifiers. Unlike conventional policies, which generate the output voltage levels only from the values of the supply voltages, this enhanced policy also uses the values of the voltage difference between supply voltages to generate additional output voltage levels, therefore maximising the number of output voltage levels for a given set of supply voltages and connection switches. Simulation results show that, when tracking a band-limited signal, the proposed switching policy can reduce the power of the high-frequency spectral content from 21 % to 11 % by upgrading a 5-level amplifier to a 7-level amplifier without adding supply voltages or connection switches.

I. INTRODUCTION AND MOTIVATION

Switching amplifiers are becoming the most popular power amplifiers in almost all applications [1], [2]. Their high efficiency and reduced size make them very suitable not only for mobile applications, wherein size and power consumption are key features, but also for high-power applications, because of reliability and the size and weight (i.e. cost) of the heat sink.

In both high and low-power applications, the external LC filter has a significant impact upon the amplifier size, cost and efficiency, since the inductors are in the power path. In pursuit of simplifying the filtering process, and thereby improve these features, this work explores multi-level amplification.

By using a multi-level output stage, the power of the high-frequency components, i.e. the spectral content at frequencies beyond the reference signal bandwidth, is reduced. Therefore less filtering effort is required to achieve the desired performance. If enough levels are used, even filter-less amplification becomes feasible.

The performance of multi-level amplification improves as the number of levels increase [1], although this increase generally involves adding supply voltages and connection switches. The proposed switching policy allows maximising the number of output voltage levels without adding connection switches, for a given set of supply voltages.

Most devices include a power-management unit which provides several supply voltages (Figure 1). A multi-level amplifier can take advantage of any available supply voltage present in a certain system, yet by employing the proposed switching policy it is possible to take further advantage of all the available power resources.

In section II, two multi-level converter topologies for switching amplifiers are presented and analysed, as well as the proposed switching policy. In order to take advantage of this policy and drive the multi-level converters as amplifiers, a native multi-level modulation must be used (section III). The performance achieved by the multi-level amplifiers employing the proposed switching policy is characterised

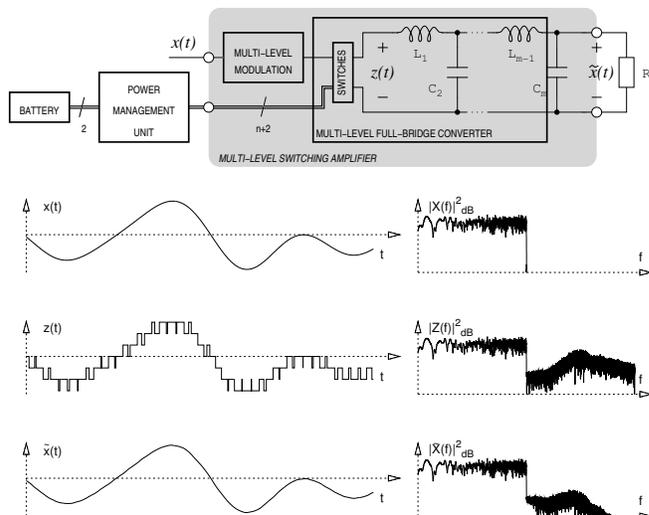


Figure 1. m -th order multi-level switching amplifier using $n + 2$ supply voltages: block diagram and significant waveforms (7-level example).

and compared with state-of-the-art multi-level amplifiers (section IV). Finally conclusions are drawn (section V).

In what follows, the signal to track and power-amplify (amplifier input) is denoted reference signal or $x(t)$, the discrete-amplitude signal (the signal supplied by the switches at the input of the power filter) is denoted encoded signal or $z(t)$ and the output signal (amplifier output) is denoted recovered signal or $\tilde{x}(t)$, see Figure 1.

II. MULTI-LEVEL CONVERTER TOPOLOGIES FOR SWITCHING AMPLIFIERS AND PROPOSED SWITCHING POLICY

Conventional switching amplifiers are based on a buck or a full-bridge converter, because they are linear. Similarly, the multi-level amplifiers are based on the multi-level version of a buck or a full-bridge converter.

Both the buck and the full-bridge converters use both the ground voltage and the supply voltage (namely GND and V_0^s) provided by the power supply to generate, through connection switches, a 2-level discrete-amplitude signal which is subsequently filtered out by a low-pass LC filter. The output of this filter is connected to the load. The multi-level versions of these converters add connection switches between the input of the filter and each additional supply voltage, so that the discrete-amplitude signal may comprise more levels.

In what follows, for the sake of notation simplicity, both the reactive filter and the load have been merged into a complex load

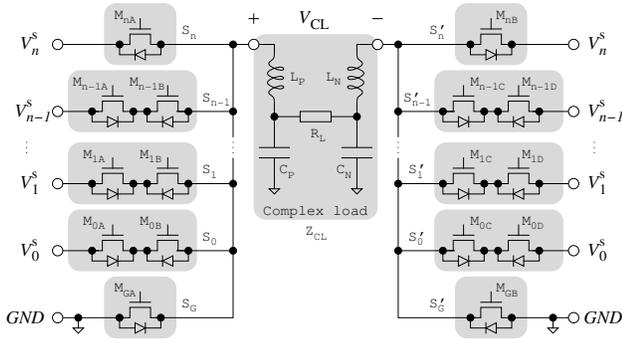


Figure 2. Multi-level full-bridge converter ($n + 2$ supply voltages). The complex load comprises a common-mode filter and the switches (S_i, S'_i) have been synthesised with power MOSFETs. If the R_L negative end is grounded, this converter simplifies to the multi-level buck topology.

Z_{CL} with two ends (Figure 2). This complex load may comprise a differential-mode filter, a common-mode filter (as in Figure 2), both of them or none (filter-less).

A. Multi-Level Buck Converter

In a multi-level buck converter, the complex load positive end is connected to all supply voltages through connection switches and the R_L negative end is grounded (as in Figure 2 but grounding the R_L negative end). In this way, the discrete amplitude signal can comprise up to as many distinct levels as distinct supply voltages.

When using n ($n \geq 0, n \in \mathbb{N}$) additional supply voltages besides GND and V_0^s ($n + 2$ supply voltages), the number of required connection switches and the maximum number of distinct output voltage levels is $n + 2$, given that each supply voltage of value V_i^s provides an output voltage level of value V_i^s . The output voltage is always positive if all the supply voltages are positive.

B. Multi-Level Full-Bridge Converter

In a full-bridge converter the R_L negative end is not grounded; instead it is symmetrically supplied with another buck converter (see Figure 2). The output voltage V_{CL} is therefore floating (differential-mode output) and thus a dedicated common-mode filter may be required in some applications. Yet, given a set of supply voltages and compared to the multi-level buck topology, this topology doubles the output voltage dynamic range.

The multi-level full-bridge converter uses one connection switch between each end of the complex load and each supply voltage¹. Therefore, a converter using $n + 2$ supply voltages requires $2 \cdot n + 4$ connection switches, see Figure 2.

Even if all supply voltages are positive², the complex load is supplied with a bipolar discrete-amplitude signal. The complex load ends are driven by a bipolar differential-mode voltage and by an unipolar common-mode voltage (positive if so are all supply voltages). Moreover, because of the differential output, the number of distinct output voltage levels not only depends upon the number and the value of the supply voltages, but also upon the switching policy, as described in the next section.

¹With only one power supply (i.e. two supply voltages, GND and V_0^s) the full-bridge converter is already multi-level capable, since three distinct output voltage levels are possible (of $\pm V_0^s$ and GND values).

²In a full-bridge converter, the polarity of the output voltage is continuously reversed, hence negative supply voltages yield the same output voltage levels as positive ones. In order to get distinct output voltage levels, their absolute value must be different $|V_i^s| \neq |V_j^s|$ if $i \neq j$. Still, negative supply voltages do modify the common-mode voltage at the complex load ends.

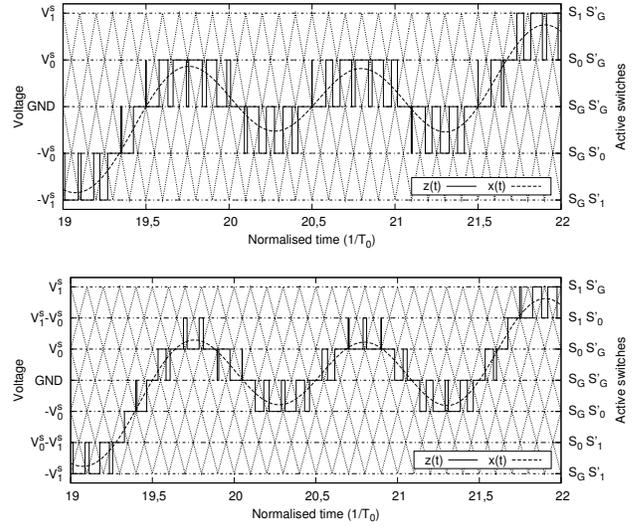


Figure 3. Significant time waveforms of multi-level PWM. Example with two power supplies employing a conventional policy (five levels, upper graph) and employing the proposed policy (seven levels, lower graph), conveniently selecting V_0^s for equally distributed output voltage levels in each case.

C. Output Voltage Levels and Switching Policy

Let us consider a system with a main power supply (which provides GND and V_0^s) and a power-management unit, which provides n additional different supply voltages ($n \geq 0, n \in \mathbb{N}$). There are $n + 2$ different available supply voltages in this system (Figure 2). In the multi-level full-bridge topology, because of the two subsets of switches, it is possible to apply any available supply voltage (GND, V_0^s, \dots, V_n^s) at each end of the complex load.

The conventional switching policies always set one end of Z_{CL} to GND (either the positive or the negative), so that the output voltage levels only comprise the values of the supply voltages (and the symmetrical negative values). The proposed policy sets both ends to any voltage, so that the output voltage levels also comprise the values of the voltage difference between supply voltages.

Let us consider a simple example, a system with three different supply voltages: V_0^s, V_1^s and GND . By setting the negative end of Z_{CL} to GND , the positive end can be supplied with GND, V_0^s or V_1^s , yielding three distinct output voltage levels of values GND, V_0^s and V_1^s . By reversing the polarity (i.e. setting the positive end of Z_{CL} to GND), two additional levels are generated, of values $-V_0^s$ and $-V_1^s$. Against this conventional policy, by employing the proposed policy it is possible to generate two additional levels. Setting the negative end of Z_{CL} to V_0^s and the positive to V_1^s (and vice versa) yields two levels of values $\pm(V_1^s - V_0^s)$; if $|V_1^s - V_0^s| \neq V_0^s$, the number of distinct output voltage levels is seven (instead of five with a conventional policy). Figure 3 summarises this example, employing a conventional policy and the proposed policy (conveniently selecting the supply voltages for equally distributed output voltage levels).

In general, in the full-bridge topology, the maximum number of distinct output voltage levels is

$$N_{\max} = 1 + \frac{(n+2)!}{n!} \quad (1)$$

Nevertheless, N_{\max} will only be achieved if the value of each supply voltage and the value of each voltage difference between

Additional supply voltages	$n = 0$	$n = 1$	$n = 2$
Conventional policy	3 (1,0)	5 (0,5 1,0)	7 (0,3 0,6 1,0)
Proposed policy	3 (1,0)	7 $\left\{ \begin{array}{l} (0,3 1,0) \\ (0,6 1,0) \end{array} \right.$	13 (0,16 0,6 1,0)

Table I

MAXIMUM NUMBER OF DISTINCT OUTPUT VOLTAGE LEVELS IN A MULTI-LEVEL FULL-BRIDGE CONVERTER USING DIFFERENT POLICIES; BETWEEN BRACKETS, THE SUPPLY VOLTAGES WHICH YIELD EQUALLY DISTRIBUTED OUTPUT VOLTAGE LEVELS (NORMALISED TO V_n^o).

any two of the supply voltages are distinct. If this condition is not satisfied, the number of effective output voltage levels becomes lower.

There are some values of the supply voltages which are particularly interesting, those which yield equally distributed output voltage levels, because they allow simpler modulation schemes. Table I compares the maximum number of distinct output voltage levels that can be generated using a conventional policy and the proposed policy, and the supply voltages that yield equally distributed output levels.

D. Switch Dimensioning for Equalised Conduction Losses and Synthesis with Power MOSFETs

When designing a multi-level converter, not all the switches handle the same current, so their ON resistance can be optimised. A possible design criterion for dimensioning the switches is their static (DC) power consumption (similar conduction losses in all switches).

Let us assume that the ON resistance R_{S_i} of the switches is always much lower than the complex load impedance at any frequency (let Z_L be the complex load minimum impedance)

$$R_{S_i, S'_i} \ll Z_L \leq |Z_{CL}(j\omega)| \quad \forall \omega \in \mathbb{R} \quad i = \{G, 0, 1, \dots, n\} \quad (2)$$

Using this approximation and assuming that the output voltage level V_a^o results in the highest current possible through the switch S_a , the power loss in this switch is

$$P_{S_a} = R_{S_a} \cdot I_{S_a}^2 = R_{S_a} \cdot \left(\frac{V_a^o}{Z_L} \right)^2 \quad (3)$$

Let V_h^o be the highest available output voltage level in the system, and let S_h be a switch generating this level. At this level, the switch S_h is going to handle the highest current (it must have the lowest ON resistance). Its power loss can be used as design reference; if so, the other switches (S_i and S'_i) may have higher ON resistance as the current through them is going to be lower. Therefore, in the example of the switch S_a , its ON resistance must fulfil

$$P_{S_a} \leq P_{S_h} \rightarrow R_{S_a} \leq R_{S_h} \cdot \left(\frac{V_h^o}{V_a^o} \right)^2 \quad (4)$$

Nonetheless, the switches $S_i, S'_i \quad i = \{0, \dots, n-1\}$ must handle bidirectional currents and withstand positive and negative voltages across them. When synthesising them with power MOSFETs, the built-in body diodes should never conduct, therefore each of these switches must be synthesised with two back-to-back power MOSFETs (Figure 2). The ON resistance of a switch must not depend on how it is synthesised, hence the ON resistance of each back-to-back power MOSFET must be half that of the switch that they implement.

Let us consider a simple example, a full-bridge converter whose supply voltages are $GND, 1V$, and $3V$; the switches are synthesised with power MOSFETs. The output voltage levels are: $\pm 3V, \pm 2V, \pm 1V$ and $0V$. Applying these values to the expression

(4), the ON resistance of the intermediate switches (S_0 and S'_0) can be 2,25 times higher than that of the others; nevertheless, because of the back-to-back synthesis, the ON resistance of each power MOSFET must be half of that value (1,13). Considering that the size of a power MOSFET is inversely proportional to its ON resistance, the area required by each switch (S_0 and S'_0) consisting of two back-to-back power MOSFETs is 1,78 times the area of a single power MOSFET switch (i.e. S_G, S'_G, S_1 or S'_1).

III. MULTI-LEVEL PULSE-WIDTH MODULATION

In general, the output voltage levels in multi-level switching converters are not necessarily equally distributed. Therefore, a suitable multi-level modulation to drive these converters must be able to handle non-regularly separated levels (native multi-level modulation).

A. Multi-Level Encoding Process

Pulse-Width Modulation (PWM) is the most common modulation in switching amplifiers (including multi-level using multiple carriers [1]). The encoding process is performed by comparing the reference signal with a carrier signal (generally a sawtooth or a triangle).

This modulation can be extended to native multi-level (N -PWM) by using carriers between each output voltage level (Figure 3). Within each carrier, the encoded signal is generated as in a regular PWM. In order to keep the properties of PWM, thus encoding at constant frequency, the adjacent carriers must be phase shifted 180° (Figure 3). Otherwise the reference signal could elude the corresponding carrier and skip some pulses.

B. Slew-Rate Limit

PWM has an intrinsic limit concerning the carrier frequency: the reference signal's slew-rate must be lower than that of the carrier [3], [4]. In the multi-level version, this intrinsic limit becomes more restrictive, since the carrier slew rate is reduced. Let N be the number of output voltage levels, c the modulation depth, A the amplitude of a sinusoid sweeping all the output dynamic range and A' the minimum distance between two consecutive levels. The limit for N -PWM is

$$\frac{f_{PWM}}{f_x} \geq \frac{\pi \cdot c}{2} \cdot (N-1) \geq \frac{\pi \cdot c}{2} \cdot \frac{A}{A'} \quad (5)$$

where f_{PWM} stands for the carrier frequency and f_x stands for the reference signal frequency. If the N levels are regularly separated (best case), the ratio A/A' simplifies to $N-1$. Notice that even in this case this condition is very restrictive, e.g. if using seven regularly separated levels and 100% of modulation depth, the ratio of the carrier frequency to the reference signal must be higher than 9,43.

If the previous condition is not satisfied, the reference signal may be faster than the carrier, hence the encoded signal may not be a pure PWM signal thus containing extra pulses. From another standpoint, given a certain reference signal and a desired switching frequency, it may be necessary to switch between non-adjacent levels to properly track the reference signal. However, N -PWM needs switching between adjacent levels.

IV. PERFORMANCE OF MULTI-LEVEL AMPLIFIERS

Four multi-level full-bridge amplifiers have been compared (see Figure 4 and Table II). Each amplifier uses a specific number of output voltage levels, yet equally distributed in all cases, including: two supply voltages (three levels), three supply voltages and a conventional policy (five levels), three supply voltages and the proposed policy (seven levels) and four supply voltages and the proposed policy (thirteen levels). The reference signal used in this characterisation is

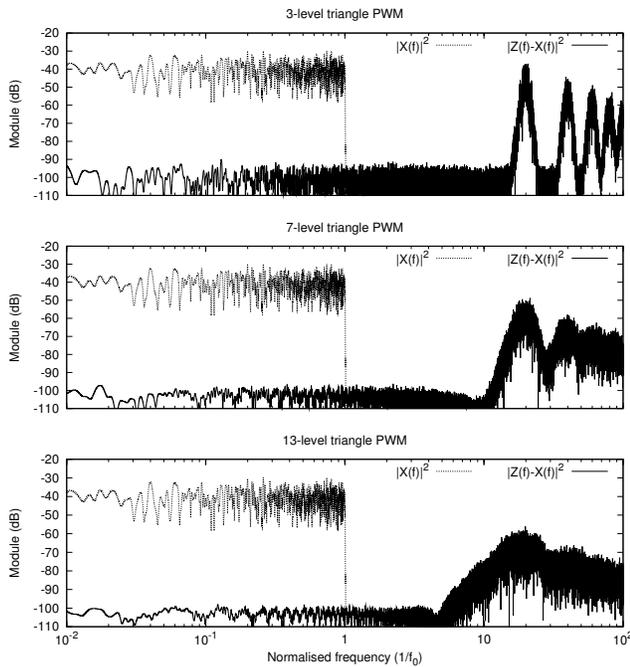


Figure 4. Encoded error spectrum of multi-level PWM, using different numbers of levels (all equally distributed). Behavioural-model simulation.

a band-limited flat-spectrum signal which sweeps all the available dynamic range without clipping.

The main advantage of multi-level amplification is the out-of-band³ power reduction in the encoded signal (Figure 4). In this way, less filtering effort is required to achieve the same performance. These simulations are quantitatively summarised in Table II, which shows the power distribution. The out-of-band power is reduced by 6 dB in the 5-level case, by 9 dB in the 7-level case and by 15 dB in the 13-level case.

If the output voltage levels are not equally distributed, the amplifier will behave as a multi-level amplifier with fewer levels; e.g. if $V_0^s = 1,0\text{ V}$ and $V_1^s = 2,1\text{ V}$, the output voltage levels will be $\pm 2,1\text{ V}$, $\pm 1,1\text{ V}$, $\pm 1,0\text{ V}$ and 0 V , hence the advantage of using the additional $\pm 1,1\text{ V}$ levels may not yield a performance improvement (the amplifier performance will be similar to a 5-level one).

A. Filter-Less Amplifiers

In certain applications, such as audio, high-frequency distortion is tolerable, thus filter-less operation is possible. The main drawback of filter-less amplifiers –apart from EMI– is efficiency, since all the out-of-band power can be considered as losses. Besides, all this high-frequency power is directly supplied to the load, which may compromise its reliability.

In a conventional full-bridge amplifier (three levels), the out-of-band power is 50%; in a conventional 5-level amplifier (three supply voltages) it is 21% (table II). These values, which would be losses in a filter-less amplifier, are too high for a switching amplifier. However, if using a 7-level amplifier (yet three supply voltages but employing the proposed switching policy), the out-of-band power is only 11%.

Notice that a boost converter is often required to achieve the desired output power (e.g. audio in mobile applications), thus three supply

³Out-of-band stands for high-frequency components, the spectral content at frequencies beyond the reference signal bandwidth.

Modulation	Power distribution (in-band + out-of-band)	High-frequency normalised power
3-PWM	50 % + 50 %	100 % (0 dB)
5-PWM*	79 % + 21 %	27 % (−5,7 dB)
7-PWM*	89 % + 11 %	12 % (−9,2 dB)
13-PWM	97 % + 3 %	3 % (−15,2 dB)

Table II
POWER DISTRIBUTION IN N -PWM SWITCHING AMPLIFIERS (IN-BAND STANDS FOR POWER WITHIN THE REFERENCE SIGNAL BANDWIDTH).

*THESE ARE THE EXAMPLES IN FIGURE 3.

voltages (including GND) are already present in the system; the 7-level converter takes full advantage of the three of them.

By using another additional supply voltage (thirteen levels), the out-of-band power is only 3%. However, generating the additional supply voltage (if it is not already present) involves more losses, which must also be taken into account.

V. CONCLUSIONS

This work has proposed a switching policy for multi-level full-bridge switching power converters, that maximises the number of output voltage levels for a given number of supply voltages and connection switches. This is achieved by also using the voltage difference between supply voltages. This work has also analysed a multi-level modulation (N -PWM) to drive these converters, targeting high-efficiency power amplifiers.

Both the converters and the modulation presented in this work are able to handle arbitrarily separated levels, thus allowing to take advantage of any available supply voltage present in a certain system.

Simulation results show that when tracking a band-limited signal, the out-of-band power can be significantly reduced by using the proposed policy; e.g. upgrading an amplifier from five levels to seven levels (neither additional supply voltages nor additional switches are required) yields an out-of-band power reduction from 21% to 11%.

If some out-of-band distortion is tolerable, filter-less amplification becomes feasible, since the out-of-band power (i.e. losses) is significantly reduced. Employing the proposed policy and four supply voltages (yielding thirteen levels), the out-of-band power is only 3%.

ACKNOWLEDGMENTS

Partial funding by project TEC2007-67988-C02-01 from the Spanish MCYT and EU FEDER funds. This work has been partially supported by the grant RUE CSD2009-00046, Consolider-Ingenio 2010 Programme, Spanish Ministry of Science and Innovation. With the support of the Commissioner for Universities and Research of the Department of Innovation, Universities and Companies of the Catalan Government and the European Social Fund.

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