

CMOS RF First-Order All-Pass Filter

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Abstract—In this paper, a wide-band first-order voltage-mode all-pass filter is presented. Due to a simple structure and appropriate performance of the proposed all-pass filter, this filter achieves a flat group delay of over 60 ps with a pole/zero pair located at 4.5 GHz. The proposed circuit demonstrates a high linearity and consumes merely 16 mW power from a 1.8-V supply. Simulation results indicate an input-referred 1-dB compression point P_{1dB} of 4.1 dBm and the wide-band operation capability of the first-order all-pass filter. Furthermore, the proposed all-pass filter is capable of converting into a second-order all-pass filter adding only a grounded capacitor. To demonstrate the performance of the proposed all-pass filter, simulation results are conducted by using Virtuoso Cadence in a TSMC 180-nm CMOS process.

Index Terms—All-pass filter, delay, CMOS, wide-band, linearity.

I. INTRODUCTION

All-pass filters or phase shifters have a variety of applications in signal processing and communication systems. In these circuits, the amplitude of the input signal is constant over the desired frequency band, while creating a frequency dependent delay. There are both current-mode and voltage-mode all-pass filters based on, e.g., the second generation current conveyors (CCII) [1]–[3], differential voltage current conveyors (DVCCs) [4]–[6], digitally programmable DVCCs (DPDVCCs) [7], differential difference current conveyors (DDCCs) [8], [9], current controlled current conveyors (CCCII) [10]–[12], operational transresistance amplifiers (OTRAs) [13]–[15], and dual-X current conveyor transconductance amplifier (DXCCTA) [16], as active elements in the literature. A number of these all-pass filters, however, suffer from excessive number of active and/or passive elements [1]–[3], [5], [7], [9]–[15], the use of floating capacitors which is not desirable for IC implementation [17]. Furthermore, most of these circuits operate up to multi-KHz frequency [1]–[3], [5]–[8], [12]–[15], [17] and the others around multi-GHz frequency [4], [9]–[11], [16].

On the other hand, there are some voltage-mode all-pass filters reported over the last two decades, which operate in radio frequencies (RFs) and have different applications [18]–[22]. In some applications, e.g. beam-forming, delay stages as delay cells are normally realized by cascading first-order all-pass filters in order to reach a desired delay [22]. However, there are just few RF first-order voltage-mode all-pass filters in the literature [22], [23], since it is hard to design an all-pass filter which has a flat group delay over a wide frequency range.

A broadband RF first-order voltage-mode all-pass filter is introduced in this work. The proposed all-pass filter is comprised of one transistor, three resistors, and one grounded inductor.

This circuit demonstrates a high linearity and a large delay in a single delay cell through a wide frequency band. In addition, the proposed filter is considerably flexible, since it can achieve a higher order by adding just one grounded capacitor.

The structure of this paper is as follows. Section II describes the structure of proposed all-pass filter and provides theoretical analyses. In Section III, simulation results are presented. An increase in the order of the all-pass filter is provided in Section IV. Ultimately, conclusions are drawn in Section V.

II. PROPOSED FIRST-ORDER ALL-PASS FILTER

Fig. 1 shows the proposed first-order all-pass filter. In this filter, M_1 is a common-source configuration to convert the input voltage signal into current. At the output node, the drain current of M_1 and the current of feedback resistor R_1 are subtracted to realize an all-pass function. Then, the current will be converted to voltage by the load resistor, R_L . Resistor R_2 is realized by the diode-connected transistor of M_2 , which is self-biased.

An all-pass filter can be accurately approximated to a first-order all-pass filter, which its ideal transfer function is expressed by

$$H(s) = e^{-s\tau} = \frac{1 - s(\tau/2)}{1 + s(\tau/2)} \quad (1)$$

where τ is time delay. If we assume that $g_{m1,2} \gg g_{ds}$ and neglect the parasitics of the transistors, the transfer function of the proposed first-order voltage-mode all-pass filter in Fig. 1 is given by

$$\frac{V_{out}}{V_{in}}(s) = -\frac{R_L(g_{m1}R_1 - 1)}{R_L + R_1} \cdot \frac{1 - sL\left(\frac{g_{m1} + g_{m2} - g_{m1}g_{m2}R_1}{g_{m1}R_1 - 1}\right)}{1 + sL(g_{m1} + g_{m2})} \quad (2)$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2 , respectively. The nominator and denominator in (2) have to be the same to realize an all-pass structure. Therefore, if we satisfy the following conditions:

$$g_{m1}R_1 = 2 \quad (3a)$$

$$R_L \gg R_1 \quad (3b)$$

$$g_{m1} + g_{m2} \gg g_{m1}g_{m2}R_1 \quad (3c)$$

then, the transfer function can be rewritten as

$$\frac{V_{out}}{V_{in}}(s) \simeq -\frac{1 - sL(g_{m1} + g_{m2})}{1 + sL(g_{m1} + g_{m2})} \quad (4)$$

The voltage gain of the filter is -1 at low frequencies, as the inductor L shorts the source terminal of M_1 to ground. At high frequencies, the inductor L can be regarded as an open-circuit and, therefore, we have a voltage gain equal to -1 again. The

pole/zero frequencies, phase, and group delay responses of the first-order all-pass filter are given, respectively, by

$$\omega_p = -\omega_z = -\frac{1}{L(g_{m1} + g_{m2})} \quad (5)$$

$$\varphi(\omega) = -2 \tan^{-1} [\omega L(g_{m1} + g_{m2})] \quad (6)$$

and

$$\tau_g(\omega) = -\frac{\partial \varphi(\omega)}{\partial \omega} = 2L(g_{m1} + g_{m2}) \cdot \frac{1}{1 + [\omega L(g_{m1} + g_{m2})]^2} \quad (7)$$

where ω is the angular frequency. From (7), it should be noted that the group delay is equal to $2Lg_{m1}$ at low frequencies and g_{m2} (i.e., $R_2 = 1/g_{m2}$) will be ignored, since the L shorts the source of M_1 to ground at DC.

At high frequencies, the resistor R_2 in Fig. 1 will be just seen at the source of M_1 and considered as a source degeneration resistor, contributing to the linearity of the circuit.

Note that, we can not ignore the effects of parasitic capacitors C_{gs} and C_{gd} on the all-pass filter in Fig. 1. Therefore, we need to find the closest parasitic pole to the dominant poles/zeros. The parasitic pole stemmed from the C_{gd} is approximately equal to $1/R_1 C_{gd}$. From (3), the value of resistor R_1 has to be small. Hence, this parasitic pole will be far beyond the dominant poles/zeros. Further analysis indicates that the nearest parasitic pole to the dominant poles/zeros is stemmed from the C_{gs} . Considering the C_{gs} , which affect the pole/zero frequencies and DC-gain, and assuming $g_{m1,2} \gg g_{ds}$, the transfer function of the first-order all-pass filter can be determined by

$$\frac{V_{out}}{V_{in}}(s) = -\frac{R_L}{R_L + R_1} \cdot \frac{[(g_{m1}R_1 - 1) - sL(g_{m1} + g_{m2} - g_{m1}g_{m2}R_1) - s^2LC_{gs}]}{[1 + sL(g_{m1} + g_{m2}) + s^2LC_{gs}]} \quad (8)$$

Consequently, it can be observed that the additional parasitic pole is located at

$$\omega_{p2} \cong \frac{L(g_{m1} + g_{m2}) + \sqrt{L^2(g_{m1} + g_{m2})^2 - 4LC_{gs}}}{2LC_{gs}} \quad (9)$$

III. SIMULATION RESULTS

The proposed first-order all-pass filter is simulated in a 180-nm TSMC CMOS process and results are obtained using Virtuoso Cadence. The proposed circuit in Fig. 1 is expected to achieve pole/zero frequencies located at 4.5GHz and simulated with $g_{m1} = 31.5\text{mA/V}$, $g_{m2} = 7.4\text{mA/V}$, $R_L = 3\text{K}\Omega$, $R_1 = 65\Omega$, and $L = 0.85\text{nH}$. The power consumption is 16mW from a supply voltage of 1.8-V.

Fig. 2 indicates the gain and phase responses of the first-order all-pass filter. The gain of the proposed filter is about -1dB , due to the fact that the DC gain of the all-pass filter is less than unity (refer to (2)), and also due to the parasitic effects of the transistors. The group delay response of the proposed all-pass filter is shown in Fig. 3, proving a flat group delay of

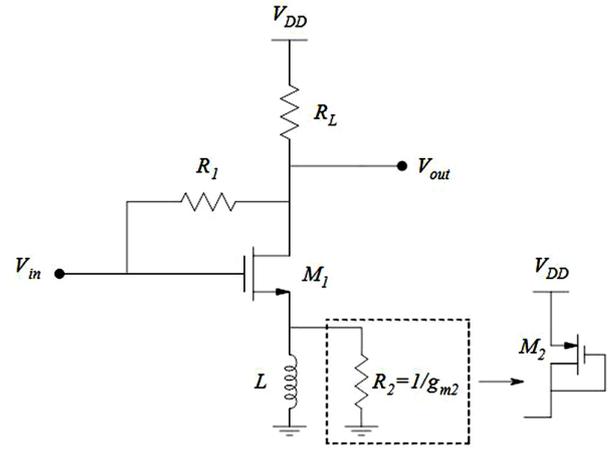


Fig. 1. The proposed first-order voltage-mode all-pass filter.

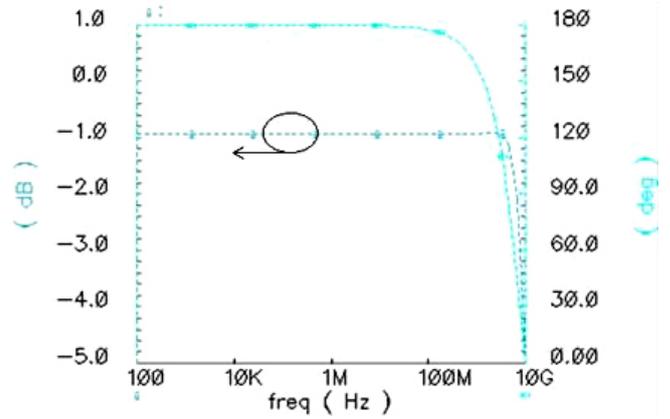


Fig. 2. Gain and phase responses of the proposed first-order all-pass filter.

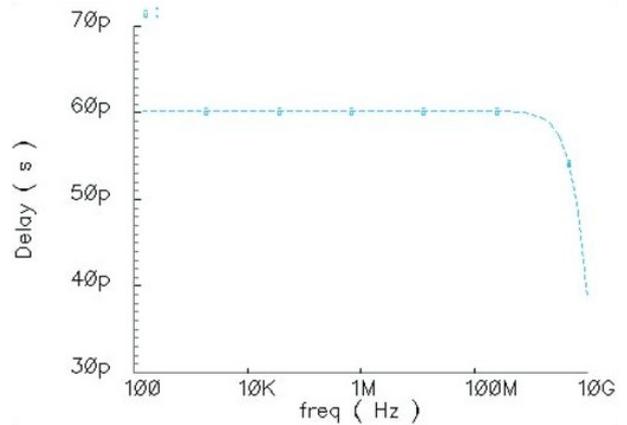


Fig. 3. Group delay response of the proposed first-order all-pass filter.

over 60ps within a bandwidth of about 4.5GHz. This simulated group delay value is close to the theoretical one in (7), with an error of around 12%.

The gain and group delay responses of the first-order all-pass filter for different values of g_{m2} , ($R_2 = 1/g_{m2}$), are shown in Figs. 4 and 5, respectively. It is noticeable that

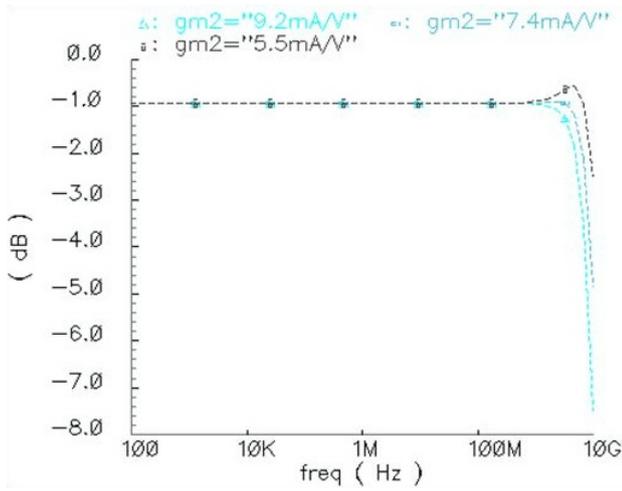


Fig. 4. Gain response of the proposed first-order all-pass filter under different values of g_{m2} , ($R_2 = 1/g_{m2}$).

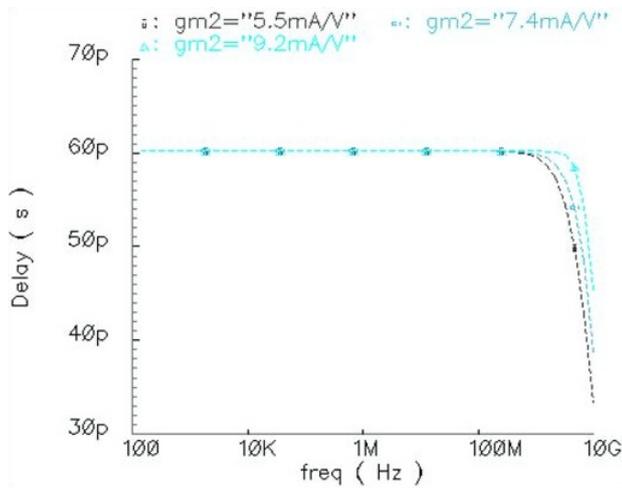


Fig. 5. Group delay response of the proposed first-order all-pass filter under different values of g_{m2} , ($R_2 = 1/g_{m2}$).

flat gain and group delay responses are achieved at high frequencies by varying g_{m2} . Moreover, it can be observed that g_{m2} is proportional to the group delay (refer to (7)), since by increasing g_{m2} , the group delay of the proposed filter is increased as well at high frequencies.

In Fig. 6, the input-referred noise response of the first-order all-pass filter is shown. The input-referred noise value is approximately $1.25\text{nV}/\sqrt{\text{Hz}}$ throughout the frequency band. The input-referred 1-dB compression point (P_{1dB}) and input-referred third-order intercept point (IIP3) responses of the first-order all-pass filter are shown in Fig. 7. The input-referred P_{1dB} and IIP3 are 4.1dBm and 17.8dBm at 2.5GHz, respectively. This high linearity of the proposed circuit is due to the high drain current of M_2 at the price of higher power consumption.

IV. INCREASING THE ORDER OF THE ALL-PASS FILTER

The proposed First-order all-pass filter in Fig. 1 can be converted into a second-order all-pass filter by adding just a

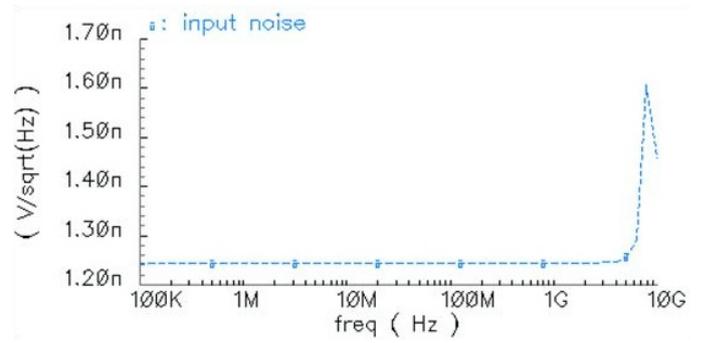


Fig. 6. Input-referred noise response of the proposed first-order all-pass filter.

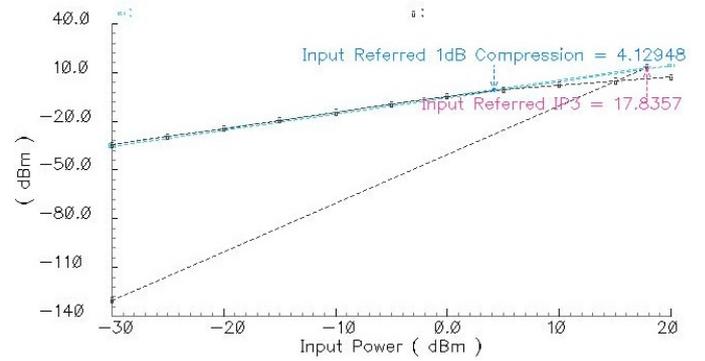


Fig. 7. Input-referred P_{1dB} and input-referred IIP3 responses of the proposed first-order all-pass filter.

capacitor in parallel with the inductor L and resistor R_2 at the source of M_1 . Fig. 8 shows the second-order voltage-mode all-pass filter.

The ideal transfer function of a second-order all-pass filter is approximately expressed by

$$H(s) = \frac{s^2 - \frac{\omega_n}{Q}s + \omega_n^2}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \quad (10)$$

where ω_n is the natural frequency of the all-pass filter and Q is the quality factor, which determine the position of poles and zeros in the complex plane. If the parasitics of the transistors are neglected and $g_{m1,2} \gg g_{ds}$, the transfer function of the second-order all-pass filter is defined as

$$\frac{V_{out}(s)}{V_{in}(s)} = -\frac{R_L(g_{m1}R_1-1)}{R_L+R_1} \cdot \frac{s^2 - \frac{1}{C} \left(\frac{g_{m1}+g_{m2}-g_{m1}g_{m2}R_1}{g_{m1}R_1-1} \right) s + \frac{1}{LC}}{s^2 + \frac{1}{C}(g_{m1}+g_{m2})s + \frac{1}{LC}} \quad (11)$$

where g_{m1} and g_{m2} are the transconductances of M_1 and M_2 , respectively. An all-pass realization will be achieved for this circuit if the conditions in (3) are satisfied. Therefore, the transfer function can be rewritten as

$$\frac{V_{out}(s)}{V_{in}(s)} \cong -\frac{s^2 - \frac{1}{C}(g_{m1}+g_{m2})s + \frac{1}{LC}}{s^2 + \frac{1}{C}(g_{m1}+g_{m2})s + \frac{1}{LC}}. \quad (12)$$

Thus, the natural frequency and the quality factor of the

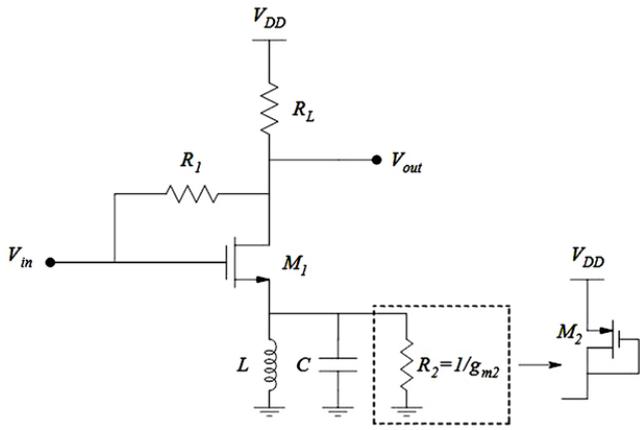


Fig. 8. The second-order voltage-mode all-pass filter achieved by adding a grounded capacitor to the circuit in Fig. 1.

second-order all-pass filter are determined, respectively, by

$$\omega_n = \frac{1}{\sqrt{LC}} \quad (13)$$

$$Q = \frac{1}{g_{m1} + g_{m2}} \sqrt{\frac{C}{L}} \quad (14)$$

The pole/zero frequencies, phase, and group delay responses of the second-order all-pass filter are expressed, respectively, by

$$|\omega_{p1,2}| = |\omega_{z1,2}| = \frac{L(g_{m1} + g_{m2}) \pm \sqrt{L^2(g_{m1} + g_{m2})^2 - 4LC}}{2LC} \quad (15)$$

$$\varphi(\omega) = -2 \tan^{-1} \left[L(g_{m1} + g_{m2}) \cdot \frac{\omega}{1 - LC\omega^2} \right] \quad (16)$$

and

$$\tau_g(\omega) = -\frac{\partial \varphi(\omega)}{\partial \omega} = 2L(g_{m1} + g_{m2}) \cdot \frac{1 + LC\omega^2}{(1 - LC\omega^2)^2 + ((g_{m1} + g_{m2})L\omega)^2} \quad (17)$$

Similar to the first-order all-pass filter, the group delay of the second-order all-pass filter is $2Lg_{m1}$ at low frequencies.

V. CONCLUSION

This paper presents a wide-band first-order voltage-mode all-pass filter. The proposed first-order all-pass filter achieves a flat group delay of approximately 60ps with pole/zero frequencies located at 4.5GHz, while consuming only 16mW power. This all-pass filter is highly linear, and has the input-referred 1-dB compression point P_{1dB} of around 4dBm and the input-referred intercept point IIP3 of 17.8dBm at 2.5GHz. The proposed circuit can reach a higher order, which demonstrates a considerable flexibility.

REFERENCES

- [1] K. Pal and S. Rana, "Some new first-order all-pass realizations using CCII," *Active and Passive Elec. Compon.*, vol. 27, no. 2, pp. 91-94, Jun. 2004.
- [2] J. W. Horng, "Current conveyors based allpass filters and quadrature oscillators employing grounded capacitors and resistors," *Comp. Elec. Eng.*, vol. 31, no. 1, pp. 81-92, Jan. 2005.
- [3] M. A. Ibrahim, H. Kuntman, S. Ozcan, O. Suvak, and O. Cicekoglu, "New first-order inverting-type second-generation current conveyor-based all-pass sections including canonical forms," *Elec. Eng.*, vol. 86, no. 5, pp. 299-301, Sept. 2004.
- [4] S. Maheshwari and D. Agrawal, "High performance voltage-mode tunable all-pass section," *J. Circuit Syst. Comp.*, vol. 24, no. 6, Jul. 2015.
- [5] S. Minaei and M. A. Ibrahim, "General configuration for realizing current-mode first-order all-pass filter using DVCC," *Int. J. Electron.*, vol. 92, no. 6, pp. 347-356, Jun. 2005.
- [6] S. Maheshwari, "High output impedance current-mode all-pass sections with two grounded passive components," *IET Circuits Devices Syst.*, vol. 2, no. 2, pp. 234-242, Apr. 2008.
- [7] I. A. Khan, M. I. Masud, and S. A. Moiz, "Reconfigurable fully differential first order all pass filter using digitally controlled CMOS DVCC," in *IEEE Proc. 8th Conf. and Exhibition, Muscat*, 2015, pp. 1-4.
- [8] R. Das and S. K. Paul, "Voltage mode first order all pass filter design using differential difference current conveyor," in *2016 Int. Conf. Microelectronics, Computing and Communications (MicroCom)*, pp. 1-4.
- [9] J. Mohan, S. Maheshwari, D. S. Chauhan, and G. Garg, "Two DDCC based cascadable voltage-mode first-order all-pass filter," in *2012 Proc. Int. Conf. Advances in Electron., Elec. and Comp. Science Eng.*, pp. 290-294.
- [10] P. Singthong, M. Siripruchyanun, and W. Jaikla, "Electronically controllable first-order current-mode allpass filter using CCCIs and its application," in *2011 Proc. 18th Int. Conf. Mixed Design of Integrated Circuits Syst. (MIXDES)*, pp. 314-318.
- [11] S. N. Songkla and W. Jaikla, "Realization of electronically tunable current-mode first-order allpass filter and its application," *Int. J. Electron. and Elec. Eng.*, vol. 6, no. 1, pp. 40-43, Jan. 2012.
- [12] S. Minaei and O. Cicekoglu, "A resistorless realization of the first-order all-pass filter," *Int. J. Electron.*, vol. 93, no. 3, pp. 177-183, Aug. 2006.
- [13] S. Kilinc and U. Cam, "Realization of allpass filters using operational transresistance amplifier (OTRA)," in *2004 IEEE Proc. 12th Conf. Signal Processing and Communications Applications*, pp. 133-136.
- [14] S. Kilinc and U. Cam, "Operational transresistance amplifier based first-order allpass filter with an application example," in *IEEE Proc. Int. Midwest Symp. Circuits Syst. (MWSCAS'04)*, Nov. 2004, pp. 65-68.
- [15] C. Cakir, U. Cam, and O. Cicekoglu, "Novel allpass filter configuration employing single OTRA," *IEEE Trans. Circuits Syst. II*, vol. 52, no. 3, pp. 122-125, Mar. 2005.
- [16] A. Kumar and B. Chaturvedi, "Cascadable first-order current-mode all-pass filter with electronic tuning," in *2016 Int. Conf. Signal Processing and Communication*, pp. 229-232.
- [17] S. Maheshwari and I. A. Khan, "Novel first-order current-mode allpass sections using CCIII," *Active and Passive Elec. Compon.*, vol. 27, no. 2, pp. 111-117, Jun. 2004.
- [18] J. Buckwalter and A. Hajimiri, "An active analog delay and the delay reference loop," in *Proc. IEEE RFIC Symp. (RFIC04), Dig.*, Jun. 2004, pp. 17-20.
- [19] C. Wijenayake, Y. Xu, A. Madanayake, L. Belostotski, and L. Bruton, "RF analog beamforming fan filters using CMOS all-pass time delay approximations," *IEEE Trans. Circuits Syst. I*, vol. 59, no. 5, pp. 1061-1073, May 2012.
- [20] P. Ahmadi, B. Maundy, A. S. Elwakil, L. Belostotski, and A. Madanayake, "A new 2nd-order all-pass filter in 130-nm CMOS," *IEEE Trans. Circuits Syst. II: Express Briefs*, vol. 63, no. 3, pp. 249-253, Mar. 2016.
- [21] A. Ulusoy, B. Schleicher, and H. Schumacher, "A tunable differential all-pass filter for uwb true time delay and phase shift applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 9, pp. 462-464, Sept. 2011.
- [22] S. K. Garakoui, E. A. M. Klumperink, B. Nauta, and F. E. van Vliet, "Compact cascadable gm-C all-pass true time delay cell with reduced delay variation over frequency," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 693-703, Mar. 2015.
- [23] P. Ahmadi, M. H. Taghavi, L. Belostotski, and A. Madanayake, "6-GHz All-Pass-Filter-Based Delay-And-Sum Beamformer in 130nm CMOS," in

Proc. IEEE Int. Midwest Symp. Circuits Syst. (MWSCAS), Sept. 2014, pp. 837-840.