IMTC 2003 – Instrumentation and Measurement
Technology Conference
Vail, CO, USA, 20-22 May 2003

A High-Speed Capacitive-Sensor Interface Using a Relaxation Oscillator and a Fast Counter

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Abstract *– This paper presents the analysis and experimental results on the jitter of a capacitive-sensor interface. The interface is implemented with a simple relaxation oscillator, a fast counter and a microcontroller. The goal is to find the criteria to implement a low-noise system, so that, even with a short measuring time, a high-resolution can be obtained. Experimental results are performed in order to prove the validity of the theoretical predictions. The quantization noise of the 50 MHz counter predominates over the internal noise of the oscillator for measuring times shorter than 2 ms. The achieved resolution for measuring times of 2 ms and 20 ms is better than 16 bits and 18 bits, respectively.*

I. INTRODUCTION

Capacitive sensors are used in a wide variety of measurement and control systems, such as liquid-level gauges, pressure meters, accelerometers and precision positioners. In these applications, the capacitances to be measured are often in the range of 0.1 pF to 10 pF, while a high resolution is required.

Electronic interfaces whose output signals are period modulated are very attractive because they can directly be interfaced to a microcontroller. Such interfaces can easily be implemented with a simple relaxation oscillator [1] and applied to capacitive sensors [2]. Due to their simplicity these interfaces can provide a good-noise performance. Reference [2] reports a resolution of better than 10^{-4} with a measurement time of 100 ms. However, some applications require a high-resolution measurement with a shorter measurement time.

To achieve a fast and accurate measurement, the noise of the electronic interface should be as small as possible. This requires the use of a low-noise relaxation oscillator and a fast counter to measure the period of the signal. Most of commercial low-cost microcontrollers can be driven with a clock frequency up to 20 MHz, but its internal counters normally work at a lower frequency. An improvement can be made using an additional counter working at a higher frequency. This will reduce the quantization noise, caused by measuring and digitizing the period-modulated output signal. On the other hand, the noise of the oscillator itself should be minimized. To enable the design of a low-noise oscillator, in this paper the contributions of the different noise sources in the relaxation oscillator have been analyzed. In a previous work a similar analysis has been made for an oscillator implemented as an integrated circuit [3]. In this paper we also consider the application of commercially available chips (Op-Amps and Comparators). Due to the high performance of these chips and the application of a fast counter the applied approximation differs from those for the integrated versions.

Moreover, the flexibility in replacing the applied components by other ones with different performance, allows us to perform a wide range of experiments to verify the theoretical analysis. The designed circuit has been applied to a contactless capacitive angular-position sensor [5] and to control an active magnetic bearing actuator.

II. CAPACITIVE INTERFACE

A. Relaxation oscillator

Figure 1 shows the schematic circuit of the first-order relaxation oscillator [1, 2], which is the core of the capacitive interface.

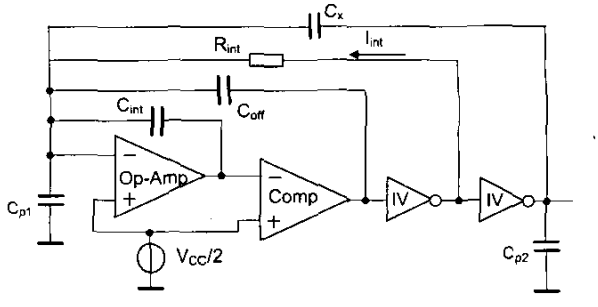

Figure 1. First-order relaxation oscillator

The oscillator is implemented with an operational amplifier (Op-Amp), a comparator (Comp), two inverters, the capacitances C_{off}, C_{int}, and a controlled current source I_{int}, which value depends on the resistor R_{int}. The performance of the oscillator is described elsewhere [3, 4]. The capacitor C_x represents the capacitance of the sensor to be measured and C_{p1} and C_{p2} model the parasitic capacitances to ground due to, for example, the connected cables. The period of the oscillator output signal is given by

$$T_x = 4R_{int}(C_{off} + C_x) \quad (1)$$

The additive and multiplicative errors can be eliminated using the three-signal approach [4].

Some parameters are fixed: the sensor itself determines C_x, and C_{off} is normally chosen to be around the maximum value of C_x; the value of C_{int} must be at least $2(C_{off} + C_x)$ in order to avoid saturating the Op-Amp output (considering a rail-to-rail output Op-Amp); the supply voltage is determined by the application itself. So, the period, T_x, of the output signal can be controlled by the value of R_{int}, i.e., the value of the integration current, I_{int}.

B. The complete interface

The capacitive-sensor interface is mainly composed of a relaxation oscillator, a multiplexer, an external counter and a microcontroller (Figure 2). The relaxation oscillator converts the capacitance values of the sensing element to a period-modulated output. The counter measures the elapsed time of N periods. The multiplexer selects the measured capacitance. The microcontroller controls the external counter and multiplexer, reads the data and transmits them via a RS232 interface to a PC.

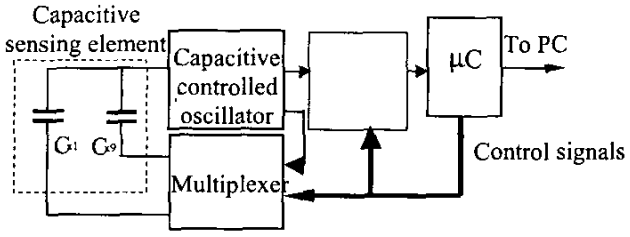

Figure 2. Functional block diagram of the capacitive-sensor interface

To measure the period of the square-wave signal at the oscillator output a Constant Pulse Counting (CPC) method [6] is used. In the CPC method we count the elapsed time, T_e, for N periods of the output signal of the relaxation oscillator. So,

$$T_e = NT_x . \tag{2}$$

The external counter measures this elapsed time by counting clock pulses with a counting frequency of 50 MHz (20 ns). The measured times for the capacitances C_{off} and the external capacitances C_{x1} to C_{x9} are sent, optionally, to the PC.

III. NOISE ANALYSIS

The noise performance of the oscillator is investigated using the circuit schematic of Figure 3 in which $C_m = C_{off} + C_x$ and the main noise sources have been indicated.

The considered noise sources are:

- the input noise voltage v_{ni} of the Op-Amp
- the input noise current i_n of the Op-Amp
- the input noise voltage v_{nc} of the comparator

The noise due to the resistor is neglectable compared to the other noise sources and the input noise current of the comparator has no influence, so they have not been included into the model. We calculate the influence of the different noise sources on the oscillator performance. White noise can be described as the sum of an infinite number of sinusoidal components having equal amplitudes, differing frequencies and a random phase. The influence of the noise in the circuit can be calculated by evaluating the influence of only one noise component. The effect of the complete noise spectrum can be found by way of superposition. For the analysis we suppose white noise and that the noise sources are uncorrelated with the output of the comparator.

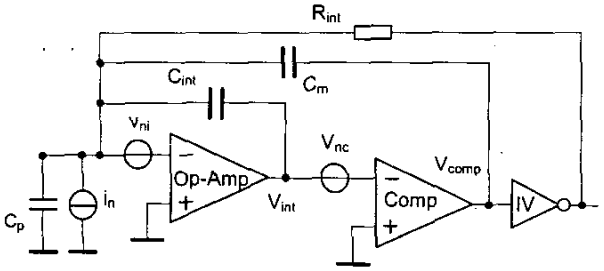

Figure 3. The relaxation oscillator with the main noise sources.

A. Noise voltage analysis

Firstly, the effect of v_{ni} and v_{nc} is analyzed. The relative variation on the period of the output signal is defined as

$$\varsigma = \frac{\Delta T_x}{T_x} . \tag{3}$$

According to the analysis described in [7], the model shown in Figure 4 is used to relate, in the frequency domain, the overall noise voltage v_n at the input of the comparator, due to the contribution of both v_{ni} and v_{nc}, with ζ,

Figure 4. Frequency model that relates the noise voltage at the input of the comparator with the relative variation of the period.

where

$$H_v(jf) = \frac{2C_{int}}{V_{DD}(C_{off} + C_x)} sin^2\left(\frac{\pi f}{2f_x}\right), \tag{4}$$

and $f_x = 1/T_x$. This transfer function is zero at $f = 0$ and at the even multiples of f_x. We define the jitter of the oscillator as the standard deviation of the normalized one-period time error

$$\sigma_\varsigma = \frac{\sigma_{\Delta T_x}}{T_x} . \tag{5}$$

The jitter due to the overall noise voltage at the input of the comparator is given by

$$\sigma_\varsigma(v_n)=\sqrt{\int_0^{B_{eq}}\left|H(jf)\right|^2 S_v(f)df}\ , \tag{6}$$

where B_{eq} is the equivalent bandwidth of the system and $S_v(f)$ is the power spectral density (PSD) of the noise voltage at the input of the comparator. Considering $B_{eq}>>f_x$, condition that has to be satisfied to assure a low nonlinearity [3, 4], and white noise, equation (6) can be approximated as

$$\sigma_\varsigma(v_n)=\frac{C_{int}}{V_{DD}(C_{off}+C_x)}\sqrt{\frac{3}{2}S_v B_{eq}} \tag{7}$$

The contribution of the $1/f$ noise is neglectable if the corner frequency of S_v is much lower than f_x.

Using (7) for the contribution of the voltage noise source v_{nc} to the jitter, we found that

$$\sigma_\varsigma(v_{nc})=\frac{C_{int}}{V_{DD}(C_{off}+C_x)}\sqrt{\frac{3}{2}S_{vc}B_{comp}}\ , \tag{8}$$

where S_{vc} is the PSD of v_{nc} and B_{comp} is the unity-gain bandwidth of the comparator.

For the noise voltage v_{ni}, its equivalent PSD at the input of the comparator is given by

$$S_v=S_{vi}\left(\frac{C}{C_{int}}\right)^2, \tag{9}$$

where S_{vi} is the PSD of v_{ni} and $C = C_{off} + C_x + C_{int} + C_p$. Defining B_{amp} as

$$B_{amp}=f_T\frac{C_{int}}{C}, \tag{10}$$

where f_T is the unity-gain bandwidth of the Op-Amp, and using (7) for the contribution of v_{ni} to the jitter, we found that

$$\sigma_\varsigma(v_{ni})=\frac{C}{V_{DD}(C_{off}+C_x)}\sqrt{\frac{3}{2}S_{vi}B_{eq}}\ , \tag{11}$$

where B_{eq} is now the lowest value of B_{comp} and B_{amp}. When $B_{amp} < B_{comp}$ the jitter can be expressed as

$$\sigma_\varsigma(v_{ni})=\frac{1}{V_{DD}(C_{off}+C_x)}\sqrt{\frac{3}{2}S_{vi}f_T C_{int}C}\ . \tag{12}$$

Keeping the parasitic capacitance C_p, and then C, at a minimum reduces the jitter. On the other hand, if $C_p >> C_{int}$, the jitter will increase with the square root of C_p.

B. Noise current analysis

Following the analysis described in [7] and particularizing for the circuit of Fig. 3, the transfer function that relates i_n with ζ is given by

$$H_i(jf)=\frac{\sin^2\left(\frac{\pi f}{2f_x}\right)}{V_{DD}(C_{off}+C_x)\pi f}\ . \tag{13}$$

Considering white noise and $B_{eq} >> f_x$, the jitter due to the input noise current of the Op-Amp, i_n, can be expressed as

$$\sigma_\varsigma(i_n)=\frac{1}{V_{DD}}\sqrt{\frac{S_i R_{int}}{2(C_{off}+C_x)}}\ , \tag{14}$$

where S_i is the PSD of i_n. Now, there is no influence from the bandwidth of the comparator and the Op-Amp. Again, the contribution of the 1/f noise is neglectable if the corner frequency of S_i is much smaller than f_x.

C. Final jitter

The jitter for N periods of the oscillator output is given by

$$\sigma_\varsigma=\frac{\sigma_{\Delta(NT_x)}}{NT_x}=\frac{\sigma_{\Delta T_e}}{T_e}\ . \tag{15}$$

where T_e is given by (2). After some extensive calculations, (7) and (14) can be approximated by

$$\sigma_\varsigma(v_n)=\frac{C_{int}}{V_{DD}(C_{off}+C_x)}\sqrt{\frac{(3/2+2(N-1))}{N^2}S_v B_{eq}}\ , \tag{16}$$

$$\sigma_\varsigma(i_n)=\frac{1}{V_{DD}}\sqrt{\frac{S_i R_{int}}{2N(C_{off}+C_x)}}\ . \tag{17}$$

When $N >> 1$, (16) can be expressed as

$$\sigma_\varsigma(v_n)=\frac{C_{int}}{V_{DD}(C_{off}+C_x)}\sqrt{\frac{2}{N}S_v B_{eq}} \tag{18}$$

and then, (8) and (11) can be expressed as

$$\sigma_\varsigma(v_{nc})=\frac{C_{int}}{V_{DD}(C_{off}+C_x)}\sqrt{\frac{2}{N}S_{vc}B_{comp}}\ , \tag{19}$$

$$\sigma_\varsigma(v_{ni})=\frac{C}{V_{DD}(C_{off}+C_x)}\sqrt{\frac{2}{N}S_{vi}B_{amp}}\ . \tag{20}$$

Equations (17), (19), and (20) can be rearranged as

$$\sigma_\varsigma(i_n)=\frac{1}{2V_{DD}(C_{off}+C_x)f_x}\sqrt{\frac{S_i}{2T_e}}\ , \tag{21}$$

$$\sigma_\varsigma(v_{nc})=\frac{C_{int}}{V_{DD}(C_{off}+C_x)}\sqrt{\frac{2}{T_e}\frac{B_{comp}}{f_x}S_{vc}}\ , \tag{22}$$

$$\sigma_\varsigma(v_{ni})=\frac{C}{V_{DD}(C_{off}+C_x)}\sqrt{\frac{2}{T_e}\frac{B_{amp}}{f_x}S_{vi}}\ . \tag{23}$$

So, the jitter given by (21) to (23) decreases inversely to the square root of the measured time T_e. An increase of f_x reduces the jitter, specially the contribution of the noise current. However, when f_x approaches to B_{int} the nonlinearity increases [3,4]. By choosing $f_x < B_{int}/4$ we assure a low nonlinearity, lower than 10 ppm, due to this factor. The use of a low-noise comparator and a low-noise Op-Amp will reduce the jitter. Bipolar Op-Amps have a low noise voltage but a high noise current. On the other hand, JFET and CMOS Op-Amps have a higher noise voltage but a negligible noise

current. So, there will be a trade-off in choosing an appropriate Op-Amp.

The worst-case standard deviation of the jitter due to the quantization noise of the counter is given by

$$\sigma_q = \frac{t_s/2}{T_e}, \tag{24}$$

where t_s is the sampling time. The quantizazion noise decreases inversely to T_e.

As all the noise sources are uncorrelated, the final jitter is given by

$$\sigma_\varsigma = \sqrt{\sigma_\varsigma^2(v_{ni}) + \sigma_\varsigma^2(v_{nc}) + \sigma_\varsigma^2(i_n) + \sigma_q^2}\ . \tag{25}$$

IV. EXPERIMENTAL RESULTS

The capacitive-sensor interface has been applied to a contactless capacitive angular-position sensor [5] and to control an active magnetic bearing actuator. In these applications the capacitances values are lower than 3 pF.

The relaxation oscillator shown in Figure 1 was implemented with C_{off} = 1.8 pF and C_{int} = 10 pF, so the full measurement range for the external capacitances was 3.2 pF (using a rail-to-rail Op-Amp), which is enough for the intended applications. For the Op-Amp (Fig. 1) we used two different types that are representative for two different classes of amplifiers: an OPA2350 and a MAX412. The OPA2350 is a rail-to-rail CMOS amplifier with a low bias current whereas the MAX412 is a low-noise BJT device. For the comparator (Fig. 1) we used two different devices, a MAX942 and an OPA2132. The first one is a high-speed BJT comparator whereas the second one is a JFET-input amplifier with a lower transition time. A summary of the most relevant specifications of these devices is listed in Table 1. These specifications are not listed for the MAX942 because the manufacturer only provides the delay time, which is the parameter of interest in general comparator applications. Because it is a high-speed BJT comparator we can expect that it will have a wide bandwidth and a high noise voltage.

Table 1. Important parameters for the applied amplifiers.

	OPA2350 (CMOS)	MAX412 (BJT)	OPA2132 (JFET-input)
f_T	38 MHz	28 MHz	8 MHz
v_n	5 nV/√Hz	1.8 nV/√Hz	8 nV/√Hz
i_n	4 fA/√Hz	1.2 pA/√Hz	3 fA/√Hz

The interface has been tested with a parasitic capacitance up to 400 pF. In this case, when using a MAX412 as the Op Amp, B_{int} = 0,7 MHz. To accomplish the relation $f_x < B_{int}/4$ in order to reduce nonlinear effects we chose R_{int} = 1.2 MΩ, so f_x will change, theoretically, from 116 kHz, with C_x = 0, to 42 kHz, with C_x = 3.2 pF.

In a first step, the noise performance of the relaxation oscillator (Fig. 1) was investigated. No external capacitance (C_x) was used. We measured the time interval for different number of periods (N) using a universal counter 53132A (Agilent), which has a resolution of 300 ps. The quantization noise did not contribute to the measured jitter. For the theoretical calculations we assumed a residual parasitic capacitance of 5 pF.

Figure 5 shows the results of the jitter using an OPA2350 as the Op-Amp, and an OPA2132 and a MAX942 as comparators. The experimental and theoretical results agree when we use an OPA2132 as the comparator. In this case, the main contribution to the jitter is due to the noise voltages of the Op-Amp and the comparator. The noise current of the Op-Amp has a negligible contribution. As predicted by (18), the jitter decreases inversely to the square root of N. For N = 1000 (measuring time of 8.6 ms) the jitter is $1.7 \cdot 10^{-6}$, corresponding to 19 bits of resolution. A larger (more than twice) jitter was observed using a MAX942 as the comparator. Probably, as compared to the OPA2132, this is due to the larger bandwidth and higher noise level of the MAX942. In this case, due to the lack of data about the input noise and bandwidth of the MAX942, we can not provide a theoretical prediction.

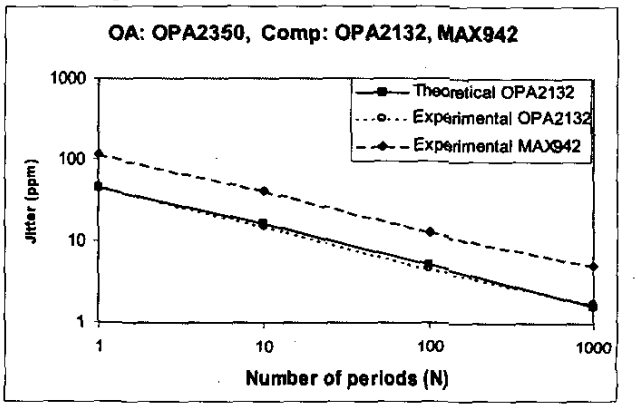

Figure 5. Jitter using an OPA2350 as the Op-Amp, and an OPA2132 and a MAX942 as comparators.

Figure 6 shows the results of the jitter using a MAX412 as the Op-Amp, and an OPA2132 as the comparator. There is a slight difference between the theoretical and experimental results. Now, the jitter is mainly due to the noise current of the Op-Amp and is four times larger than the jitter achieved using an OPA2350 for the Op-Amp. So, in order to reduce the jitter of the oscillator a CMOS Op-Amp is more suitable to be used than a BJT Op-Amp. An increase of f_x could reduce the noise, as predicted by (21), but in this case we should use a faster Op Amp, which normally is noisier.

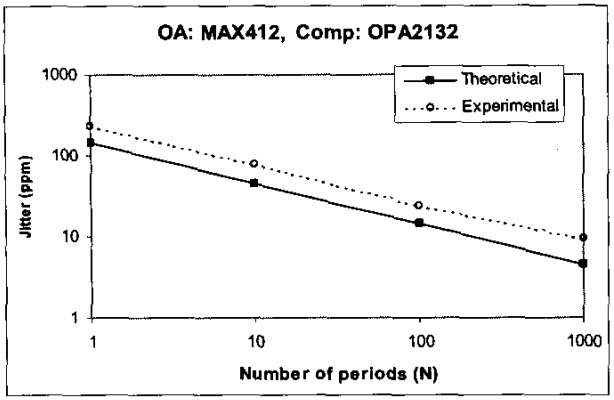

Figure 6. Jitter using a MAX412 as the Op-Amp and an OPA2132 as the comparator.

Figure 7 shows the effect of the parasitic capacitance, C_p, on the jitter. In this measurement we applied the "best" choice using an OPA2350 as the Op-Amp and an OPA2132 as the comparator. For $N = 1$, as predicted by (11) and (12), the jitter increases with an increasing value of Cp.

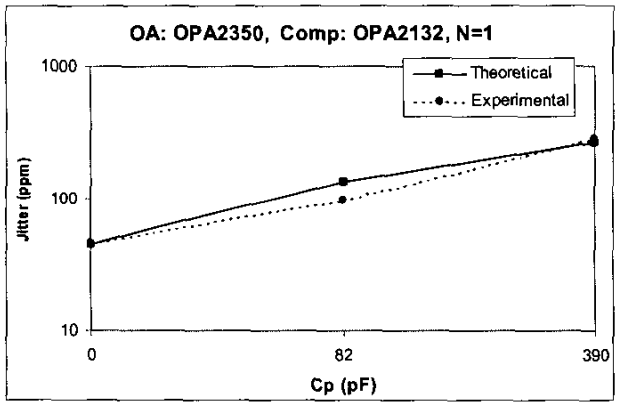

Figure 7. Jitter using an OPA2350 as the Op-Amp and an OPA2132 as the comparator, for N = 1 and different values of C_p.

In a second step, a complete capacitive-sensor interface based on the functional block diagram of Fig. 2 was implemented. We used a 74HC4040 as a counter with a 50 MHz clock (sampling time of 20 ns). As a microcontroller we used a PIC16F876 (Microchip) with a clock frequency of 20 MHz. For the oscillator (Fig. 1) we used $R = 1$ MΩ, $C_{off} = 1.5$ pF, and $C_x = 3.3$ pF, which yields $T_x = 19.2$ µs ($f_x = 52$ kHz).

Figure 8 shows the results using an OPA2350 as the Op-Amp and a MAX942 as the comparator.

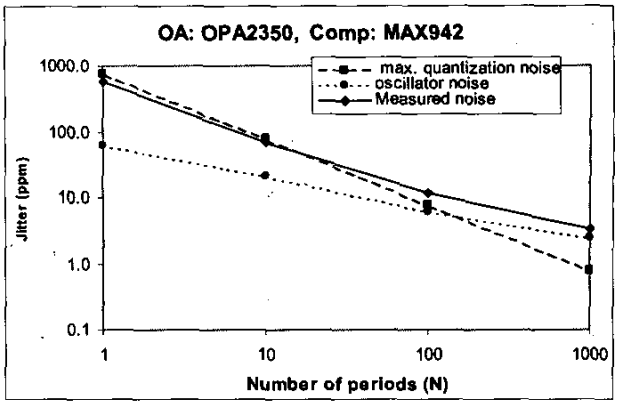

Figure 8. Jitter using an OPA2350 as the Op-Amp and a MAX942 as the comparator. The interval time is measured using the circuit of Fig. 2.

It is shown that up to $N = 100$ the quantization noise limits the resolution. This is due to the low jitter achieved with the relaxation oscillator. When $N = 100$ (measuring time about 1.9 ms) the jitter amounts to $11 \cdot 10^{-6}$ (16.5 bits of resolution). Referred to $C_x = 3.3$ pF this corresponds to a resolution of 36 aF for a measuring time about 2 ms. When $N = 1000$ the resolution is limited by the noise of the oscillator circuit. In this case, the jitter amounts to $3.4 \cdot 10^{-6}$ or 18 bits of resolution. As shown above this high resolution could be further improved by replacing the MAX942 by an OPA2132.

V. CONCLUSIONS

A high-speed capacitive-sensor interface using a simple relaxation oscillator, a fast counter and a microcontroller has been presented. The jitter performance of the relaxation oscillator has been analyzed theoretically in detail so the guidelines for implementing a low-noise oscillator have been pointed out. The theoretical predictions have been proved by experimental measurements using different kinds of Op Amps and comparators. It has been shown that to achieve a low jitter we should use a CMOS Op-Amp with low input noise voltage and a relatively slow, low-noise comparator. The parasitic capacitance at the input of the Op-Amp should be kept at a minimum. A prototype implemented with a microcontroller and a high-speed (50 MHz) counter has been tested. When the measuring time is shorter than 2 ms, the quantization noise of the counter predominates over the noise of the oscillator. A resolution of 16 bits and 18 bits has been achieved for a measurement time of 2 ms and 20 ms, respectively.

ACKNOWLEDGMENT

This work was supported by the Spanish Ministry of Education, Culture and Sport through a post-doc grant PR2001-0281, by the Spanish CICYT under the project

TAP99-0742, and by the Dutch Technology Foundation (STW), The Netherlands, under the Project DEL 4540.

The authors would like to thank F. N. Tóth and E. J. Schnitger, Enraf Delft Instruments, for their guidelines in designing the external counter for the electronic interface.

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