Multi-Valued Logic Circuits on Graphene Quantum Point Contact Devices

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ABSTRACT

Graphene quantum point contacts (G-QPC) combine switching operations with quantized conductance, which can be modulated by top and back gates. Here we use the conductance quantization to design and simulate multi-valued logic (MVL) circuits and, more specifically an adder. The adder comprises two G-QPCs connected in parallel. We compute the conductance of the adder for various inputs and show that Graphene MVL circuits are feasible.

1 INTRODUCTION

Graphene displays quite interesting properties appropriate for be- yond CMOS device design, such as very high thermal conductiv- ity, high electron mobility in room-temperature and the ability to withstand very high current densities [5, 6]. It can therefore be considered as a serious candidate for post-silicon integrated circuit architectures and generally electronics along with its pronounced ability to offer very high speed switching [6].

nanoribbons maintain the highest electron mobility. The G-QPC is placed on a silicon dioxide substrate about 300 nm thick. A metallic contact on a heavily doped n-Si substrate acts as the back gate. The source and drain contacts are also placed on the dielectric. In particular, the corresponding G-QPC device with the proposed dimensions has 6 different quantized conductance levels, 5 of which are broad enough to be actually usable. Those levels are sufficient enough for designing circuits for MVL logic and, more specifically, Radix-4(Quaternary) arithmetics, because they can encode all the

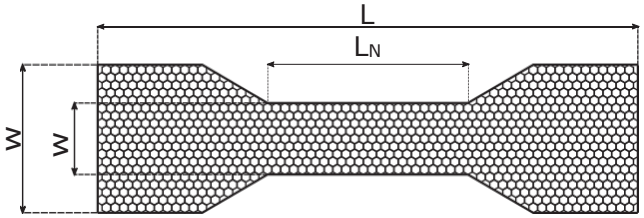

Figure 1: The G-QPC layer of the device used for the radix-4 arithmetic system. The dimensions are $L = 25a$, $L_N = 9a$, $W = 14a$, $W_N = 4a$, where L is the total length of the device, L_N is the length of the shortened area, W is the total width and W_N is the width of the shortened area, respectively.

four necessary digits. We are even allowed to bypass half of them, so that the selected levels are even farther from one another, and the results can be easier separated by appropriate selection. Moreover, the device has also one top gate and one back gate. The top gate is separated from the Graphene nanoribbon by a silicon dioxide layer, so that no electrons can enter the device from either top or back gates. The length of top gate is $5a$, where a 0.246nm is the lattice constant of graphene, while the back gate covers the whole device. In our design, back gate voltage represents the input of the device, while top gate voltage is constant and used only for minimizing small overshoots that may appear at the conductance levels.

In the proposed design, the device conductance changes by applying the appropriate voltage at the back gate of the device. The calculation of this conductance will be done using the non equilibrium Green's function method (NEGF) along with tight binding Hamiltonians [1, 8]. Briefly, the conductance of the G-QPC device, as a function of energy is calculated as follows:

$$G_{value}(E) = \frac{2q^2}{h} Trace[\Gamma_L G^R \Gamma_R G^A] \quad (1)$$

where Γ_L and Γ_R, are the broadening factors, G^R is the retarded Green's function, G^A is the advanced Green's function, $q = 1.6 \cdot 10^{-19} Coulomb$ is the electron charge and $h = 1.06\ 10^{-34}\ J\ s$ the Planck constant. Taking all these into account, equation 1 as found above can be rewritten:

$$G_{value}(E) = 7.7463 \cdot 10^{-5} \cdot Trace[\Gamma_L G^R \Gamma_R G^A] \quad (2)$$

As a result, in the aforementioned equation 2 only $Trace[\Gamma_L G^R \Gamma_R G^A]$ depends on energy and, for specific energy values, the conductance of the device can be computed.

Even though conductance can be calculated for every energy value, only electrons with energies near Fermi Energy level, take part in current flow. Thus, the conductance of only a small region of energies, a few kT above and below energy Fermi, should be taken under consideration. Therefore, the total conductance that a G-QPC device displays, can be calculated as the mean value of conductance for this energy region of interest. In fact, back gate voltage moves the Fermi energy level up or down, and so changes the conductance that the device displays.

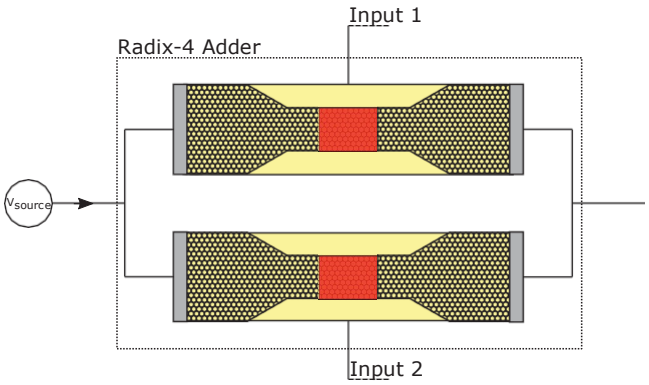

Figure 2: The circuit of the two digit adder. Inputs 1 and 2 represent the terminals for the back gate voltages.

2 THE RADIX-4 NUMERICAL SYSTEM

A radix-4 numeral system, consists of a set of numbers from -3 to 3, including 0. A conversion to the more common decimal system can be achieved with the following equation [7]

$$D = \sum_{i}^{n} x_i \cdot 4^i \quad (3)$$

where x_i represents a number from the set described above. In this case, we used an unsigned number representation, so the digits that we will take under consideration are [0,1,2,3]. Such a system is very convenient to use, because the radix proposed, is a power of 2, and the conversion from and to the binary system is straightforward and efficient. Thus, devices using a radix 4 system, could be easily designed along with today's very mature binary logic circuits, even as interconnects, with the advantage of optimizing the connection wiring between binary subsystems [9]. The operation of addition in such a numeral system is described in [4].

3 HIGH RADIX G-QPC CIRCUIT

By using the G-QPC device that exploits the unique characteristics of Graphene, and the quantization of conductance that is displayed, we propose here a radix 4 adder. For the creation of a two Quaternary-digit adder, we connected two G-QPCs in parallel, as shown in Figure 2. In this figure, yellow background represents the silicon dioxide layer behind of which the back gate is placed, while the two grey regions on the left and right depict the source and drain contacts, respectively. Moreover, the red region in the middle is the top gate. As mentioned before, with the application of the appropriate voltage at each back gate we are in position to tune the devices at specific conductance level. Thus the output current will differ, for different combinations of inputs. V_{SOURCE} can be set at any value that will not damage the device, and fortunately, Graphene can sustain high current densities and therefore high source voltages. Though, it would be more convenient to use voltages similar to those already used on the back or top gates. The current that will run through the device, will be measured at the output and will determine the result of the addition.

Quaternary Digit	Back Gate Voltage(Volts)
0	0.13
1	−2.7
2	−2.15
3	−1.45

Table 1: Correlation between the Quaternary system digits and back gate voltages used for tuning properly the G-QPC device

The devices shown in Figure 2 are tuned separately, but the total conductance that will arise, will determine the result of the addition being executed. The total conductance of a circuit with devices in parallel connection, can be easily calculated by:

$$G_{TOT\,AL} = G_1 + G_2 \tag{4}$$

The potentials applied to the back gates are specific, and each one represents one digit out of the four that make up a Quaternary numeral system. Those correlations between back gate voltages and Quaternary digits can be seen at the following Table 1.

The specific back gate voltages mentioned above, were chosen so that each digit, is represented by only one predefined conductance value. Moreover, changing the back gate voltage of one device, so as to move from one digit to the next or the previous one (i.e. from 2 to 3 or 1), corresponds to an equal change in conductance, as shown in Figure 3. This last property of the selected conductance levels eliminates the danger of error in case of additions with same result but different added digits, and makes the circuit scalable by allowing the simultaneous addition of n bits. That can be achieved with the use of n G-QPC devices connected in parallel.

At this point, an advantage of using G-QPC devices for radix 4 addition is that, the parallel combination of such devices, creates more conductance levels than those available at a single device. More specific, through the parallel connection of two G-QPC devices, results higher than 3 (the highest digit that a radix 4 numeral system can depict), can be encoded and represented, without further circuitry. Carry does not necessarily need special manipulation.

4 SIMULATION RESULTS

In this section numerical simulations of the G-QPC devices forming the Radix-4 adder circuit as discussed before are presented. The simulation results are expected to be in accordance with quaternary addition described in [4] and show that the proposed circuit maps correctly an addition in a higher radix (4) numeral system.

As described above, the region of interest in those diagrams is a few kT above and below $E = 0$, which corresponds to Fermi energy. In Figures 3 conductance is depicted for a wide range of energies, from $E = -0.5$ to $E = 0.5$ in units of $((E - E_F)/\tau)$, where $\tau = -2.7eV$ is the overlap integral for atoms that are nearest neighbors[8]. However, the mean value of conductance and therefore the mean value of resistance, presented in Table 2, are calculated using values for a range of energies from $E = -0.1$ to $E = 0.1$ in units of $((E - E_F)/\tau)$. Also, in those figures, conductance (x-axis) is normalized. More precisely, x-axis corresponds to $Trace[\Gamma_L G^R \Gamma_R G^A]$.

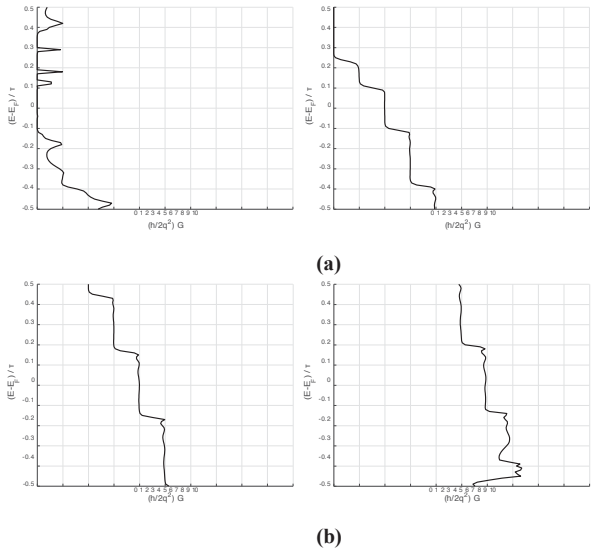

Figure 3: Conductance of a single G-QPC device. In (a), the two subfigures, from left to right, demonstrate the conductance of the device for input digit 0 ($-0.13V$) and input digit 1 ($-2.7V$) respectively. In (b), the two subfigures, from left to right, demonstrate the conductance of the device for input digit 2 ($-2.15V$) and input digit 3($-1.45V$) respectively

In Figure 4 the results of the proposed Radix-4 adder circuit are presented. The nature of the circuit implies that changing input 1 with input 2, and input 2 with input 1, would not bring any difference to the result, so only one of those calculations are depicted. For example 0+1 and 1+0 have the same result, 1+2 and 2+1 have the same result, and so on. In all the subfigures presented in Figure 4, top gate voltage does not change, it is constant and its value is $V_{TG} = 0.07Volts$. The variable is back gate potential which determines the inputs, as mentioned above.

Based on 1 for the inputs of the devices, the results are as expected, and show that the proposed circuit indeed maps a Radix-4 addition. It can be easily distinguished that the devices, in additions with the same result, irrespective of the inputs, are tuned so that the total conductance of the circuit is the same, and thus the current that will run through it, will also be the same.

We also calculated the mean value of adder's resistance for the energy region of interest, as mentioned above. This mean value is calculated for every possible 2 digit addition in a Radix-4 system, and is presented in Table 2. We applied a source potential of $1Volt$, and calculated the current that runs through the device. The current was calculated using the corresponding Ohm's law:

$$I = \frac{V_{SOU\,RCE}}{R_{MEAN}} \tag{5}$$

Table 2 is an other view of the results shown in Figure 4. The visualization of the table (Figure 5) leads to the result that operations with the same result, indeed conduct the same amount of current through the device, while the current difference between consecutive results (i.e. between 1 and 2, 2 and 3 etc.) is almost the

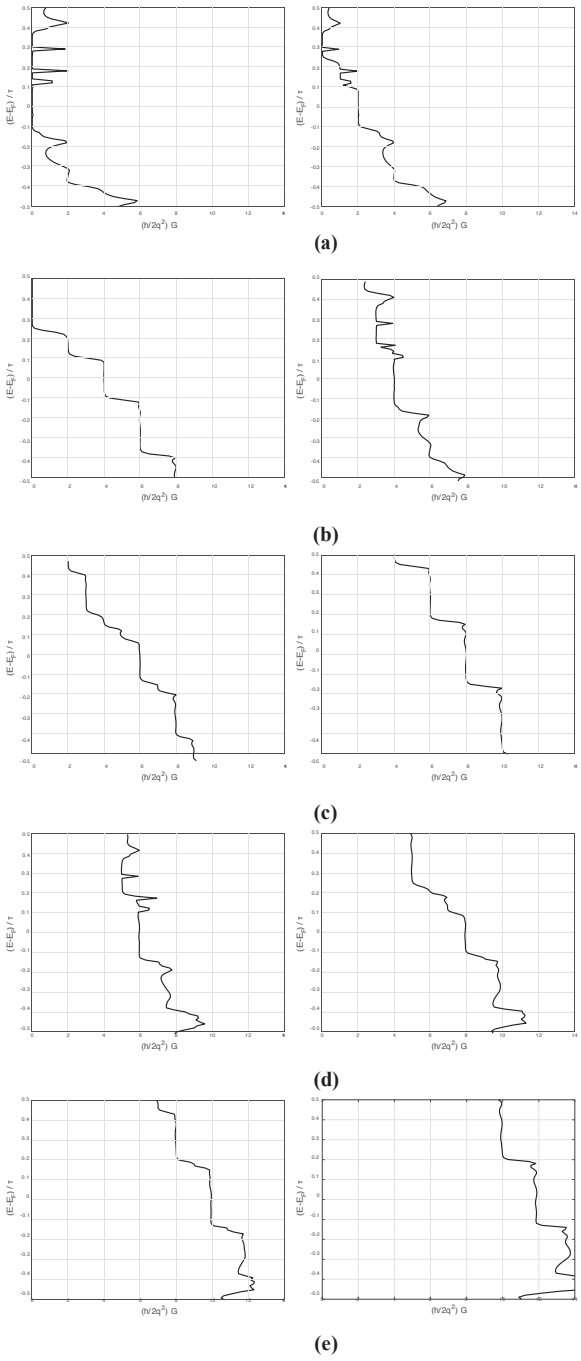

Figure 4: Conductance of the proposed circuit for every possible input combination for 2-digit addition. More specific, from left to right we have: In (a), operation 0 + 0 **and** 0 + 1**. In (b), operation** 1 + 1 **and** 2 + 0**. In (c), operation** 2 + 1 **and** 2 + 2**. In (d), operation** 3 + 0 **and** 3 + 1**, and finally in (e), operation** 3 + 2 **and** 3 + 3

same. It is also obvious that the higher the result of the operation, the higher is the current running through the device.

Calculations	Result	R_{MEAN} (Ohm)	Current(Ampere)
0+0	0	$2.6798 \cdot 10^{7}$	$3.7316 \cdot 10^{-8}$
1+0	1	$6.5291 \cdot 10^{3}$	$1.5316 \cdot 10^{-4}$
1+1	2	$3.2719 \cdot 10^{3}$	$3.0564 \cdot 10^{-4}$
2+0	2	$3.2443 \cdot 10^{3}$	$3.0823 \cdot 10^{-4}$
2+1	3	$2.1686 \cdot 10^{3}$	$4.6112 \cdot 10^{-4}$
2+2	0	$1.6238 \cdot 10^{3}$	$6.1585 \cdot 10^{-4}$
3+0	3	$2.1787 \cdot 10^{3}$	$4.5900 \cdot 10^{-4}$
3+1	0	$1.6343 \cdot 10^{3}$	$6.1188 \cdot 10^{-4}$
3+2	1	$1.3044 \cdot 10^{3}$	$7.6662 \cdot 10^{-4}$
3+3	2	$1.0901 \cdot 10^{3}$	$9.1738 \cdot 10^{-4}$

Table 2: The results of the simulations in numbers

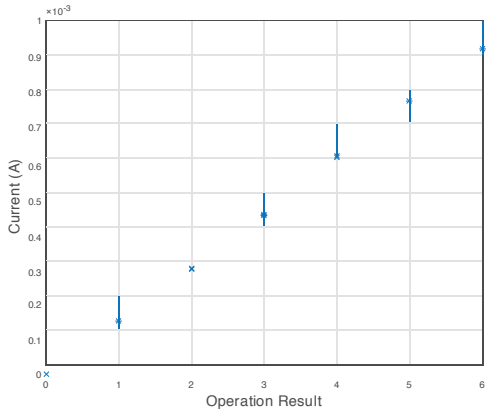

Figure 5: Visualization of Table 2. Shows the correlation between current running through an adder, and the result of the computation

5 CONCLUSIONS

We used G-QPC connected in parallel to design a MVL adder. We used non-equilibrium Green's functions combined with tight binding Hamiltonians to compute the conductance of the device for various input values. The inputs of the adder are the two back gate potentials. The output is the combined conductance and, therefore the current. The back gate voltages assign a predefined conductance to each digit. The addition errors are eliminated because the change in back gate voltages correspond to discrete equidistant conductance values. The proposed adder is scalable and allows the simultaneous addition of n bits.

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