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# Smart AC Storage based on Microbial Electrosynthesis Stack

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*Abstract—* **In this paper, a variable and smart energy storage system, consisting on a two-level voltage source converter with LCL filter and Microbial Electrosynthesis (MES) stack, is presented. This energy storage system is able to contribute to damp the variability of renewables and provide grid services, by controlling the active and reactive power exchanged with the grid and can be considered as another alternative in the market of storage normally centered in batteries. The proposed system converts electrical energy into methane, taking waste water as another input. The converted energy inside the MES presents a new degree of freedom, which can be exploited to provide ancillary services such as energy management, frequency regulation, voltage profile improvement and oscillation damping. The big challenge for controlling this system lays on the fact that the dc bus voltage of the converter has to be changed in order to regulate the exchanged active power with the grid. This paper presents a cascaded approach to control such system by means of combining extern control loops with fast inner loops. The outer power loop, with a PI controller with special limitation values and anti-windup capability, is used to generate dc bus voltage reference. An intermediate loop is used for dc bus voltage regulation and current reference generation. A new proportional resonant controller is used to track the current reference. The proposed scheme is validated through real-time simulation in OPAL OP4510 hardware in the loop system.**

*Keywords— Energy storage; microgrid; Microbial Electrosynthesis (MES) stack; proportional resonant controller .*

## I. INTRODUCTION

The electricity production from Renewable-based Distributed Generation (DG) technologies energies has rapidly increased due to the growth of electrical energy consumption and the environmental concerns [1-2]. Microgrids were introduced as a flexible and proper platform for facilitating the integration of DGs, loads, and energy storage systems [3-4]. In the microgrid, the loads and renewable based energy resources have a random and unpredictable behavior [5-6]. Therefore, using energy storage systems and programmable generators are necessary in order to control the voltage, frequency and power exchanged with the upstream network [7-8]. Capacity constraints are the biggest limitation of the common energy storage systems, such as batteries, that has led to the development of new electrical energy storage technologies [9].
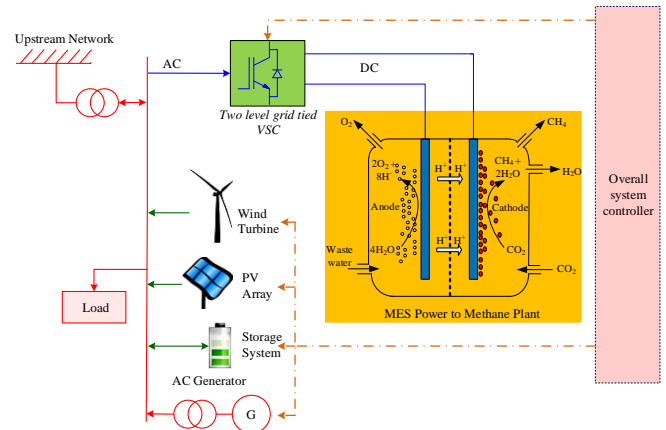


Fig. 1. Schematic of a microgrid with smart storage based on MES power plant.

The Power-to-Gas (P2G) especially Power-to- Methane technology might contribute to tackle this problem [10-11]. The P2G process links the power grid with the gas grid by converting electrical energy into a grid-compatible gas. The position of P2G plants for management high contributions of renewable energies has been discussed in [12-13].

In this paper, a smart and variable AC storage with the ability to receive active power from the grid and to exchange reactive power with the grid is proposed (see Fig. 1). To achieve this goal, the proposed topology for the power converter is a two-level voltage source converter (2LVSI) because 1) MES stack has to be fed by DC voltage 2) 2LVSI is able to draw the sinusoidal current from the grid. Also, the proposed control scheme consists of three loops, outer power loop, middle DC link voltage loop, and inner current loop, which is implemented in the stationary reference frame. The contribution of control scheme consists of two parts, first a new Proportional-Resonant (P+R) controllers with harmonic compensation capability and anti-windup capability to be used as the current controller, and secondly a new dc link voltage reference modifier, which defines the appropriate reference to keep the system stable.

This paper is organized as follows. In section II, microbial electrosynthesis energy storage is briefly introduced. In Sections III, the description of the proposed topology scheme and its control system are presented. In Section IV, the simulation results that permits to analyze the performance of

the proposed controller are presented. Finally, the conclusions that arise from this work are presented in Section V.
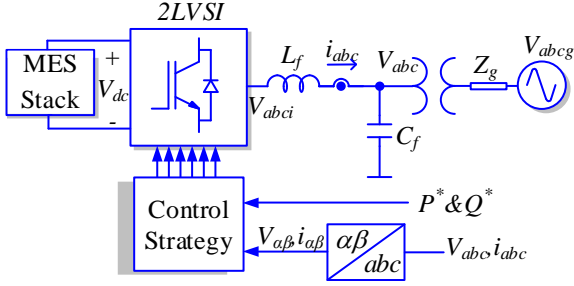


Fig. 2. Overall schematic of proposed smart load.

## II. MICROBIAL ELECTROSYNTHESIS STEAK

Microbial electrosynthesis (MES) is a form of microbial electrocatalysis in which electrons are supplied to living microorganisms by applying a dc voltage to the stack [14]. The electrons are then used by the microorganisms to reduce carbon dioxide to yield methane and clean water from wastewater:

$$CO_2 + 8H^+ + 8e^- \rightarrow CH_4 + 2H_2O, \qquad (1)$$

Waste streams from biorefineries e.g. biodiesel and bioethanol plants and wastewaters are possible substrates for MES. MES integration helps biorefineries realizing the full polygeneration potentials, i.e. recovery of metals turning apparently pollutants from biorefineries into resources, creation of chemicals and biofuels from reprocess of CO2 and clean water [15]. Also, the produced methane can be transferred to natural gas distribution utility and there is not any difficulty related gas storage [16].

## III. PROPOSED TOPOLOGY AND ASSOCIATED CONTROL SCHEME

In this paper, it is supposed that the overall system controller can send the value of the power reference to the MES power plant. The MES power plant, as it counts on a 2LVSI as the interface, converts power reference to DC link voltage reference, then it is tracked by voltage controller and current controller. For a 2LVSI the relationship between DC side and AC side voltage can be expressed as (see Fig. 2) [17]:

$$V_{dc} = \frac{2V_i}{m} \qquad (2)$$

where $V_i$, $V_{dc}$ and $m$ are the maximum phase voltage of 2LVSI, DC bus voltage and 2LVSI modulation index, respectively. The values of $m$ depends on switching method and it can change from zero until 1.1507 [18]. Therefore, DC bus voltage can change between a minimum value and infinitive.

The proposed control scheme consists of three main parts (see Fig. 3): 1) dc link voltage reference generation in the outer power loop, 2) in the middle dc link voltage loop, 3) inner current loop with P+R controllers with harmonic compensation and anti-windup capabilities.

In the outer loop according to Fig. 3, the active power reference compares with the output active power of 2LVSI, then the error passes through the PI controller to find initial DC

link voltage reference $V_{dcref}$. In the present application, the grid voltage is fixed, hence for operation of 2LVSI in the linear region, the DC link voltage should be higher than the specific value. The DC link voltage reference modifier is proposed to keep 2LVSI under control and also avoid the system becomes unstable. The output of DC link voltage reference modifier $V^*_{dc}$ is used as a reference for middle DC link voltage loop. The reference of current in the stationary reference frame can be found based on the output of DC link voltage controller, reactive power reference and the positive sequence of point of common coupling (PCC) voltage. The current reference is tracked by the proposed proportional resonant controller with anti-windup and harmonic compensation capabilities (see Fig.3).
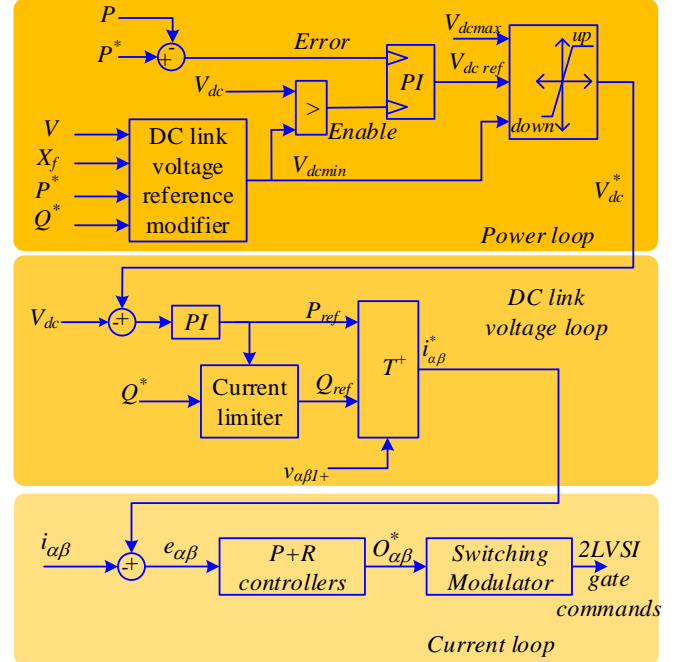


Fig. 3. Proposed control scheme.

### A. DC bus voltage reference modifier

To prevent converter instability, a new DC bus voltage reference modifier will be proposed. This method does not require to the values of the grid voltage ($V_g$) and the equivalent grid impedance ($Z_g$), and certificates the converter to stay stable for any active and power references. Considering the equivalent circuit diagram of system in Fig. 4, the active and reactive powers absorbed by the converter from the PCC can be inscribed as follows:

$$P = \frac{V.V_i}{\underbrace{X_f}_{S}} \sin\delta = S \sin\delta, \qquad (3)$$

$$Q = \frac{\left(V V_i \cos\delta - V^2\right)}{X_f} = S \cos\delta - \frac{V^2}{X_f}, \qquad (4)$$

Squaring the relationships of P&Q in (3) and (4), and reordering,

$$P^2 + (Q + \frac{V^2}{X_f})^2 = S^2 (\sin \delta)^2 + S^2 (\cos \delta)^2 = S^2 \tag{5}$$

Therefore, the converter must produce the following voltage to exchange power with grid:

$$V_i = \frac{X_f}{V} \sqrt{(Q + \frac{V^2}{X_f})^2 + P^2}, \tag{6}$$

For a grid with fixed voltage, the minimum DC bus voltage can be found as:

$$V_{dc} \geq \sqrt{3} V_i \rightarrow V_{dc} \geq \frac{X_f \sqrt{3}}{V} \sqrt{(Q + \frac{V^2}{X_f})^2 + P^2} \tag{7}$$

Fig. 5 shows the minimum DC link voltage $V_{dcmin}$ based on active and reactive powers. It can be concluded that $V_{dcmin}$ is directly related to reactive power, and almost independent of active power.
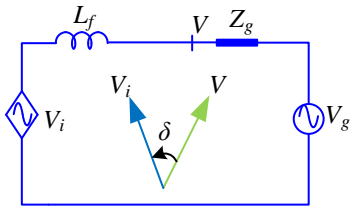


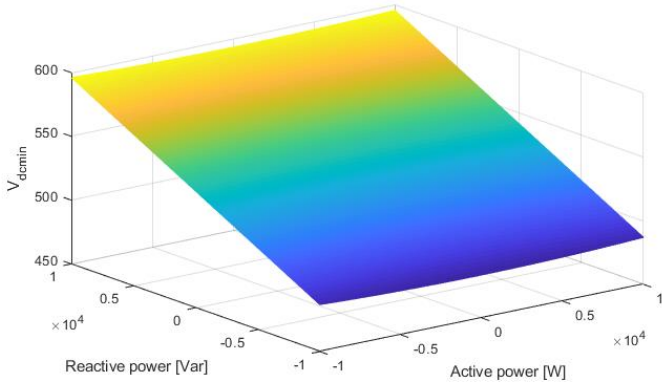Fig. 4. Modelling converter of smart load as a voltage source.



Fig. 5. Minimum DC link voltage based on active and reactive powers.

## B. Proposed P+R controllers

In fact, the anti-wind up of the P+R controllers and the dc voltage reference modifier must work complementary together. In the transient case, the anti-windup part of the P+R controllers limits the input of the switching modulator (SM) and avoids the saturation of the integral terms of the P+R controllers. In steady state, the dc voltage reference modifier does not allow to reduce dc link voltage lower than specific value and avoids the saturation of the controller. To draw a sinusoidal current from the grid, a P+R controllers with harmonic compensation capabilities should be used, a typical ones can be expressed as:

$$PR = K_p + \sum_{h=1,3,5,\dots}^{odd} \frac{2K_{ih}\omega_{ch}s}{s^2 + 2\omega_{ch}s + h^2\omega_o^2} \tag{8}$$

where $h$, $K_p$, $K_{ih}$, $\omega_o$ and $\omega_{ch}$ are harmonic order, the proportional coefficient, the resonant coefficients, the resonant frequency and the resonant bandwidths, respectively. The output of the P+R controllers (input switching modulator) have to be smaller than the specific value $O_{max}$, otherwise there will be over modulation. In over modulation, the switching frequency is reduced and the waveforms at the converter's output are distorted.

The suggested anti-windup scheme for P+R controllers consists of three mains parts (see Fig. 6): AC limiter, anti-windup for resonant controller in fundamental frequency, and anti-windup for resonant controllers in the other frequencies. The AC limiter (ACL) to limit the input of SM can be considered as [19]:

$$\begin{cases} |O_{\alpha\beta}| = \sqrt{O_\alpha^2 + O_\beta^2} \\ O_{\alpha\beta}^* = O_{\alpha\beta}, & |O_{\alpha\beta}| < O_{max} \\ O_{\alpha\beta}^* = \frac{O_{max}}{|O_{\alpha\beta}|} out_{\alpha\beta}, & |O_{\alpha\beta}| > O_{max} \end{cases} \tag{9}$$

With this limiter, the input of SM has no clamp and it is at all times sinusoidal. The value of $O_{max}$ is chosen based on the switching method.

The integrators within the controller may experience wind-up while a limiter hinders the output of a controller. In proposed controller, the ACL is used inside of anti-wind-up as the core block. If the absolute value of the output of the controller $|O_{\alpha\beta}|$ is more than the threshold $O_{max1}$, the harmonics compensation is canceled, so that the controller still has the ability to track the current reference at the fundamental frequency. Also, the difference between the AC limiter (ACL) and the controller's output lays mainly on the feedback signal to compensate the inputs of the integrators of resonant controller in the fundamental frequency, so if the $|O_{\alpha\beta}|$ is going higher than threshold $O_{max}$, the output of P+R controllers is clamped by AC limiter and the input of resonant controller in the fundamental frequency is modified by anti-windup scheme.

The main important variables in the anti-windup scheme are the maximum available outputs of the P+R controllers ($O_{max}$ and $O_{max1}$), which should be chosen based on $V_{dc}$. The proposed values for thresholds are given as:

$$O_{max1} = \frac{V_{dc}}{2} - \frac{t_{dead}}{T_s} V_{dc}, \tag{10}$$

$$O_{max} = \frac{V_{dc}}{\sqrt{3}} - \frac{t_{dead}}{T_s} V_{dc}, \tag{11}$$

where $t_{dead}$ and $T_s$ are the switching dead time and the switching period, respectively.
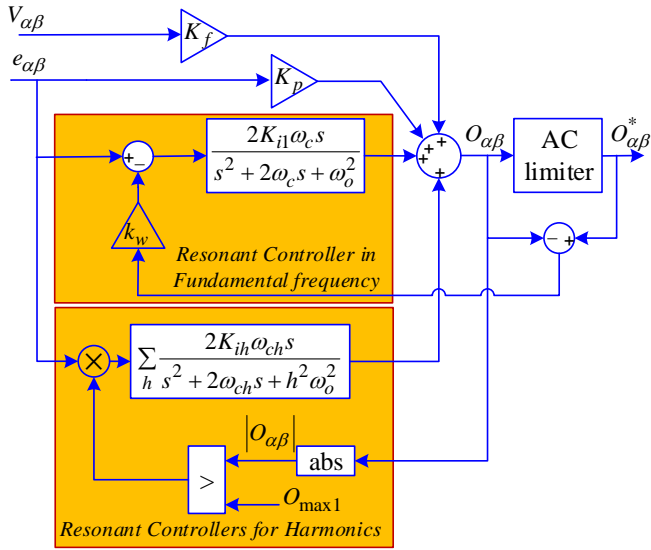
Fig. 6. P+R controllers with anti-wind-up capability and harmonic compensation capability in the inner current loop.

## IV. REAL TIME SIMULATOR RESULTS

This paper uses OPAL-RT-OP4510 as a real-time simulator to verify the effectiveness of the proposed AC smart load topology.

The real-time simulators are one of the best tools to evaluate the advances in power switching devices and power electronics converters impact different industries, applications, and emerging technologies. Armed with a powerful Xilinx Kintex7 FPGA and the latest generation of Intel Xeon four-core processors, the OP4510 provides raw simulation power for both sub-microsecond time and CPU-based real-time simulation step power electronic simulation. This feature makes it possible to couple high-speed FPGA-based models, such as power electronics converters and electric drives, to slower electrical and mechanical systems on the CPU, providing even more detailed simulations.

Fig. 7 and Fig. 8 show the schematic and setup of implementation of proposed system in OPAL-RT. The hardware part includes switches, diodes, electrical components and voltage and current sensors is implemented in FPGA. The hardware part runs fast with sample time 875ns second. The control system is implemented in CPU part and runs slow with sample time 10µs. Due to the increase in the switching frequency, the time step of the real time model should be much lower than the converter's switching time step. Typical CPU-based real time simulation can only realize a minimum time step of Ts ≥ 10 µs affected by the large bus latencies in a CPU. Also, the OP4510 connects to an oscilloscope to monitor voltage, current and electrical power in real time. The values of currents and voltages are routed from the FPGA based model to the DAC channels directly.

The parameters of 2LVSI of proposed AC smart storage are listed in Table 1. According to [20-21], MES stack has a very slow dynamic and its time constant is around several hours. Therefore, it is modeled as a passive circuit with curve fitting

of available data. Two simulation have been done to verify the performance of the proposed system.
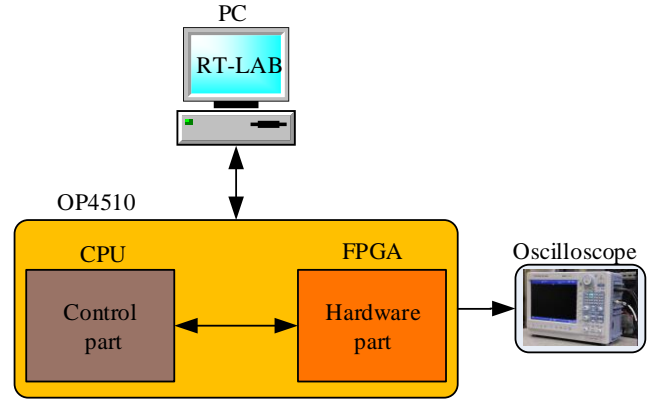


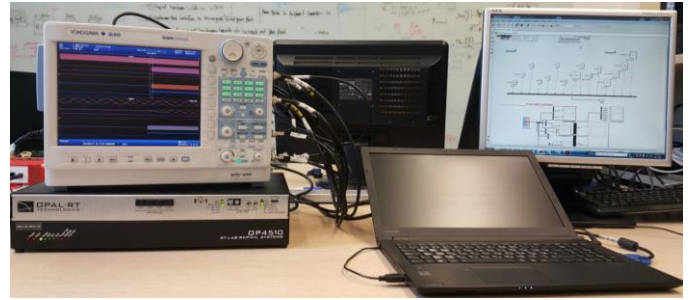Fig. 7. Schematic of implementation of proposed system in OPAL-RT.



Fig. 8. Real time simulator setup.

Table 1    2LVSI parameters.

| Parameter | Value |
|---|---|
| Grid voltage | 380V-50Hz |
| Grid short circuit capacity (SCC) | 10kA |
| Nominal power | 10kVA |
| LC filter inductor ($L_f$) | 3.4mH |
| LC filter capacitor ($C_f$) | 5 µF |
| Switching frequency | 10kHz |
| DC link capacitor ($C$) | 2200 µF |

In the first test, the active power reference step up from zero to nominal value (10kW) and reactive power reference is set 0Var. The obtained results are shown in Fig. 9 and Fig. 10. As can be seen in Fig. 9, despite the fact that the reference power is zero, the DC bus voltage is limited to 543V to prevent system instability, and thus the active power absorbed by the 2LVSI is non-zero. Once the reference of active power is changed from zero to 10 kW, the DC bus voltage increases, and the reference and the instantaneous value of active power become exactly the same. As shown in Fig. 9, the voltages of the LC filter's capacitors are constant, and the grid current increases with convenient and fast transient response. According to Fig. 10, the current reference in stationary reference frame is correctly followed by the controller, and before increasing the power reference, the peak of the switching duty cycle is close to its maximum value and the system is controlled at the boundary of stability and instability. By increasing the power reference and also DC bus voltage, the value of switching duty cycle are reduced and the converter

works in the linear region. Also, the dynamics of DC voltage variations is shown in Fig. 10, which has the same behavior as a first-order system with a raise time about 60 ms.
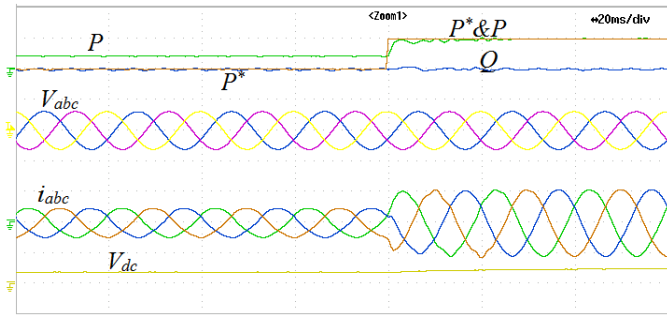


Fig. 9. Real time simulator results: active power reference step-up for the smart storage. From top: active power reference ($P^*$, 10kW/div), active power ($P$, 10kW/div), reactive power ($Q$, 10kVA/div), grid voltage ($V_{abc}$, 1000V/div), grid current ($i_{abc}$, 20A/div), DC link voltage ($V_{dc}$, 1000V/div).
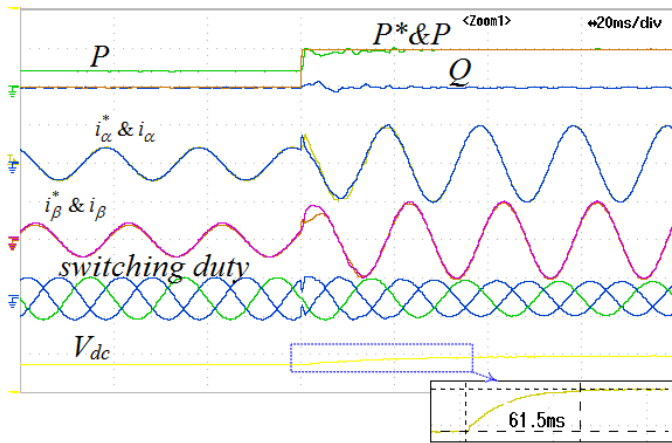


Fig. 10. Real time simulator results: active power reference step-up for the smart storage. From top: active power reference ($P^*$, 10kW/div), active power ($P$, 10kW/div), reactive power ($Q$, 10kVA/div), actual and reference currents, Switching duty cycle, DC link voltage ($V_{dc}$, 1000V/div).
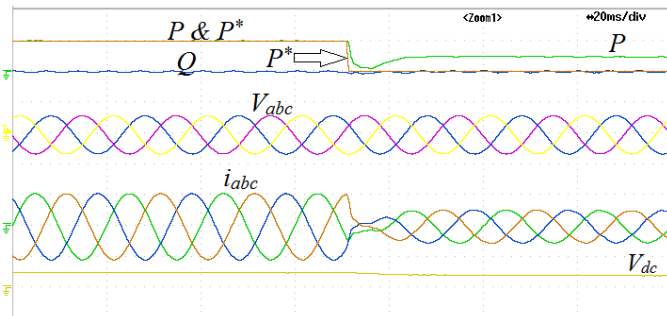


Fig. 11. Real time simulator results: active power reference step-down for the smart storage. From top: active power reference ($P^*$, 10kW/div), active power ($P$, 10kW/div), reactive power ($Q$, 10kVA/div), grid voltage ($V_{abc}$, 1000V/div), grid current ($i_{abc}$, 20A/div), DC link voltage ($V_{dc}$, 1000V/div).
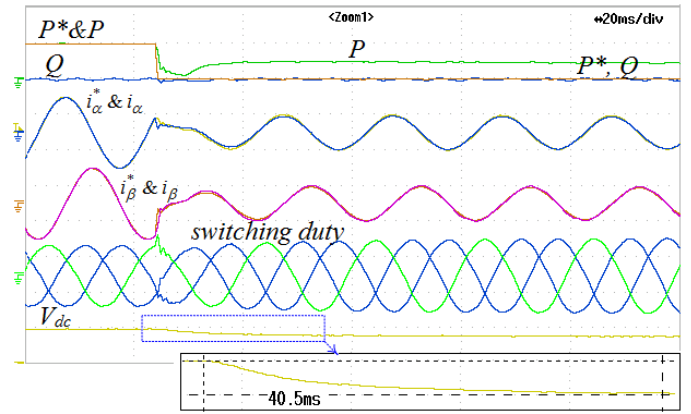


Fig. 12. Real time simulator results: active power reference step-down for the smart storage. From top: active power reference ($P^*$, 10kW/div), active power ($P$, 10kW/div), reactive power ($Q$, 10kVA/div), actual and reference currents, Switching duty recycle, DC link voltage ($V_{dc}$, 1000V/div).

The results for reducing active power reference from 10kW to zero are shown in Fig. 11 and Fig. 12. The most important event happens at the moment that the active power reference changes, dc voltage reference modifier and anti-windup of P+R controllers prevent from increasing switching duty cycle and system instability. The DC bus voltage decreases gradually in 40 ms, thus it is possible to continue connecting proposed AC load to the grid.
The presented results show that the prosed smart AC load can exchange power with the grid with a good transient response and zero steady state error.

## V. CONCLUSION

In this paper, the feasibility of designing a smart AC storage based on MES energy storage and conventional two-level voltage source converter was addressed. A cascade three loops control scheme has been proposed to track power references, avoid converter uncontrollability and keep grid current sinusoidal. The results of the implementation of the proposed storage in OPAL-RT OP4510 simulator show that the system maintains good performance for exchanging power with the grid.

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