Modern Gain-Cell Memories in Advanced Technologies

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***Abstract*— With the advent of the slowdown in DRAM capacitor scaling [1] and the increased reliability problems of traditional 6T SRAM memories [2], industry and academia have looked for alternative memory cells. Among those, gain-cells have attracted significant attention due to their smaller size (compared to SRAM) and non-destructive read operation (compared to DRAM) as well as considerable low power and reasonable robustness. This paper first summarizes the available evidences of SRAM and eDRAM in commercial and test chips. Then, it analyzes the performance, reliability and scaling of eDRAM gain-cells in 10 and 7 nm FinFET technology; as well as above and below V_T (i.e. sub-threshold).**

Keywords—SRAM, DRAM, gain-cells, FinFET

I. Introduction

SRAM memory cells have dominated computing systems for on-chip memory in the last decades. Similarly, capacitor-based DRAM has dominated off-chip memory (i.e. main memory). Despite the dominance, recent studies have shown the difficulties of continuous scaling of DRAM cells [1], as well as, instability/reliability issues in SRAMs. As an alternative, several authors have studied eDRAM gain-cells as a viable solution. Table 1 compares the pros and cons of several SRAM and DRAM cells and it points to documented industrial work/collaborations and academic tape-outs that use these cells. SRAM still dominate the market, yet, we can see a rising interest from industry for eDRAM gain-cells.

The following sections provide a succinct characterization of gain-cells in advanced technologies (10 and 7 nm FinFET; as well as, at sub-threshold voltages) in terms of robustness, process variability and aging, for different modern technologies and sub-threshold domains (sub-V_T). For space reasons, we will not include energy results, another factor in favor of eDRAM. We will focus our attention mainly on 2T, 2T1D, 3T and 3T1D eDRAM cells.

II. Concept of Gain Cell Memories

A. Description of 2T, 2T1D, 3T and 3T1D gain-cells

All these cells are technologically compatible with conventional CMOS, avoiding the specific layers and processes required for the implementation of the capacitor in 1T1C-DRAM. Fig. 1 shows the schemes of the circuits for the four types of eDRAMs. The main difference between the 2T and 3T is that the latter includes an additional reading path and device (T3) that improves the reading access time. In the case of 2T1D and 3T1D, the cell includes a gated-diode (D) that it has an effect of storage device with amplified consequences. This gate-diode increases the retention time and read/write speed. We have simulated it by using the Predictive Technology Models for multi-gate devices High Performance (PTM-MG HP) [22].

B. Retention time (RT)

Gain-cells are fundamentally dynamic memories. Consequently, the value stored in the cell degrades/leaks over time. Unless, the value is refreshed (i.e. rewritten), the value is lost. The time in between refreshes is defined as retention time.

Table 1: SRAM and eDRAM characteristics and documented industrial products and tests

Cell type	SRAM			eDRAM		
	6T	**8T**	**10T**	**3T**	**2T**	**1T1C**
Access time	Good	Not so good	Not so good	Good	Good	Bad
Energy						
Area	Not so good	Bad	Bad	Good	Good	Good
Reliability	Bad	Better	Better	Good	Good	Good
Industrial Test	Widely used	ST [3] IBM [4] TSMC/Video [5]	ST [3] IBM [4] Reneseas/Ko [9]	EPFL [10] UM/LDPC [11] Hitachi [12] STARC [13]	Intel/Memory [14] UM/Biomedical [15] EPFL/Biomedical [16]	Samsung/Camera [17]
Industrial Products		Intel Atom [6] Intel Nehalem [7] AMD Llano [8]				Intel Broadwell [18] IBM Power [19]

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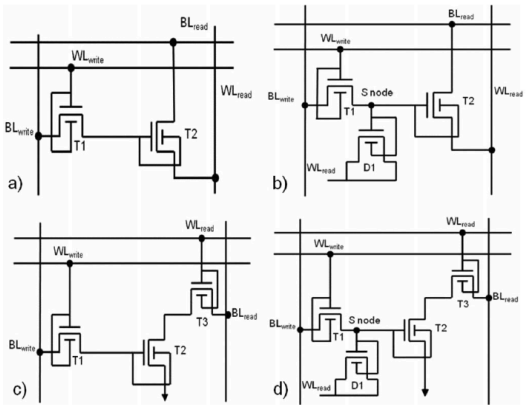

Fig 1. Structure of gain-cells a) 2T, b) 2T1D, c) 3T, d) 3T1D [20].

Fig. 2 compares the retention time for 20/22 nm FinFET and planar bulk technology nodes for the four eDRAM cells and different implementation strategies (all transistors in cell are pMOS, nMOS or mixed [20]). A mixed cell is defined as a cell where T1 is pMOS and the rest are nMOS. The pMOS version shows the highest RT, followed closely by the mixed cell.

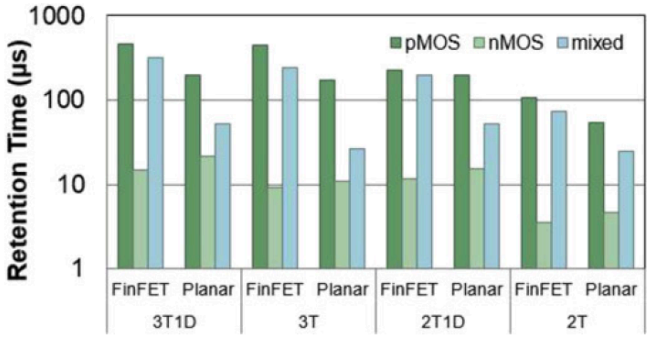

Fig. 2. Retention time at 22 nm using FinFET devices [20].

Fig. 3 shows results of the impact on RT (retention time, one of the key parameters in eDRAM) variability due to process fluctuations. Two levels of variability are considered at device level, Moderate (6% for bulk and 3% for FinFET) and High (15% bulk, 7% FinFET). FinFET technologies show a 50% reduction in parametric variability for the same technology node [21]. In conclusion, the best performing cells (pMOS) are the ones that have less variability; eDRAM cells can be implemented with a single transistor type.

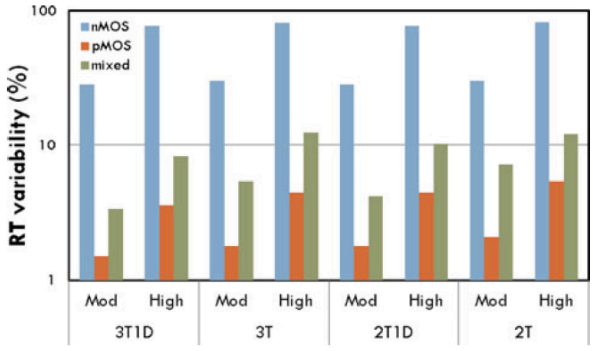

Fig. 3. RT variability levels when an eDRAM under moderate and high device variability levels [20].

III. Gain-Cell in 10 nm FinFET Technology

A. Performance analysis

Being the 3T1D the cell with better performance, we will concentrate on this configuration in this section. In the circuit in Fig. 1, all the transistors use a configuration where gate and back gate are shorted, this configuration is called SG (Single Gate) configuration. Certain FinFET technologies allow also a complementary biasing of the back gate configured as an independent gate (IG).

Fig. 4 shows the Retention Time (RT) and Write/Read Access Time (WAT and RAT) for different IG device configurations (all transistors in 3T1D are IG, or only n-type devices are IG: IGn). Full IG and IGT1 –where only T1 is IG- stand out clearly as the best alternatives. A negative voltage in the back-gate biasing (V_{BG}) improves RT while WAT is not affected.

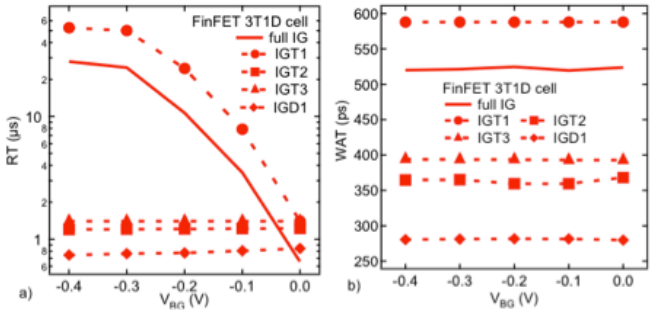

Fig. 4. RT for several IG configurations under back-gate biasing.

B. Variability impact analysis of IG eDRAMs

Comparing IG with SG-FinFET and bulk planar CMOS devices, the bulk CMOS-based has the highest RAT and WAT. On the other side, the SG is the fastest alternative but with the smallest RAT. Table 2 shows the effect of process variability for key metrics (WAT, RAT, Write Power –WP; and RT). Again, the IG alternative exhibits lower performance fluctuation against variability.

Table 2: Process variability impact (in %) on 3T1D

(%)	IGT1-FinFET		SG-FinFET		Bulk Planar	
	Mod	High	Mod	High	Mod	High
WAT	1.7	3.6	1.8	4.6	1.6	5.8
RAT	0.8	2.1	0.8	2.2	4.5	12.1
WP	0.2	0.4	0.4	0.5	0.8	2.6
RT	13.4	31.2	22.1	67.1	19.1	39.9

C. Variability impact on Yield

Fig. 5 depicts yield simulations for (a) 3T1D single cell and (b) a 2 kB memory block, when 3T1D-DRAM cells are based on IGT1, SG or bulk planar devices, where all the cells are subject to a high variation scenario. Fig. 5a shows the manufacturing yield for a 2 kB cache memory block with a reconfigurable array of 32 cells per column, 512 columns and 24 redundant columns. To compute yield, any cell with a retention time lower than 714 ns is defective. Fig. 5a shows that, at cell level, more than a 90% of yield is achieved for all cell configurations, while in the case of the memory block (Fig. 5b) only the IG reaches the 90% yield.

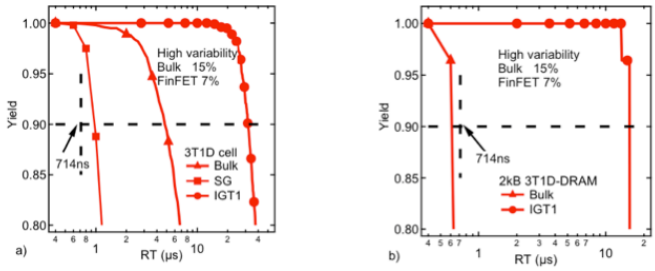

Fig. 5. Yield versus RT for different IG and SG FinFETs and planar bulk technologies, a) single cell, b) 2kB memory block.

IV. Degradation Effect on Gain-Cells in Technologies Below 10 nm

In this section, we will characterize the behavior of eDRAM cells on a 7 nm technology in front of degradation caused by aging. Together with variability (previous section), aging is one the key reliability issues. Next, we evaluate the effect of NBTI on the p-type devices of the cell. We simulate it by shifting the V_T from 0 to 100 mV (Fig. 6). This stress level can be accomplished for large hold periods when data is retained in the D node. Fig. 6 shows the influence of aging on RT, RAT and WAT.

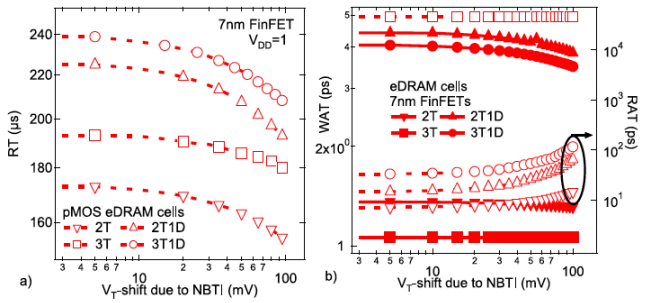

Fig. 6. Degradation of RT, WAT and RAT for different cells due to device aging, simulated by a V_T-shift.

The results show a larger variation for the two gated-diode cells (15%) and a smaller one for the other two (8%). Additionally, Fig. 6b shows that aging also increases the eDRAM cells' read access time, and, consequently, that it reduces eDRAM cells' corresponding working frequency.

V. Gain Cells at Sub-threshold Voltage Domain

In this section, we evaluate the behavior of eDRAM cells in sub-threshold domain (sub-V_T), this means for V_{DD} from 0.16 to 0.3 V – a very interesting domain for IoT where 6T SRAM have no space.

A. Performance's impact of low V_{DD}.

Fig. 7 shows the RT behavior for the specified margin of voltages. We compare 2T and 3T1D cells mixed and nMOS only. Although the mixed-based 3T1D and 2T have a similar evolution in terms of RT with V_{DD}, the gated-diode gain cell (3T1D) yields higher RT values (65% higher). When the nMOS-only 3T1D eDRAM cells are then compared to the mixed ones, the latter has significantly higher RT values (20x). Consequently, the mixed 3T1D cell is a very promising cell.

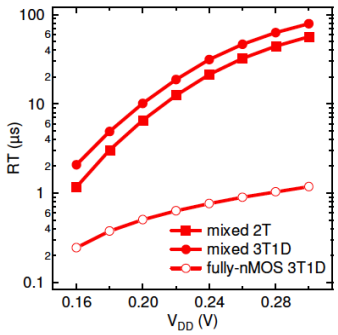

Fig. 7. RT for different gain-cells at low voltage levels.

We can evaluate the design space by resizing the cell devices in order to improve RT. We consider the following resizing strategies: 2W, 2L, 2WL, mWL. In particular, when only the W or L is increased, a different RT trend is observed in the analyzed V_{DD} range (0.16 – 0.3 V). While the 2L cell has a better RT (2x) at the ultra-low V_{DD} level (0.16 - 0.24 V), beyond that point, the RT values tend to be similar to those of the nominal cell. In contrast, the opposite behavior is observed for the 2W cell: although the RT is initially almost the same as the nominal proposal, it improves (2x) as the V_{DD} increases. It is worth noting that the RT cross-point is observed around 0.25 V, close to the threshold voltage of the 10 nm p-FinFET devices used in this study for the write access transistor (Fig. 4b). For the 2WL cell, the RT showed a uniform increase (2x) as compared to the nominal cell for the entire V_{DD} range. Finally, the largest increase in RT (3.5x) is obtained with the mWL proposal. This improved performance of the asymmetrically upsized (mWL) 3T1D-eDRAM cell can be explained by the larger sub-threshold slope values and lower I_{off} as L increases in the write access p-FinFET.

Fig. 8a shows the working frequency for different 3T1D-eDRAM cell proposals (nominal, 2W, and mWL). The largest values correspond to the 2W configuration, due to the larger drive current resulting from the cell devices' doubled W. In contrast, the mWL proposal has the lowest frequency value, although it is still within the usual operational range (> 100MHz) of sub-V_T memory circuits. Note that these values are obtained by analyzing the performance of a single gain-cell memory. The memory block is considered in the next section.

B. RT and Yield for 3T1D at 0.2 V

Following the same yield evaluation criteria than in previous section, we evaluate the impact on the 714 ns rule and the 2kB reconfigurable memory block with a V_{DD}=0.2V. Fig. 9 shows the results for the yield of the memory block with the different resizing alternatives we mentioned above. At 25ºC all the alternatives achieved a 99% of yield, at 75ºC only the mWL arrive to this yield achievement while no one verifies it for 100ºC, temperature affects significantly the retention time. Even at high temperature 3T1D (mWL) manifest a reasonable RT and good yield.

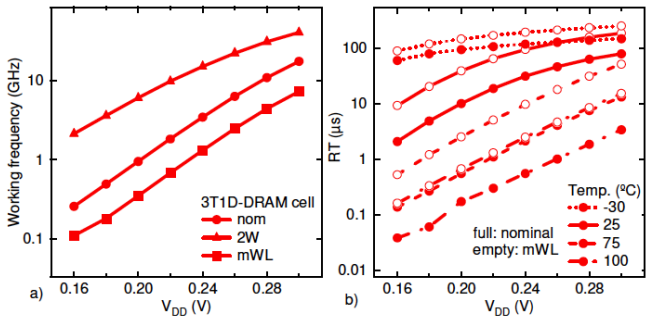

Fig. 8. Evolution of the working frequency and RT for different 3T1D-eDRAM configurations at low voltage levels.

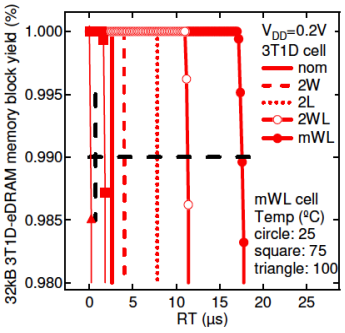

Fig. 9. RT and yield for different 3T1Ds with V_{DD} at 0.2 V.

VI. Conclusions

eDRAMs gain-cells manifest a tolerable impact on performance when affected by aging and process variability. This type of cells is not affected by the dramatic impact of aging and variability that affects static 6T cells dropping its SNM and causing faults. Several eDRAM gain-cells have been analyzed and compared under process variations and aging. To conclude, even with a negative effect on performance, they show a higher robustness when compared to SRAMs and they stand as a solid alternative to be considered in future advanced technologies.

Acknowledgments

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