A 2.4 GHz CMOS Class-F Power Amplifier With Reconfigurable Load-Impedance Matching

Mitra Gilasgar, Antoni Barlabé, Member, IEEE, and Lluís Pradell, Member, IEEE

Abstract—A novel reconfigurable CMOS class-F power amplifier (PA) at 2.4 GHz is proposed in this paper. It is able to match the output load variations mainly due to the effect of hand and head on a mobile phone. The effect of load variation on PAE, output power and distortion is compensated by reconfiguring the output network using an impedance tuner. The tuner controls the output matching at fundamental frequency without affecting the class-F harmonic tuning, up to $3^{rd}$ harmonic. To the authors' knowledge, this is the first design of a CMOS class-F PA addressed to compensate the effect of load variation. Measurement results for 50 Ω load impedance show a maximum PAE of 26%, and maximum output power of 19.2 dBm. The measured total harmonic distortion is 4.9%. Measurement results for load values other than 50 Ω show that PAE increases from 6.5% (not-tuned PA) up to 19.9% (tuned PA) with the same output power (19.2 dBm). Tuning also reduces the ACLR by 5 dB and the spectral regrowth of a WiFi signal at the PA output. The size of the fabricated chip is 1.6 mm × 1.6 mm.

Index Terms—Reconfigurable, class-F, power amplifier (PA), CMOS, impedance tuner

I. INTRODUCTION

Power amplifiers (PAs) are critical blocks in wireless communication systems because of their high power consumption. The demand for longer battery lifetime, smaller size and lower cost brings a great need for PAs to be highly efficient and integrated with other devices in a single chip [1]. The PA is the most difficult block to implement in CMOS [2] due to the low breakdown voltage, the conductive substrate, and the sheet-resistance of the poly silicon that limit the output power and efficiency.

Switching PAs [3] such as class-E [4]–[6] and class-F [7]–[10], have a minimum overlap between drain voltage and current waveforms, resulting in low power consumption and high efficiency. Although the class-E load network (consisting of one resonator) is simpler than class-F (consisting of multiple resonators), the voltage swing on the drain of a class-E PA can reach up to 3.6 times the drain bias voltage $V_{DD}$, while only 2 times $V_{DD}$ is possible for a class-F PA. Therefore, for the implementation on low breakdown technologies such as CMOS, a class-F PA is more suitable. A few fully integrated class-F PAs in CMOS have been reported [11]–[14]. To overcome the CMOS substrate limitation [15], low-loss matching networks using off-chip components have been proposed [16]–[19]. Furthermore, techniques such as power combining [14], [20] and stacked transistors [21] are used to increase the output power.

In wireless communications networks it is desired that RF front ends and consequently PAs could adapt to different conditions such as change in bias, frequency, load impedance or power. Load impedance variation happens when a user holds the mobile phone and the strong interaction between head, hand and antenna causes a change in antenna impedance [22], [23] leading to a reduced performance. In [24], a not-integrated tunable output matching network (OMN) for reconfigurable RF frontends is presented which includes harmonic tuning. Some other topologies for adaptive impedance tuners are presented in [25], [26].

Recent RF PAs with reconfigurable impedance tuning networks are aimed for multi-band operation [13], [20], [27], [28]. Other works are aimed for output power control using on-chip power combiners [29], bondwires and switched capacitors [30], or a combination of an adaptive power supply and impedance tuning using varactor diodes [31]. Techniques for adaptive control of impedance matching networks which provide automatic compensation of antenna mismatch are presented in [32]. In [33], a dynamic load trajectory manipulation technique is presented to enhance the efficiency of a CMOS Class-G PA, but with fixed load (antenna) impedance. In [34], a reconfigurable Doherty PA with transformer-based networks is presented which provides robust PA operation against load mismatches up to 2:1 VSWR. Among all the reported CMOS PAs only [13], [14] are reconfigurable class-F PAs, however the reconfiguration is not in load impedance but in frequency [13] or output power [14].

In this paper a novel reconfigurable CMOS class-F PA working at 2.4 GHz is proposed which can match different load impedance values. The effect of PA load variation on power-added efficiency (PAE), output power and distortion is...
compensated by reconfiguring the output network using an impedance tuner which includes two MOS variable capacitors. The tuner controls the output matching at fundamental frequency without affecting the class-F harmonic tuning up to 3rd harmonic.

II. PROPOSED RECONFIGURABLE CLASS-F PA DESIGN

A. Load-pull analysis

In an ideal class-F PA, the load impedance seen by the transistor should be a short circuit at even harmonics and an open circuit at odd harmonics. In a real PA, the active device is not an ideal switch, and therefore the optimum load impedances at harmonic frequencies are not short or open circuits. The load impedance values at the output of transistor at fundamental and harmonic frequencies which give highest power-added efficiency (PAE) or highest output power or a tradeoff between them can be derived from a load-pull analysis using the nonlinear model of the transistor. The active device in this design is a 3.3 V thick oxide 0.18 µm NMOS transistor available in TSMC™ CMOS technology. The transistor size is 64 × 8 µm (64 fingers with a length of 8 µm each). The output power and PAE contours of this device obtained from load-pull at fundamental frequency (2.4 GHz) are shown in Fig. 1(a). It shows that a maximum PAE of 30.1% can be achieved for a load impedance Z_L1 = 42 + j21.6 Ω, which has been selected for the PA design. The same procedure is done for 2nd harmonic (Fig. 1(b)) and 3rd harmonic (Fig. 1(c)). To reduce distortion (harmonic content at the amplifier output), harmonic loads near to those of an ideal class-F operation were chosen, even though (from Fig. 1(b)) the 2nd harmonic load does not show optimal PAE/output power. With the above criteria, the selected load impedance values are Z_L2 = 2.5 – j3.7 Ω and Z_L3 = 11.3 + j53 Ω, respectively. The 3rd harmonic load is shifted from an ideal open circuit due to the transistor drain capacitance. This way a class-F operation is guaranteed providing a trade-off between PAE, output power and distortion. The OMN proposed in Section II.B (Fig. 2) is designed to give these impedances at the desired frequencies.

From Fig. 1(c) it is apparent that PAE and output power are much insensitive to the impedance at 3rd harmonic and therefore (as studied in detail in Section II.C) to variations of this impedance produced by the reconfigurable OMN and different amplifier load impedances. The above calculations take into account loss in the matching networks. The effect of loss in the PA performance is further analyzed in Sections II.C and III.

B. Output matching network

The proposed OMN to achieve class-F operation using lumped elements is shown in Fig. 2(a). It consists of a harmonics filter and a CLC pi-shaped matching network at fundamental frequency (f_0) with variable capacitors (tuner).

The harmonics filter should provide an open circuit for odd harmonics and a short circuit for even harmonics in an ideal class-F operation. In that case, the parallel inductance L_d and a series capacitor C_s are not required and, since in our design the operation is limited to the 2nd and 3rd harmonics, the series LC resonator built by L_2 and C_2 resonates at 2f_0, providing a short circuit to the 2nd harmonic. The resonator L_3C_3 provides an open circuit at 3f_0. At frequencies well below its respective resonant frequency, resonator L_2C_2 behaves as a capacitor, and resonator L_3C_3 behaves as an inductor, giving a low pass filter that will have a small influence on the matching network behavior.

In a realistic class-F operation, since the optimum load impedances at harmonics are not short or open circuits but the values obtained previously from load-pull analysis (Section II.A), the harmonics filter is modified by adding the parallel inductance L_d and the series capacitor C_s. In that case, the equivalent circuit at 2f_0 is shown in Fig. 2(b). It can be observed that the filter for the 2nd harmonic is uncoupled from the matching network, thus adjusting the variable capacitors will not have any effect on the 2nd harmonic load. At 3f_0, the equivalent circuit is presented in Fig. 2(c), which is also uncoupled from the matching network section.
The design process begins by choosing appropriate values for the resonator components (L₂, C₂ and L₃, C₃). Considering their respective resonance frequencies the values of the products L₂C₂ and L₃C₃ are obtained. Inductors are chosen so as to minimize the chip area with optimum Q factor. Then the capacitor values are fixed. Values of C₁ and L₀ are obtained from analysis of the circuit in Fig. 2(b) and 2(c) by solving

\[ aC₁^2 + bC₁ + c = 0 \]
\[ L₀ = \frac{X₂}{4X₂ω₀C₁ + 2ω₀} \]

where
\[ a = 5ω₀X₂X₃ \]
\[ b = \left(5ω₀X₂X₃C₂ - \frac{15}{4}X₂ + \frac{5}{2}X₃\right) \]
\[ c = 3X₂C₂ - 2X₃C₂ \]

being X₂ and X₃ the transistor optimum load reactances at 2nd and 3rd harmonic respectively obtained previously by load-pull analysis, and ω₀ the fundamental angular frequency. In the above derivation, the circuit elements are considered lossless, and therefore only the imaginary part of Z₄,2 and Z₄,3 is taken into account. In this design the following values were chosen for the resonator elements: C₂ = 7 pF, L₂ = 0.06 nH, C₃ = 0.6 pF, L₃ = 0.8 nH. The values of C₁ and L₀ obtained using (1) are C₁ = 9 pF, L₀ = 2.3 nH.

![Harmonics Filter](image1)
![Matching Network](image2)

Fig. 2. (a) Proposed output matching network for the Class-F PA using lumped elements. (b) Equivalent circuit at 2f₀. (c) Equivalent circuit at 3f₀.

Next step is the design of the pi-shaped matching network (tuner) at fundamental frequency (elements C₀₁, L₀ and C₀₂ in Fig. 2). With such a circuit topology any arbitrary load impedance can be transformed into the optimal transistor load impedance at fundamental frequency (Z₄,1). To calculate C₀₁, L₀ and C₀₂, the input impedance at fundamental (Z₄,1 in Fig. 2(a)) is first calculated from the required transistor load impedance Z₄,1 = 42 + j21.6 Ω, by taking into account the effect of the harmonics filter elements. Next, the real and imaginary part of the normalized input admittance \( Y_{L1} = \frac{1}{Z_{L1}} \) are expressed as

\[
\text{Re}\left(Y_{L1}\right) = \frac{1 + \bar{X}(\bar{B}_1 - \bar{B}_2)}{(1 - \bar{X}B_2)^2 + \bar{X}^2} \\
\text{Im}\left(Y_{L1}\right) = \frac{\bar{B}_1(1 - \bar{X}B_2) - \bar{X}}{(1 - \bar{X}B_2)^2 + \bar{X}^2}
\]

where \( \bar{X} = j\omega L₀ \), \( \bar{B}_1 = j\omega C₀₁ \), \( \bar{B}_2 = j\omega C₀₂ \). By assuming a convenient value for L₀ (L₀ = 3 nH), the system in (2) can be solved for C₀₁ and C₀₂ obtaining C₀₁ = 1.38 pF and C₀₂ = 0.58 pF. The matching network is implemented as shown in Fig. 3. C_var1 and C_var2 are MOS varactors that use the gate capacitance of a MOS transistor and their capacitance value can be controlled by applying a voltage at the gate of it (V_ctl1, V_ctl2). Fixed capacitors, C_p1 and C_p2, must be connected in series before the variable capacitor in order to block the gate DC voltage, preventing it from going to the output of the PA. Another advantage of using two capacitors in series is that the peak voltage at the drain gets divided by two (approximately), hence minimizing the risk of breakdown. In this design the chosen values for C_p1, C_p2 are 10 pF and 6.1 pF respectively, and the varactor capacitance range is 1.1 pF–2.4 pF for C_var1 and 0.54 pF–1.1 pF for C_var2. These selections are justified by the simulations performed in Section II.C. As shown in the simulated results of Fig. 4 and 5, the selected varactor ranges are appropriate to cover a region in the Smith Chart of amplifier load impedances (antenna) with reflection coefficient magnitude up to 0.5, which are transformed in a circle close to the optimal transistor load impedance at fundamental frequency (with PAE > 27%). The particular varactor values C_var1 = 1.6 pF and C_var2 = 0.64 pF, combined with C_p1 and C_p2, produce C₀₁ = 1.38 pF and C₀₂ = 0.58 pF, as required in the nominal case of a 50 Ω (antenna) load discussed above.

![Matching Network](image3)

Fig. 3. Implementation of the matching network of Fig. 2(a) at fundamental frequency, using a series connection of capacitor and MOS varactor.

C. Impedance reconfiguration

The operation of the OMN to compensate the effect of load variation on the performance of the PA is demonstrated in Fig. 4, in which the simulated OMN input impedances for the full range of varactor capacitances C_var1 and C_var2 are plotted on a
Smith Chart at fundamental frequency, 2\(^{nd}\) and 3\(^{rd}\) harmonics. All the OMN circuit elements shown in Fig. 2, namely the CLC pi-network at fundamental (tuner), \(L_2C_2\) resonator at 2\(^{nd}\) harmonic, \(L_3C_3\) resonator at 3\(^{rd}\) harmonic, inductance \(L_d\) and capacitance \(C_e\) are included in the simulation. Therefore any effect caused by the harmonic circuit elements is taken into account at fundamental frequency, and also the effect of variation of capacitances \(C_{var1}\) and \(C_{var2}\) are included in the simulation at harmonic frequencies. Different amplifier load impedances with increasing reflection coefficient magnitude have been considered. As a first case Fig. 4(a)–(b) show the simulated OMN input impedance for a nominal load impedance \((Z_{4A} = 50\ \Omega)\). In Fig. 4(a) the OMN circuit elements are ideal (lossless). In Fig. 4(b) lossy elements are considered, with quality factors \(Q_L = 12\) for inductors and \(Q_C = 20\) for capacitors (including MOS varactors), which are commonly used in CMOS technology.

From inspection of Fig. 4(a)–(b) the following conclusions of the OMN operation for nominal amplifier load impedance are extracted:

- The OMN input impedance range at fundamental frequency includes the optimal value \((Z_{4A} = 42 + j21.6\ \Omega)\) from load-pull simulations. Specifically, this is achieved for \(C_{var1} = 1.6\ \text{pF}\) and \(C_{var2} = 0.64\ \text{pF}\), within the capacitance variation range. Moreover, as it can be observed comparing with the PAE contours of Fig. 1(a), most OMN input impedance values fall inside a circle featuring good amplifier performance with PAE > 27% and \(P_{out} > 17\ \text{dBm}\). Therefore possible inaccuracies in setting the varactor voltages (thus capacitances) have a little impact in the amplifier performance.

- The OMN input impedance at 2\(^{nd}\) harmonic is independent of the varactor capacitance variation, and therefore the 2\(^{nd}\) harmonic is decoupled from tuning at fundamental frequency. Regarding the 3\(^{rd}\) harmonic, the imaginary part changes with varactor capacitance, though the variation range is small (from \(j49\ \Omega\) to \(j63\ \Omega\)), with a negligible impact on PAE and output power as it can be observed in Fig. 1(c).

- Loss in the circuit elements (including MOS varactors) has a small effect in the input impedance distribution at fundamental frequency. In particular, comparing Fig. 4(a) to Fig. 4(b), a maximum phase rotation of 20\(^{\circ}\) and a reduction of 0.06 in the reflection coefficient magnitude are observed, but always keeping the optimal impedance value within the range of varactor capacitances. The effect of losses is more apparent on impedances at the 2\(^{nd}\) and 3\(^{rd}\) harmonic, featuring a reflection coefficient magnitude of 0.85 (2\(^{nd}\) harmonic) and 0.69 (3\(^{rd}\) harmonic), but the PAE and output power are unaffected.

The OMN input impedance has been simulated for load impedances \(Z_{4A}\) with a reflection coefficient \(\Gamma_{4A} = |\Gamma_{4A}|e^{j\phi_{4A}}\) of increasing magnitude \((0 \leq |\Gamma_{4A}| \leq 0.5)\) and full phase range \((-180^\circ \leq \phi_{4A} \leq 180^\circ)\), simultaneously sweeping the varactor capacitances \(C_{var1}\) and \(C_{var2}\) in their full capacitance range. All
circuit elements are considered lossy, with same quality factor as in the previous 50 Ω simulation. Fig. 4(c)–(d) show the results for the particular cases $|\Gamma_{LA}| = 0.3$ and $|\Gamma_{LA}| = 0.5$ and full range of phase $\phi_{LA}$ with an increment of 45°, in a zoomed Smith chart. Every simulated OMN input impedance set for a given phase $\phi_{LA}$ consists of a “matrix” of dots corresponding to the different $C_{var1}$ and $C_{var2}$ values. A constant PAE circle around the optimal OMN input impedance at fundamental frequency is also drawn, in order to assess which load impedances will be transformed into OMN input impedances yielding PAE > 27% and $P_{out} > 17$ dBm, which are only slightly smaller (3% and 0.5 dB, respectively) than the optimal results. It can be observed that any impedance $Z_{LA}$ with $|\Gamma_{LA}| \leq 0.3$ is transformed within the 27% PAE circle for some value of the varactor capacitances. Impedances with $0.3 \leq |\Gamma_{LA}| \leq 0.5$ are also transformed within the circle but with limited phase range. In the limit ($|\Gamma_{LA}| = 0.5$), the allowed phase range is $-180° \leq \phi_{LA} \leq -125°$ and $33° \leq \phi_{LA} \leq 75°$. Higher reflection coefficient values ($|\Gamma_{LA}| > 0.5$) are transformed outside, but surrounding the circle. Therefore though the theoretical PAE and output power will be smaller than 27% and 17 dBm, respectively, the OMN will still be compensating the varying load impedance to achieve the best possible amplifier performance. The 2nd and 3rd harmonic impedances are insensitive to load impedance variations. Although not shown in the zoomed view of Fig. 4(c)–(d), the harmonic impedances follow the same pattern as in Fig. 4(a)–(b). The black area in Fig. 5(a) depicts the load impedance region that will be transformed within the constant PAE circle, which agrees with the perturbed region for mobile phones reported in the literature [22], [23]. The necessary capacitances $C_{var1}$ and $C_{var2}$ to cover this area can then be mapped into varactor actuation voltages, $V_{ctl1}$ and $V_{ctl2}$, respectively, which range is -3.3 V to +3.3 V. Fig. 5(b) shows the varactor actuation voltages as a function of the load reflection coefficient magnitude ($|\Gamma_{LA}|$) and phase ($\phi_{LA}$). It can be observed that the required control voltages mainly depend on the phase.

D. Power Amplifier Implementation

Using the reconfigurable output matching structure proposed in Section II.B, the final reconfigurable CMOS class-F PA configuration is shown in Fig. 6. A cascode structure has been selected that permits higher bias voltages without damaging the transistors. The input matching network is composed of a series inductor $L_1$ ($L_2 = 4.6$ nH) and a parallel capacitor $C_1$ ($C_2 = 0.61$ pF) to match the power device to 50 Ω input impedance for a high power transfer. MOS varactors in the OMN and inductors are critical in terms of loss. In Section III the PA performance degradation due to these losses is simulated and compared to measurements. A picture of the fabricated chip is shown in Fig. 7 in which the pads for RF signal, and CMOS transistor and MOS varactor DC-bias are apparent.

III. SIMULATION AND MEASUREMENT RESULTS

Simulations are performed with Keysight ADS and Cadence Spectre RF software packages considering the circuit of Fig. 6. The nominal bias point is $V_{DD} = 3$ V, $V_{GG} = 1.3$ V, with DC drain current ranging from 44 mA to 63 mA for input powers from -10 dBm to +15 dBm, respectively.

A. 50 Ω load

In a first case a nominal load (antenna) impedance $Z_{LA} = 50$ Ω (impedance $Z_{LA0}$ at the center of Smith Chart in Fig. 5(a)) is considered and the MOS varactors are fixed to their nominal values $C_{var1} = 1.6$ pF and $C_{var2} = 0.64$ pF. Fig. 8 compares the simulated $P_{out}$ and PAE vs. $P_{in}$ under three assumptions: (i) ideal (lossless) elements in matching networks; (ii) lossy inductors but ideal capacitors; (iii) lossy inductors and lossy capacitors (including MOS varactors). In cases (ii) and (iii)
complex foundry models which take into account loss and couplings are used for the inductors and capacitors. The maximum \( P_{\text{out}} \) is 21.1 dBm, 19.4 dBm and 18.7 dBm and the optimal PAE is 57%, 34% and 28.9%, for cases (i), (ii) and (iii), respectively. These results agree with the predictions from load-pull analysis in Fig. 1(a). In case (iii) the \(-1\) dB compression point is \( P_{\text{out,1dB}} = 14.5 \) dBm, and for optimal PAE, \( G_p = 10.2 \) dB, \( P_{\text{in}} = 8 \) dBm. It can be observed that the inductor loss is a main limitation for \( P_{\text{out}} \) and PAE, whereas loss associated to capacitors has a smaller contribution. The simulated drain voltage and current waveforms of the PA for different input powers are shown in Fig. 9. It can be observed that in order to achieve a proper class-F voltage and current waveforms, a high input drive bigger than 2 dBm is required.

Using a measurement setup consisting in a wafer-probe station connected to a network analyzer, the results of Figs. 10 to 12 have been obtained. Fig. 10 compares the measured and simulated large signal S-parameters of the fabricated PA chip, showing a good agreement. For an input power of 5 dBm the

![Fig. 6. Proposed reconfigurable class-F PA.](image)

![Fig. 7. Fabricated PA chip in TSMC\(^\text{TM}\) 0.18 \(\mu\)m CMOS technology. Die size is 1.6 mm \(\times\) 1.6 mm.](image)

![Fig. 8. Simulated PA behavior for V\(_{\text{DD}}\) = 3V. (a) Output power. (b) PAE.](image)

![Fig. 9. Simulated drain voltage and current waveforms of the proposed class-F PA for different input powers (-5 dBm, 0 dBm, 5 dBm, 7 dBm, 10 dBm).](image)
measured gain is 11.5 dB and the simulated gain is 12.3 dB at 2.4 GHz. The PA performance regarding PAE and $G_p$ are measured versus output power and compared to simulations in Fig. 11 and Fig. 12. Besides the nominal bias point a higher bias voltage ($V_{DD} = 4$ V, $V_{GG} = 1.5$ V) has also been used in measurements. For $V_{DD} = 3$ V, a maximum measured PAE of 22% for $P_{out} = 16.8$ dBm with $G_p = 7.9$ dB is obtained. For $V_{DD} = 4$ V, the maximum measured PAE increases to 26.5% for $P_{out} = 18.7$ dBm with $G_p = 9.7$ dB, and a maximum output power of 19.2 dBm is obtained with a PAE of 20%, being the measured $-1$ dB compression point $P_{out,1dB} = 15.8$ dBm. The measured OIP3 and IIP3 are 23.4 dBm and 12.2 dBm, respectively. In both cases the measured output power is shifted down 2 dB with respect to the simulated output power. This difference is mainly attributed to the quality factor of fabricated inductors and capacitors (including MOS varactors) which may have been overestimated in simulation. If, for instance, slightly smaller values ($Q_L = 8$ and $Q_C = 15$) were considered, then $G_p$ decreases by 1.5 dB.

For nonlinear measurements a CW/digitally-modulated RF generator is connected to the input of the wafer-probe station and a spectrum analyzer/vector signal analyzer to its output. A directional coupler is inserted between the wafer-probe station output and the spectrum analyzer in order to obtain an accurate measurement of the output power using its coupled port. To this end, the loss produced by the directional coupler and connection cable is characterized prior to the measurement. The simulation and measurement results of the output spectrum are shown in Fig. 13. The measured harmonic rejection for 2$^{nd}$ and 3$^{rd}$ harmonics are 28 dBc and 32.6 dBc respectively. The output spectrum shows a high harmonic suppression up to 5$^{th}$ harmonic which shows that the proposed topology has the ability to reject harmonics without an extra filtering section. The measured total harmonic distortion (THD) is 4.9%.

To assess the PA nonlinear behavior under real operating conditions, adjacent-channel leakage ratio (ACLR) measurements have been performed using IEEE 802.11g WiFi signals (OFDM–64 QAM with maximum data rate of 54 Mb/s and PAPR = 9 dB) delivered to the PA input. Fig. 14 shows the measured spectrum regrowth at the output of the amplifier for $P_{out} = +2$ dBm and $P_{out} = +18.7$ dBm. The latter
corresponds to maximum PAE. The bias condition is $V_{DD} = 4$ V. It can be observed that the PA meets WiFi mask specifications (trace below blue limit line) for $P_{out} \leq 18$ dBm. The measured ACLR values (in dBc) at 2.412 GHz (WiFi channel #1) for different output powers are presented in Table I. As expected, ACLR degrades with increasing $P_{out}$, but even at highest $P_{max}$ levels (with optimum PAE) ACLR is better than $-26.6$ dBc. Fig. 15 shows the measured EVM (%) of a WiFi IEEE 802.11g OFDM–64 QAM signal with maximum data rate of 54 Mb/s. For $P_{out} \leq 7$ dBm the PA features an EVM $\leq 1.3$%. For $P_{out} \leq 13$ dBm the PA features an EVM $\leq 5.6$%, which allows the maximum specified data rate (54 Mb/s). For $P_{out} = 18$ dBm, the EVM is 14.4%, which allows a maximum data rate of 24 Mb/s. The above results mean the PA must operate at $5.7$ dB back-off to meet the EVM specifications at maximum data rate (54 Mb/s). Back-off is evaluated as the maximum output power for maximum PAE (18.7 dBm) minus the output power to meet the EVM specifications (13 dBm).

**TABLE I**

<table>
<thead>
<tr>
<th>Load impedance ($\Omega$)</th>
<th>$P_{out}$ = 12 dBm</th>
<th>$P_{out}$ = 16 dBm</th>
<th>$P_{out}$ = 18 dBm (highest PAE)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Not tuned</td>
<td>Tuned</td>
<td>Not tuned</td>
</tr>
<tr>
<td>50$^*$ (L)</td>
<td>-38.2</td>
<td>-30.3</td>
<td>-26.6</td>
</tr>
<tr>
<td>50$^*$ (U)</td>
<td>-39.9</td>
<td>-31.4</td>
<td>-26.9</td>
</tr>
<tr>
<td>19.9–j7.1 (L)</td>
<td>-35</td>
<td>-26.3</td>
<td>-23.3</td>
</tr>
<tr>
<td>19.9–j7.1 (U)</td>
<td>-39.7</td>
<td>-31.2</td>
<td>-25</td>
</tr>
<tr>
<td>145.5–j18.5 (L)</td>
<td>-37.8</td>
<td>-28.3</td>
<td>-25.5</td>
</tr>
<tr>
<td>145.5–j18.5 (U)</td>
<td>-38.3</td>
<td>-29.9</td>
<td>-25.5</td>
</tr>
</tbody>
</table>

* For a matched load (50 $\Omega$), $C_{var1}$ and $C_{var2}$ have nominal values
L: lower channel, U: upper channel.

**TABLE II**

<table>
<thead>
<tr>
<th>$Z_{L,i}$ ($\Omega$), (i = 0,1,...,8)</th>
<th>Not Tuned</th>
<th>Tuned var1</th>
<th>Tuned var1 and var2</th>
</tr>
</thead>
<tbody>
<tr>
<td>PAE (%)</td>
<td>$P_{out}$ (dBm)</td>
<td>PAE (%)</td>
<td>$P_{out}$ (dBm)</td>
</tr>
<tr>
<td>50$^*$</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>50$^*$</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>50$^*$</td>
<td>–</td>
<td>–</td>
<td>–</td>
</tr>
<tr>
<td>80.7 + j3.9</td>
<td>10</td>
<td>15.4</td>
<td>12</td>
</tr>
<tr>
<td>37.8 + j33.3</td>
<td>11</td>
<td>15.7</td>
<td>17.1</td>
</tr>
<tr>
<td>24.3 + j5.5</td>
<td>5</td>
<td>13.5</td>
<td>10.3</td>
</tr>
<tr>
<td>41.5 – j48</td>
<td>4.7</td>
<td>13.3</td>
<td>10.7</td>
</tr>
<tr>
<td>19.9 – j7.1</td>
<td>5.2</td>
<td>13.7</td>
<td>12.7</td>
</tr>
<tr>
<td>145.5 – j18.5</td>
<td>6.5</td>
<td>13.4</td>
<td>16.2</td>
</tr>
<tr>
<td>145.5 – j18.5</td>
<td>6.5</td>
<td>13.4</td>
<td>16.2</td>
</tr>
<tr>
<td>145.5 – j18.5</td>
<td>6.5</td>
<td>13.4</td>
<td>16.2</td>
</tr>
<tr>
<td>145.5 – j18.5</td>
<td>6.5</td>
<td>13.4</td>
<td>16.2</td>
</tr>
<tr>
<td>145.5 – j18.5</td>
<td>6.5</td>
<td>13.4</td>
<td>16.2</td>
</tr>
</tbody>
</table>

* For a matched load (50 $\Omega$), $C_{var1}$ and $C_{var2}$ have nominal values

The PA is first measured for each load impedance, without

\[ \text{Fig. 15. Measured EVM (%)} \text{ of a WiFi IEEE 802.11g signal produced by} \]

\[ \text{the PA with a matched 50 $\Omega$ (antenna) load (in a tuned case), and with a} \]

\[ \text{mismatched (antenna) load $Z_{L,\text{un}} = 145.5-j18.5$ $\Omega$ (not-tuned and tuned cases).} \]

**B. Mismatched loads**

In order to test the effect of antenna load ($Z_{L,A}$) variation, which can occur by the hand and head effect on the mobile phone [22], [23], the PA is measured with different mismatched loads and tuned. Using an output tuner, eight load impedances covering the theoretical load impedance region (black region in Fig. 5(a)), which is transformed within a circle of PAE = 27%, have been synthesized at 2.4 GHz. The tuner is composed of a 50 $\Omega$ coaxial sliding line to change the load (antenna) reflection coefficient phase, and a 25 $\Omega$ fixed line which can be combined with a fixed attenuator to change the load (antenna) reflection coefficient magnitude. The tuner is inserted between the power amplifier output and the network analyzer (or spectrum analyzer/vector signal analyzer). These mismatched impedances are plotted as superimposed black and white dots in Fig. 5(a) ($Z_{L,A1}$ to $Z_{L,A8}$) and listed in Table II.

![Fig. 14. Measured spectrum regrowth of a WiFi IEEE 802.11g signal produced by the PA with a matched 50 $\Omega$ load. (a) $P_{out} = +2$ dBm. (b) $P_{out} = +18.7$ dBm (corresponding to maximum PAE). The indicated absolute power levels are not actual PA output power because of the measurement setup couplers and attenuators.](image-url)
applying any voltage to the MOS varactors (C_{var1} and C_{var2} in Fig. 6). This case is referred as not-tuned performance. Then the MOS varactors are tuned manually by changing the DC voltage applied to their gate using the control voltages in the look-up table presented in Fig. 5(b) ranging from −3 V to 3 V. This case is referred to as tuned performance. Three tuning conditions are considered: not-tuned, tuned using only C_{var1} and tuned using both C_{var1} and C_{var2}. The performance of the PA regarding measured PAE and gain for four selected loads are shown in Fig. 16 and Fig. 17 respectively.

![Fig. 16: Measured PAE for different load impedances of (a) 80.7 + j3.9 Ω, (b) 37.8 + j33.3 Ω, (c) 41.5 − j48 Ω, and (d) 65.2 + j66.4 Ω compared in three different conditions of no tuning (dashed), one varactor (Var1) tuned (circle), and both varactors (Var1 and Var2) tuned (cross).](image)

![Fig. 17: Measured gain for the same impedances as in Fig. 16 compared in three different conditions of no tuning (dashed), one varactor (Var1) tuned (circle), and both varactors (Var1 and Var2) tuned (cross).](image)

![Fig. 18. Measured spectrum regrowth of a WiFi IEEE 802.11g signal produced by the PA for the mismatched load Z_{L65} = 145.5−j18.5 Ω. (a) Not-tuned state. (b) Tuned state with P_{out} = 16 dBm. The indicated absolute power levels are not actual PA output power because of the measurement setup couplers and attenuators.](image)

It can be observed that when using C_{var1} as tuning element the gain and output power increase around 1-2 dB, and when using both C_{var1} and C_{var2} as tuning elements a total gain and output power increase of 2 dB to 6 dB is achieved. In Fig. 17 it is observed that the gain for maximum PAE ranges from 8 to 9 dB, very close to the matched load case. The tuning results are also compared in Table II showing, for each load-impedance, a significant increase in PAE in the tuned condition with respect to not-tuned. For Z_{LA1}, Z_{LA2}, Z_{LA4}, Z_{LA6}, and Z_{LA8}, the tuned PAE is close to 19%, in contrast to very low values for not-tuned condition. The highest tuned PAE is 19.9% for Z_{LA6}, and the highest P_{out} is 19.2 dBm for Z_{LA6}, same as in the matched load condition. Z_{LA4} = 41.5 − j48 Ω, which is theoretically out of the load impedance region of Fig. 5(a), reaches a tuned PAE of 19.7%. This shows that the proposed circuit successfully compensates the effect of PA load variation. By tuning C_{var1} and C_{var2} varactors the nonlinear distortion is reduced with respect to not-tuned condition. As an example, Fig. 18 shows the measured spectrum regrowth for the mismatched load Z_{LA6} = 145.5 − j18.5 Ω before and after tuning. In the tuned state, the PA is delivering an output power P_{out} = 16 dBm. It can be observed that in tuned condition the spectrum regrowth is highly...
TABLE III
COMPARISON WITH OTHER SWITCHED-MODE CMOS POWER AMPLIFIERS

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Technology</th>
<th>Freq. (GHz)</th>
<th>Signal type</th>
<th>$V_{dd}$ (V)</th>
<th>$P_{out}$ (dBm)</th>
<th>PAE$_{max}$ (%)</th>
<th>Gain$_{max}$ (dB)</th>
<th>Distortion</th>
<th>Area, mm$^2$</th>
<th>Class</th>
<th>Reconfiguration</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5]</td>
<td>0.18 µm CMOS</td>
<td>5</td>
<td>Constant envelope</td>
<td>2</td>
<td>15.4</td>
<td>40.6</td>
<td>NA</td>
<td>NA</td>
<td>0.81</td>
<td>E</td>
<td>NO</td>
<td>Fully Integrated Injection-locking to increase PAE</td>
</tr>
<tr>
<td>[6]</td>
<td>90 nm CMOS</td>
<td>1.8</td>
<td>Constant envelope</td>
<td>2.5 - 1.5</td>
<td>24</td>
<td>12</td>
<td>NA</td>
<td>NA</td>
<td>3.69</td>
<td>E</td>
<td>Switched capacitor bank OMN</td>
<td>Fully Integrated Tuning for DC supply compensation</td>
</tr>
<tr>
<td>[4]</td>
<td>0.18 µm CMOS</td>
<td>2.4</td>
<td>Constant envelope</td>
<td>0.8</td>
<td>9</td>
<td>NA</td>
<td>19</td>
<td>NA</td>
<td>0.7</td>
<td>E</td>
<td>NO</td>
<td>Fully Integrated</td>
</tr>
<tr>
<td>[19]</td>
<td>0.18 µm CMOS</td>
<td>0.824 - 0.915</td>
<td>3G LTE (Variable envelope)</td>
<td>3.3</td>
<td>26.7</td>
<td>34.2</td>
<td>31.2</td>
<td>ACLR = -35.2 dBc</td>
<td>1.41</td>
<td>F</td>
<td>NO</td>
<td>OFF chip OMN and feedback</td>
</tr>
<tr>
<td>[13]</td>
<td>0.13 µm CMOS</td>
<td>0.7-1.2</td>
<td>Constant envelope</td>
<td>4.8</td>
<td>24.6 - 20.1</td>
<td>48.3 - 30</td>
<td>16.5 - 14.9</td>
<td>NA</td>
<td>2.25</td>
<td>F</td>
<td>Switched capacitor bank OMN</td>
<td>Fully Integrated Tuning for frequency adjustment</td>
</tr>
<tr>
<td>[14]</td>
<td>0.25 µm CMOS</td>
<td>1.4</td>
<td>Constant envelope</td>
<td>1.5</td>
<td>8.5 - 24.8</td>
<td>49</td>
<td>NA</td>
<td>NA</td>
<td>0.43</td>
<td>F</td>
<td>NO</td>
<td>Fully Integrated Parallel combination of 3 amplifiers</td>
</tr>
<tr>
<td>[11]</td>
<td>0.2 µm CMOS</td>
<td>900</td>
<td>Constant envelope</td>
<td>1.8 - 3</td>
<td>31.8</td>
<td>43</td>
<td>NA</td>
<td>NA</td>
<td>2.0</td>
<td>F</td>
<td>NO</td>
<td>Fully integrated</td>
</tr>
<tr>
<td>[16]</td>
<td>0.6 µm CMOS</td>
<td>1.9</td>
<td>Constant envelope</td>
<td>3</td>
<td>22.8</td>
<td>42</td>
<td>10.5</td>
<td>IIP3 = 19.5 dBm</td>
<td>N/A</td>
<td>F</td>
<td>NO</td>
<td>OFF chip OMN</td>
</tr>
<tr>
<td>[34]</td>
<td>65 nm CMOS</td>
<td>3.10 - 3.98</td>
<td>QPSK/16 QAM</td>
<td>3</td>
<td>27.3 (CW)</td>
<td>21.8</td>
<td>28.6</td>
<td>16.8</td>
<td>2.087</td>
<td>F</td>
<td>Active Doherty load modulation</td>
<td>Transformer-based parallel power combining</td>
</tr>
</tbody>
</table>

This work: 0.18 µm CMOS 2.4 WiFi QAM (Variable envelope) 3 - 4 19.2 26 11.5 ACLR = -29.8 dBc THD = 4.9 % 2.56 F MOS varactors OMN Fully integrated. Tuning for load (antenna) matching

Reduced, which is also confirmed by the ACLR data presented in Table I. For $Z_{L_A}$, the lower channel ACLR is reduced by 5 dB. A similar reduction can be observed for other mismatched loads. At highest $P_{out}$ levels (optimum PAE) it can be observed that ACLR is ~29.8 dBc, a better value than with matched output load. This results show that the OMN tuner is able to not only match the switch-mode PA to antenna variations but also improve distortion and back-off characteristics. Regarding the EVM, in Fig. 15 it can be observed that in a tuned condition under mismatched (antenna) load impedances, the EVM values improve up to 3% with respect to the not-tuned state, completely recovering the featured EVM levels in the 50 Ω load case.

Table III shows a comparison of the PA presented in this paper with other PAs in the bibliography. Most PAs are not reconfigurable. The proposed design exhibits a PAE which is smaller than in [13] (frequency-reconfigurable design) and in the not-reconfigurable designs of [11], [14], [16] and [19], but the center frequencies are substantially lower (1.2 GHz, 0.9 GHz, 1.2 GHz and 0.915 GHz respectively). Furthermore, in [14] bondwires are used to implement the required inductors, thus avoiding the loss associated to spiral inductors, and in [19] bondwires, SMD capacitors and SMD inductors are used. In [16], a partially off-chip output matching network is used (bondwire and SMD capacitor). The PAE of the Class-E power amplifier reported in [5] is 40.6% at 5 GHz, but it is using an injection-locking technique. Concerning the gain of the proposed power amplifier, it is similar to the amplifier reported in [16] (10.5 dB at 1.9 GHz) and in [13] (14.9 dB at the frequency 1.2 GHz, which is lower than 2.4 GHz). Compared to [4] and [19], it is smaller (19 dB at 2.4 GHz, and 31.2 dB at 0.915 GHz, respectively), but in [4] and [19] multistage designs are used. Concerning the area of the proposed power amplifier, it is smaller than that of [6], very similar to [13], and bigger than that of [11], [14] and [19], but the designs of [11], [14] and [19] are not reconfigurable. Among the reconfigurable designs, reconfiguration responds to different criteria (frequency band in [13] and DC power in [6]) than the load (antenna) variation criteria proposed in this paper. Only in [34] an efficiency enhancement is provided against antenna mismatch, but the allowed load mismatch (2:1 VSWR) is smaller than in the design proposed in this paper (3:1 VSWR, corresponding to $|\Gamma_{L_A}| = 0.5$). To the authors’ knowledge, the PA presented is the only integrated class-E PA aimed to continuous load variation adjustment at fundamental frequency (without affecting harmonic tuning) using MOS varactors, and has an excellent balance between output power, PAE and distortion.

The OMN tuner proposed in this paper could be automated in order not to require human intervention. This requires knowledge of the instantaneous (real time) value of the (antenna) load impedance, which in turn can be accomplished by adding elements for impedance-sensing and actuation of the MOS varactors in the OMN tuner shown in Fig. 6. A possible configuration of this system is shown in the block diagram of Fig. 19, which can be easily fabricated using commercially-available integrated circuits, and also it would be possible to integrate the full system in CMOS to obtain an on-chip solution. The system includes a directional coupler, two peak detectors, a phase comparator, and a digital microcontroller system which incorporates A/D and D/A blocks, a CPU, the stored look-up table values of Fig. 5(a), and a control algorithm. The directional coupler could be implemented using lumped elements [35] to save area. The

impedance detector consists of two peak detectors and a phase comparator, delivering a very-low frequency signal containing the amplitude and phase information of the incident and reflected waves, respectively. A possible CMOS vector-detector configuration is reported in [36]. A raw measurement of the (antenna) load reflection coefficient is obtained from the complex ratio between detected incident and reflected waves, 

\[ M = \frac{M_{\text{ref}}}{M_{\text{inc}}} \] 

In order to de-embed the actual antenna reflection coefficient \( \Gamma_{\text{inc}} = \frac{\Gamma_{\text{ref}}}{\Gamma_{\text{out}}} \) a mathematical correction is applied to \( M \), which takes into account the effect of the directional coupler and the loads of coupled ports (\( \Gamma_{\text{ref}} \) and \( \Gamma_{\text{out}} \) in Fig. 19). The digital control system compares the measured (corrected) antenna reflection coefficient values with the load values stored in a look-up table jointly with the actuation-voltages plotted in Fig. 5(b). Using an algorithm for estimation of minimum distance, the closest impedance value in the look-up table is selected, and the corresponding actuation voltages \( V_{\text{ctl1}} \) and \( V_{\text{ctl2}} \) are used to tune the varactors automatically. This procedure is repeated for any antenna reflection coefficient (which is time-varying due to hand and body effects). In this way the tuner could be controlled automatically in real time. The estimated overhead produced by a control system such as the one illustrated in Fig. 19 is low. Excluding the micro-controller it is less than 1% of the PA power consumption and around 15% of die area [37], including the microcontroller it would be around 2% of the PA power consumption.

### IV. Conclusion

In this work, a novel reconfigurable CMOS class-F power amplifier at 2.4 GHz with up to 3rd harmonic tuning has been presented. It is able to match load variations caused by hand and body effect on the antenna. The amplifier measurements for a nominal load impedance of 50 Ω show an optimal PAE of 26%, a THD of 4.9%, and ACLR of -26.9 dB while delivering an output power of 18.7 dBm. Load (antenna) variations are compensated by using an impedance tuner in the amplifier output matching network which integrates two RF MOS variable capacitors. The measured results for mismatched loads show that the impedance tuner is able to continuously tune load reflection coefficients with a magnitude up to 0.5 maintaining a tuned PAE better than 18.6%, in the phase range [-90°, -90°], with an output power higher than 17.5 dBm. The maximum tuned PAE and output power are 19.2 dBm and 19.9% respectively which coincides with the result in the matched output load condition. Also in the tuned condition the PA is able to compensate the nonlinear distortion. The measured lower channel ACLR for mismatched loads is reduced by 5 dB with respect to the not-tuned condition, reaching -29.8 dBc for an output power of 18 dBm (maximum PAE). Thus the proposed reconfigurable tuner circuit concept is validated, showing that it is able to successfully compensate the effect of load variation on the power amplifier performance.

### ACKNOWLEDGMENT

The authors wish to thank the HIPICS research group of UPC, for their support to access the 0.18 μm CMOS technology and Cadence Software and to the technical staff of Dept. TSC (UPC) in preparing the samples for measurement.

### REFERENCES


