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Compensation of Transient Beam Loading in Ramping Synchrotrons using a Fixed Frequency Processing Clock

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Abstract. Transient beam loading compensation schemes, such as One-Turn-FeedBack (OTFB), require beam synchronous processing (BSP). Swept clocks derived from the RF, and therefore harmonic to the revolution frequency, are widely used in CERN synchrotrons; this simplifies implementation with energy ramping, where the revolution frequency changes. It is however not optimal for state-of-the-art digital hardware that prefers fixed frequency clocks. An alternative to the swept clocking is the use of a deterministic protocol, for example White Rabbit (WR): a fixed reference clock can be extracted from its data stream, while enabling digital distribution of the RF frequency among other data. New algorithms must be developed for BSP using this fixed clock and the digital data transmitted on the WR link. This is the strategy adopted for the SPS Low Level RF (LLRF) upgrade. The paper gives an overview of the technical, technological and historical motivations for such a paradigm evolution. It lists the problems of fixed clock BSP, and presents an innovative solution based on a real-time variable ratio re-sampler for implementing an OTFB with the new fixed clock scheme.

1. Motivation

With particles travelling close to the speed of light, it is not possible to make a measurement on a given bunch passage, process the data and act on the same bunch in the same turn. Fortunately, action in the same turn is rarely needed: in the longitudinal plane, beam dynamics are governed by the synchrotron frequency that is typically orders of magnitude smaller than the revolution frequency. The longitudinal distribution does barely change from one turn to the next, and the processing can profit from a one (or few) turn(s) delay budget. This is the way OTFB [1] and Longitudinal Dampers work [2].

In the transverse plane, the betatron frequency is larger than the revolution frequency, but the betatron tune spread is typically much smaller than the revolution frequency. Transverse dampers LLRF includes the appropriate phase shift, so that it can measure on a given turn and act on the next turn [3]. Implementation of an exact one (or few) turn(s) delay is therefore essential to these LLRF systems. This is trivial with a digital implementation whose clock remains synchronous with the RF frequency, solution widely adopted since the first One-Turn-Delay Feedback implemented on the SPS by D. Boussard [4, 5, 6].



1.1. Classic OTFB implementation

The OTFB is a BSP RF feedback with gain on the revolution frequency harmonics, and an exact one-turn loop delay. The filter must track these harmonics during the acceleration, when the spacing between them increases proportionally to the revolution frequency. If the processing clock is an integer multiple M of the revolution frequency (M sampling periods equal one turn) the processing is very simple [1, 7], as given by transfer function (1), whose frequency response is represented in figure 1. The parameter a in (1) governs the bandwidth of the filter around each revolution frequency harmonic, and G is the gain of the filter.

$$H(z) = G \frac{1-a}{1-az^{-M}} z^{-M} \quad (1)$$

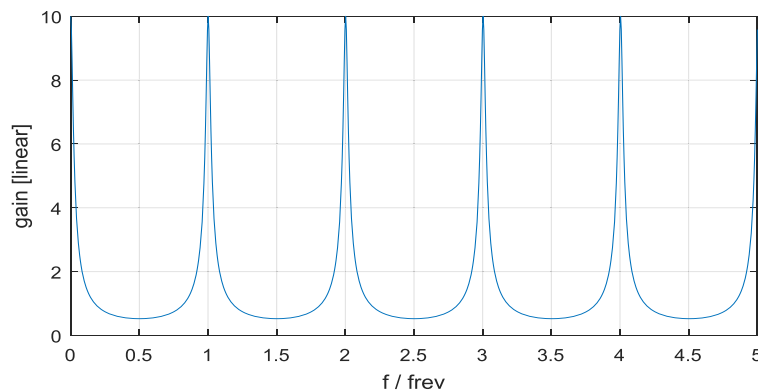


Figure 1. Frequency response of the classic OTFB filter.

2. RF and clock distribution

Many synchrotrons use a classic master-slave architecture for RF reference and clock/phase distribution and synchronization. The RF reference is generated in a Master Oscillator and distributed to all slave systems (cavities, injectors RF, beam instrumentation, kickers). The frequency changes during the acceleration ramp, together with the beam energy. If the digital clock is derived from this RF, it is trivial to keep the processing synchronous with the revolution frequency. This derived swept clock architecture is common at CERN since the mid-80s and can be found in LHC, SPS, PSB, PS and LEIR [8, 9].

This is not ideal however: part of the processing should not depend on the beam energy (for example correction to an amplifier or cavity frequency response when the cavity is not tuned). Furthermore, commercial electronics are not intended to be operated with varying clocks. Digital logic devices such as FPGAs, intensively used in LLRF, require stable clocks. The swept clock architecture has several other limitations:

- Beam transfer between machines requires periodic synchronization of their RF, resulting in abrupt phase and frequency transients that can result in synchronization errors in the FPGA [10].
- The spectral purity of the clock is essential for low RF noise. The use of Phase Locked Loops (PLLs) [11] to clean the clocks is not optimal when these are swept in frequency. PLLs are also present in almost any discrete processing digital device, for instance Digital Clock Managers in FPGAs. If the clock is swept, then the compatibility with new devices using PLLs is limited [12].

- Similarly, these modern devices use serial links for interconnection. A swept clock has a dramatic effect on the data alignment of these serial protocols.
- LLRF systems make intensive use of discrete processing architectures, based on synchronous digital logic design. Swept clocks complicate design synchronization and clock constraining.
- Fast or even abrupt modifications of the phase or frequency of the RF are needed in some non-adiabatic RF gymnastics (bucket merging at the end of slip stacking process for example). These will result in fast clock phase and frequency changes.

3. Paradigm change

A double paradigm change has been decided at CERN to cope with all these problems.

The RF reference will not be distributed as analog signal, but instead transmitted as a numerical word, using a Deterministic Link. This approach is used in other accelerators, BNL [13], GSI [14]. In Deterministic Links, the time of flight between emitter and receiver is known and reproducible. White Rabbit link (WR) has been selected as our protocol, a link developed and in use at CERN [15, 16]. This protocol is an extension to Gigabit Ethernet and Precision Time Protocol (PTP - IEEE 1588). With the enhancements, regardless of node location, an upper bound delivery latency is guaranteed by quantifying the physical link asymmetry during the calibration phase, and with precise measurements and updates of the link, during normal PTP operation. It will be used to transmit the numerical value of the RF frequency (Frequency Tuning Word – FTW) and other controls and timings.

The second paradigm change is the use of a fixed clock for the electronics. This approach is used in other accelerators, BNL [17], GSI [18, 19]. This clock will be recovered from the WR data stream. For BSP, the frequency information will be provided numerically (FTW). Thanks to this absolute clock recovered from the WR, the RF reference can be reconstructed at each receiver. With this new architecture, the problem is the implementation of BSP with fixed clocking. This paper presents a solution for an OTFB.

4. New OTFB solution

In the classic solution, FPGA with a swept clock, the OTFB filter is implemented by means of a periodic Infinite Impulse Response (IIR) comb filter with a delay equal to one exact turn. An alternative must be found with fixed clocking.

4.1. Discarded alternatives

Solutions for specific implementation of the OTFB were analysed and discarded. Among these, the use of a single swept domain clock in a FPGA for implementation of the OTFB comb filter, a bank of filters for the revolution harmonics [20], or alternative filtering architectures, where the response of the filter relies on coefficients which are updated in real time. Technical considerations made these less attractive for the SPS, but the main motivation though was the lack of generality of the solutions for other BSP architectures.

4.2. Selected solution

This paper proposes a solution based on the implementation of the BSP within a dedicated part of the FPGA, using also a fixed clock. This corresponds to the blue region in figure 2. This entity is responsible for the OTFB filter, which tracks the revolution frequency harmonics, dependant on the energy ramping.

The input comes from a rate conversion stage transforming the original signal, into a data stream with a desired effective sampling time inversely proportional to the frequency ramp of the synchrotron. This is the responsibility of the green ReSamPling (RSP) block in figure 2. Within the BSP block (in blue), the resampling has effectively made the data stream beam synchronous and the implementation of the One-Turn-Delay feedback is then very simple. One turn delay again corresponds to an integer number of clock samples.

At the output of the BSP entity, another conversion stage does the opposite translation, from the energy dependant sampling time to the original sampling rate of the signal.

Then follows a filtering block whose response does not change with the acceleration ramp, to implement the beam asynchronous processing, (compensation for cavity and amplifier response, fine adjustment of the full one-turn delay), shown in yellow colour on figure 2.

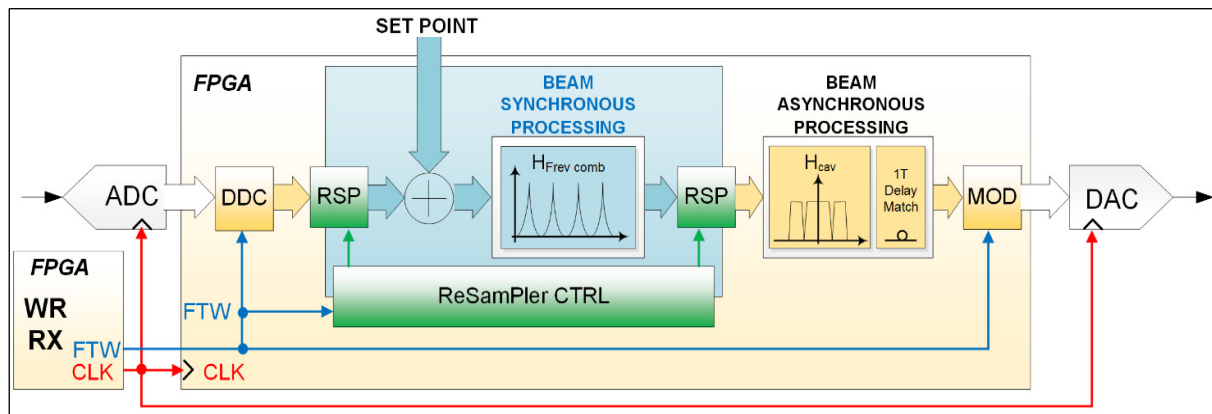


Figure 2. New OTFB implementation showing the two processing regions.

4.3. Hardware architecture

The absolute fixed clock (125 MHz) is recovered in the WR receiver (WR RX) FPGA from the data stream. This FPGA is hosted in a microTCA crate, within the eRTM module [21]. This module is responsible for the generation and management of the clocks and reference signals used in the system. This module is also responsible for the transmission of the numerical frequency value (FTW) to the FPGA implementing the OTFB.

4.4. Conversion stages

The conversion stage shown in figure 2 implements a resampler. Resampling algorithms are used in many applications. They are found in audio equipment, where the recorded music is resampled to accommodate another storing format [22]. They are also used in communication systems, such as Software Defined Radio (SDR). In these systems, the objective is a generic RF front-end, which is able to deal with multiple communication standards and, therefore, different input signal rates. These applications usually aim at fixed and predefined resampling ratio [23]. Fixed resamplers are commonly based upon Cascaded integrator–comb filter (CIC) architectures or polyphase filters. In both, the limitation is the resampling ratio, which accepts only a discrete set of values [24, 25].

Polyphase resamplers decompose the problem in multiple parallel interpolators, “phases”. Each phase computes a value for a given between-sample time difference. The output is obtained selecting the phase that matches the current input-output “time distance” [26]. In the figure 3, the time distance between the first input (blue) and output (red) sample of a resampler is depicted.

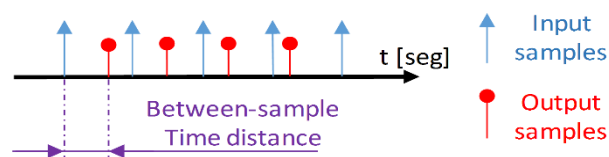


Figure 3. Input/output resampler signals, time distance.

This distance depends on the ratio between sampling times, and for a fixed ratio follows a periodic pattern. This periodicity implies that only a discrete set of phases is needed. In our solution, the resampling ratio is not fixed. It varies with the acceleration ramp. This requires an infinite number of phases. This type of resampler is known as an arbitrary sample rate converter [27].

A Variable Fractional Delay (VFD) filter [28, 29] is used to solve the problem and to compute the between-sample values at the output of the resampler. VFDs are all pass filters modelling a pure delay, which is a fraction of the sampling period. This delay, or time distance, is calculated in real time from the instantaneous resampling frequency, for each output data sample. The only limit is that the resampling frequency must be varied slowly compared to the filtering response time. An efficient implementation of the VFD is the Farrow architecture [30]. Such architecture minimizes the hardware operations needed for computing a resampled output, by optimizing the internal pre-filtering steps [31].

Our solution has been simulated in Matlab. The performances can be seen in figure 4, displaying a spectrum snapshot of the input and output signals. Processing is composed of an upsampler, followed by an intermediate notch filter, and a downsampler at the output. The processing is done with a fixed clock and a variable ratio for the resamplers. In the figure 4 test case, the upsampler ratio is 1.01/1 and the downsampler ratio is 1/1.01. These figures are similar to the SPS case. The input signal is composed of three harmonics at 0.04, 0.08 and 0.12 [f/f_s] normalized frequency (f_s being the sampling frequency). As a proof of principle test, the intermediate filter “notches” out the upper and lower harmonics of the signal, 0.12 and 0.04 [f/f_s]. The spectrum of the regenerated signal exhibits spurious around 100 dB below the input signal. These spurious are artifacts resulting from the resampling process.

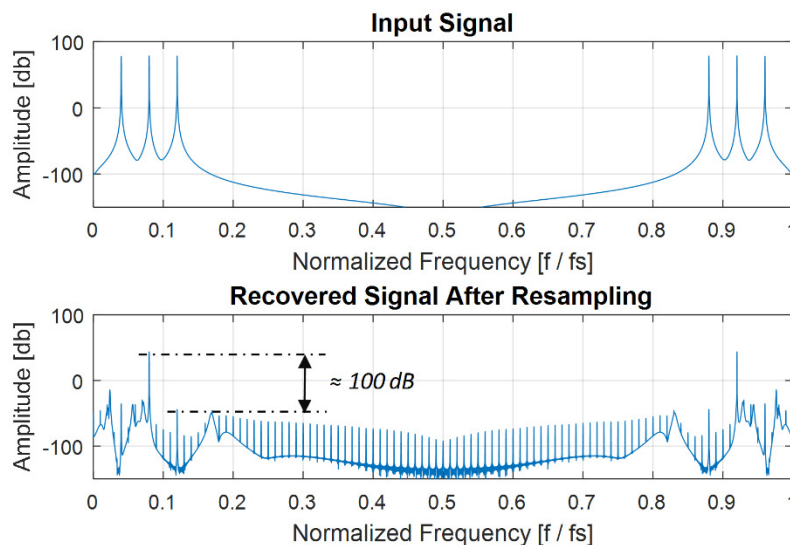


Figure 4. Resampled signal, input and recovered signal.

5. Conclusion

This paper presents a method for implementing a One-Turn-Delay-Feedback with fixed digital clocking, avoiding the swept clock in the current SPS solution. The RF frequency is changed following the acceleration ramp. It is based on a digital resampling of the data stream. The resampler performs beam-synchronous processing in the FPGA without changing the digital clock. Simulations are presented that show an excellent spectral purity. The algorithm is presently being migrated to Simulink, and will later be implemented in HDL. The prototype LLRF will be evaluated on an SPS test cavity, with frequency ramping, in 2018.

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