Master Thesis

Master’s degree in Smart Electrical Networks and Systems (SENSE)

Performance Evaluation of SiC Power MOSFETs for Hybrid & Electric Vehicle DC-DC Converters

Thesis

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Abstract

A continuously growing penetration of electric (EV) and hybrid electric (HEV) vehicles, reinforced by the need for increased energy savings, drove the research towards power electronic components with superior material properties. Wide-bandgap (WBG) power semiconductor materials such as Silicon Carbide (SiC) offer significant improvements in power converter’s performance as they allow higher operating voltage, higher switching frequency and higher maximum operating temperature. As a consequence, it is expected to be utilized in traction DC-DC converters where high efficiency, high power density and lower cooling requirements are desired while, simultaneously, achieving significant reductions in the total weight and volume of the powertrain.

The improved features introduced by SiC MOSFETs on DC-DC converter topologies employed in EVs and HEVs are investigated and experimentally verified. Initially, a non-isolated half-bridge DC-DC converter topology is designed with operating principles that correspond to a converter found on energy management systems of HEVs or fuel cell vehicles. The operating principle of the converter is presented and the bi-directional flow of energy aspect is explained. Subsequently, the design has been modelled and evaluated on a simulation software that considered the operating stages of the converter by also accounting for the gate driving circuit and the predefined cooling requirements. Finally, a test prototype was built in custom-made printed circuit board (PCB) and validated in terms of reliable operation and circuit efficiency.

The benefits from utilizing SiC power semiconductors are presented under constant 24 V loading conditions and 80 kHz switching frequency. A constant voltage was maintained through automatically modulating the gate driving signal, whereas an efficiency of around 96% was achieved due to fast switching times introduced by SiC MOSFETs and thus the reduced switching losses. The efficiency of the system is dependable on the MOSFET operating performance and therefore an exposure of the transistors in environmental conditions was considered for each individual SiC MOSFET provided by different suppliers.

Significant attention has been paid to rapid temperature change, extreme humidity, mechanical vibration and accelerated ageing tests that aim to address possible degradation and defects in the SiC material. The effect of the testing process was examined in component-level, by assessing the electrical characteristics of the SiC MOSFETs, as well as in converter-level by evaluating potential efficiency reductions and operating flaws. Finally, verification of the conditions under which each individual change occurred is of equal importance for prospective improvements in the transistor and converter alike.
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1. Introduction

1.1. Background

Decreasing the global average temperature by reducing, and consequently achieving net-zero energy-related greenhouse gas (GHG), is a problem that has been tackled for the past two decades. Initiatives have been taken in order to shift from the massive energy production based on fossil fuel to a more environmentally friendly and viable solution that will reduce the negative effect of climate change. The wide penetration of renewables such as photovoltaics (PV) and wind turbines, have managed to reduce the amount of \( CO_2 \) emissions in the atmosphere. Despite this turn towards a more sustainable production of electric energy, major cuts must be delivered in other industries, one of which is transportation, in order to meet this long-term goal. The deployment of electrified transportation could be one of the most suitable solution towards the decarbonization of the global energy system.

Electrified transportation will include both commercial vehicles and public transport utilized in urban environments. As far as the public transportation is concerned, many countries have already deployed fully electrified buses in large urban cities with the most apparent example the city of Shenzhen in China, the only city worldwide with all-electrified public transportation. On the other hand, electric (EV) and hybrid electric vehicles (HEV) for private owners have been introduced into the market since the early 2000s and their penetration is expected to grow further in the upcoming years. For instance, by 2040 electric vehicles is estimated to possess 33% of the global car fleet [1]. EVs and HEVs will certainly become more price competitive in the forthcoming years mainly due to the increase in fossil fuel price and the decreased battery costs. Their large-scale implementation will eventually reduce both the amount of pollutants in the atmosphere and the noise in large urban centers.

Increasing the number of EVs and HEVs shifts the focus on the power losses issue that exist in these types of vehicles. Increased power losses are not beneficial neither for the electrical grid nor for the consumers. Therefore, it is important to increase the efficiency of energy consumption in power electronic converters employed in such vehicles in order to minimize the overall power losses.

A power electronic converter is an electronic circuit that either changes the voltage level between the input and output or both the voltage level and the frequency as in the case for an AC-DC rectifier or DC-AC inverter. Its operation is based on the switching sequence and frequency of the employed power transistors based on a pulse modulated signal that drives their gate. Power converters, especially DC-DC converters, are employed in all EVs and HEVs in order to supply electricity to low voltage loads such as lights and electronic control units.
Albeit their complexity is based on the type of vehicle, for instance electrically isolated converters are utilized in EVs while non-isolated DC-DC converters can be employed in HEVs, the largest portion of power losses, during their operation, is dissipated in the power semiconductors which limits the converter’s operation in terms of power density and frequency.

For years, silicon (Si) has been the material most commonly utilized in power semiconductors such as MOSFETs and IGBTs and dominated the market due to its wide availability and price. However, the growing requirements of the automotive industry, especially in terms of efficiency, has shifted the interest towards newly emerged technologies that do not exhibit the limitations of Si, for instance, lower operating temperatures and slower switching times. Silicon Carbide (SiC) and Gallium Nitride (GaN), which form part of wide-bandgap (WBG) semiconductor materials, have attracted much attention in recent years. In particular, they allow for higher switching frequencies, higher blocking voltage capability, higher maximum operating temperatures, higher thermal conductivity and lower voltage drop which make them suitable candidates for high power density and efficiency applications. These material properties affect the overall converter circuitry in terms of cooling requirements, robustness and volume.

The interest in WBG materials has driven the manufacture of high quality power semiconductor devices which can compete with their conventional and much cheaper Si counterparts. As long as the manufacturing cost declines every year [2], their implementation in automotive power converters is certain. Besides, the penetration of more and more competitors on the WBG market will only accelerate the cost reduction and the improved features that these power devices can offer. One of the remaining questions is how their characteristics could be affected when exposed to extreme operating conditions.

1.2. Main Objectives

The main objective of this thesis project is to evaluate the suitability of SiC MOSFETs, for EV and HEV applications, assess their characteristics when operating in power converters and examine the effect of different testing condition on component- and converter-level. The goals that this project aims to achieve are the following:

- Study and design DC-DC power converters based on commonly implemented modules in market available electric vehicles.
- Evaluate the characteristics of SiC MOSFETs during the operation of the converter under various loading conditions.
- Expose the MOSFETs to adverse environmental conditions and evaluate their effect on the power transistor.
- Assess how the implemented tests on a component-level might impact the overall
• Indicate potential defects and mechanisms that might affect the reliability of the converter in the long run.

1.3. Thesis Outline

The overall project is divided into two distinctive parts: the first part covers the theoretical background of SiC power semiconductors and the design process that was followed all the way to the prototype implementation, while the second part presents the implemented tests and the obtained results. More specifically, the thesis is outlined as follows:

• **Chapter 1** gives a brief background on the evolution and penetration of EVs and HEVs as well as the potential that WBG materials might have in the automotive industry. Overall, the project is introduced and the main objective and goals are presented.

• **Chapter 2** analyzes the theory behind WBG semiconductor material by giving details about their structure and the main features. A comparison is made between Si and SiC power semiconductors and some challenges regarding the deployment of SiC MOSFETs are given. The chapter concludes with the current implementations of SiC in the automotive industry.

• **Chapter 3** details the design of the power converter circuit. It presents the power electronic module and the design of the passive components utilized as well as the modelling of the corresponding heat sink based on the cooling requirements.

• **Chapter 4** gives an overview of the implemented prototype and compares the simulation results with the ones taken from the operation of the converter under lab conditions.

• **Chapter 5** presents the results obtained from the testing of SiC MOSFETs under environmental conditions. The chapter makes a comparison between the results taken before and after the various tests and intends on analyzing the effect of each test on the MOSFETs' characteristics and the overall efficiency of the converter.

• **Chapter 6** summarizes the project by drawing conclusions and gives a new trajectory for future work and ideas.

• **Appendix** provides information regarding the project’s overall budget.
2. SiC Power Electronic Components: Theoretical Background, Characteristics & Current Market Trends

This chapter highlights the basic MOSFET characteristics that are important for the conduction of the project and, in general, the operation of DC-DC power converters in automotive applications. Initially, a brief introduction to the MOSFET’s operating characteristics and their application in DC-DC converters is given. The basic advantages of SiC technologies are discussed and a comparative analysis between Si and WBG technologies is mentioned. Subsequently, the market status of SiC power semiconductors as well as their utilization in the automotive industry is stated based on literature review.

2.1. MOSFET Technology

MOSFET, an acronym for the Metal-Oxide Semiconductor Field-Effect Transistor, is an inherent part of the power electronics industry due to its on-state current and blocking voltage capabilities. It has been widely used for application where high switching frequency has to be achieved and increased efficiency is required. The conductivity of the device is controlled via the applied gate voltage and can be utilized for the amplification or the switching of electronic signals. The output current is proportional to the applied charge on the device, which is given from a low-impedance source that provides sufficient current to control the transistor’s charge [3]. Additionally, they can be utilized for high-frequency applications due to their high-switching speeds, which is the time required by the charge carriers to traverse the semiconductor region, that can vary from tens to hundreds of nanoseconds.

Structurally, a power MOSFET is a three-terminal unipolar device with four alternating layers of p- and n-type doping across its main body. The layer structure discriminates the MOSFETs into two types: the n-channel and the p-channel MOSFETs. Each of these types is presented with three terminals where the gate of the MOSFET controls the current flow between the drain and source, when a voltage is applied to the gate. The fundamental difference between these two MOSFET types depends on the conduction of the current.

- In the **n-channel** MOSFET, a positive voltage is applied to the gate resulting in a flow of negative-charged electrons between drain and source.

- In the **p-channel** MOSFET, a negative voltage is applied to the gate which results in a flow of positive-charged holes between drain and source.

In general, n-channel MOSFETs are preferred over their counterparts as the mobility
of electrons is much higher than of holes [4]. As a consequence, the project deals only with the former type of MOSFETs. The structure and electrical symbol of an n-channel MOSFET is given in Fig. 2.1.

![Image](image.png)

Fig. 2.1: Cross-section (left) and equivalent model (right) of n-channel power MOSFET [3]

In Fig. 2.1, the $n^+$ region is the doping in the drain and source layers, while the $p^+$ region is the body of the MOSFET where the conducting channel between drain and source is created. The $pnn$ junction between drain and source prevents the free flow of current even when voltage is applied between these two terminals. Nevertheless, applying a voltage that biases the gate positively with respect to the source results in the attraction of electrons from the $n^+$ source and drain regions thus forming an n-channel that allows the flow of substantial current [4]. The magnitude of the applied voltage to the gate is responsible for the number of concentrated electrons beneath the gate oxide and therefore the width of the n-channel.

2.1.1. Modes of Operation – V-I Characteristics

In power converter applications, MOSFETs are utilized as switches in order to control the power flow towards the load and, especially in DC-DC converters, the output voltage. In such cases, the operation of a MOSFET can be divided into three different modes based on the voltage applied to the control terminals. The operating regions of a MOSFET are given in accordance with the V-I characteristics of Fig. 2.2.
In the cut-off region, the MOSFET acts as an open-switch thus not allowing the current flow between the output terminals. The MOSFET must be designed to withstand the breakdown voltage applied between the drain and source ($BV_{DS}$) in order to avoid breakdown. In this mode, the applied voltage between gate and source is in the magnitude of some volts and is lower than the gate threshold voltage $V_T$ given by the aforementioned figure.

When the gate-to-source voltage reaches the threshold, the MOSFET enters the ohmic region where the voltage across the terminals, $V_{DS}$ and the current, $I_{DS}$ increase linearly due to the creation of a channel. In this region, the MOSFET acts as a resistor controlled by the gate voltage and operates as an amplifier. In order to enter the ohmic region, the following condition must be fulfilled:

$$V_{GS} - V_{GS,th} > V_{DS} > 0$$

Finally, in the saturation or active region, the conducting channel has been fully created and the current flow between the drain and source terminals is dependent only on the gate-to-source voltage $V_{GS}$, according to Fig. 2.2. Therefore, the MOSFET acts as a closed switch. That being said, by increasing the applied control voltage, the width of the conducting channel increases thus allowing more current to flow between the output terminals. In this case, the condition that must be met is given by eq. (2.2):

$$V_{DS} \geq V_{GS} - V_{GS,th} \text{ and } V_{GS} > V_{GS,th}$$

### 2.2. WBG Semiconductor Material

Modern electrified transportation has reemerged with the beginning of the 21st century when the need to reduce fossil fuel consumption and focus on renewable energy became imperative. The electric power conversion and control relies strongly on the utilization of solid-
state electronic devices in the field of power electronics. Silicon (Si) is the dominant material utilized in power semiconductors such as transistors and diodes, due to its superior physical and electrical properties, its abundancy on earth as well as to the effective extraction and purification methods that justify its relative low cost.

However, this particular technology has reached its maturity and therefore material limitations arose when considering the growing energy needs. For instance, there is a need to reduce the portion of power losses dissipated in power semiconductors and due to silicon’s limitations, the overall efficiency and energy savings are reduced significantly. As a result, the turn towards power electronic components with superior properties than their Si-based counterparts paved the road for the WBG semiconductor materials.

2.2.1. **Definition of Energy Bandgap**

Materials are comprised of a series of electron energy levels, the energy bands, that hold a number of electrons, based on their primary number. According to quantum physics, the higher the number of electrons, the higher is their distribution in energy bands. When an external energy source is applied to the material, the electrons tend to move to higher energy bands by absorbing this energy and then return to their origin by releasing this gained energy. The energy bands theory can be summarized in the following simplified Fig. 2.3.

![Fig. 2.3: Simplified energy band diagram of semiconductor](image)

Supposing that thermal energy is applied on the material of Fig. 2.3, in order for an electron to move from the valence band with energy $E_v$ to the conduction band where its energy will rise to $E_c$, the required amount of energy is $E_g = E_c - E_v$ which is the energy of the bandgap between these two energy bands. The width of the bandgap varies between materials and determines their electrical properties. For the conductors, the absence of bandgap means that the two energy bands overlap and the electrons can move to higher
energy bands by applying small amount of energy. On the other hand, in the insulators, the energy source must be very high in order for the electrons to overcome the bandgap justifying the limited flow of electric charges [6].

The electrical properties of a material could be modulated by the introduction of impurities via a process called doping. In relation to the energy bandgap theory, doping introduces additional allowed energy states within the energy bandgap close to the energy bands. Based on the dopant type, the energy states could be created close to the conduction band (electron donor impurities, n-doped semiconductors) or close to the valence band (electron acceptor impurities, p-doped semiconductors).

An application of a small amount of energy is possible to thermally ionize the dopant atoms and thus creating free charge carriers in the conduction or valence band. In that case, the energy bandgap is such that only a small amount of energy is necessary to push the electrons between the energy state of the dopant and the energy band making them able to operate with very little energy input. However, the width of this bandgap is the main reason behind the superior properties of WBG materials compared to mid-range bandgap materials such as silicon or Gallium Arsenide (GaAs), as it will be demonstrated in the next paragraph.

### 2.2.2. Fundamental Properties of WBG Materials

Through harnessing the capabilities of WBG materials, a new generation of power semiconductors has developed that has the potential of operating in higher temperatures, switching speeds and operating voltages than the already established Si technology. Utilized in power converters, they will allow transformation of electric energy with increased efficiency compared to the existing Si-based power converters while achieving reductions in volume unit and improvements in their overall robustness [7]. The benefits of the utilization of WBG materials can be observed both in component and converter levels.

The most prospective candidates of WBG materials that are being utilized in power semiconductors manufacturing are Silicon Carbide (SiC) and Gallium Nitride (GaN), albeit there are other potential solutions that could be exploited, such as diamond-based semiconductors, though their manufacturing cost is prohibitive [8]. The main reason for this choice of material is a combination of their aforementioned WBG characteristics with the availability of the substrate and epitaxial materials utilized for the material’s process techniques and the maturity of the overall technology.

More specifically, in terms of bandgap energy, a mid-range bandgap material such Si or GaAs has 1.12 eV and 1.43 eV respectively, while a WBG material has a bandgap energy greater than 3 eV. In general, the wider the energy bandgap of the material, the more promising are the features for the semiconductor, a fact that is demonstrated in Table 1.1.


Table 1.1: Si, SiC and GaN material properties [8][9][10]

<table>
<thead>
<tr>
<th>Semiconductor</th>
<th>$W_g$ (eV)</th>
<th>$E_{crit}$ (MV/cm)</th>
<th>$n_i$ (cm$^{-3}$)</th>
<th>$\mu_n$ (cm$^2$/Vs)</th>
<th>$\varepsilon_r$</th>
<th>$\lambda$ (W/cmK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.12</td>
<td>0.29</td>
<td>$1.4 \times 10^9$</td>
<td>1350</td>
<td>11.9</td>
<td>1.5</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.43</td>
<td>0.4</td>
<td>$1.8 \times 10^6$</td>
<td>8500</td>
<td>13.1</td>
<td>0.5</td>
</tr>
<tr>
<td>SiC</td>
<td>3.28</td>
<td>3.0</td>
<td>$8 \times 10^{-9}$</td>
<td>1000</td>
<td>9.6</td>
<td>4.9</td>
</tr>
<tr>
<td>GaN</td>
<td>3.4</td>
<td>3.3</td>
<td>$2 \times 10^{-10}$</td>
<td>1500</td>
<td>9.0</td>
<td>1.3</td>
</tr>
</tbody>
</table>

*Fig. 2.4: Device length of Si and SiC Schottky diodes based on the electric field energy [9]*

According to Table 1.1, $W_g$ is the energy bandgap of the semiconductor that is required by an electron to move from the valence to the conduction band. A material with higher bandgap than 2 eV of energy is considered as WBG. The maximum electric field $E_{crit}$ is a property that defines the breakdown voltage of a material. Higher $E_{crit}$ increases the blocking voltage capability and allows for higher doping concentration $n_i$ which consequently reduces the electrical resistivity of the material [8]. On the other hand, $\mu_n$ refers to the electron mobility which is the speed of an electron under a given electric field. The relative electric field permittivity $\varepsilon_r$ demonstrates how fast the interelectrode capacitance of the material can charge and discharge thus affecting the switching speed of the semiconductor. Finally, $\lambda$ is the thermal conductivity of the material and is related to how fast the temperature of the material could rise.

Noticeable improvements that have been introduced by GaN and SiC to the power semiconductors’ operating features and are analyzed below [8]:

![Schottky contact and Ohmic contact diagram](image-url)
• **Higher operating temperatures**: Compared to Si and GaAs, WBG materials have almost three times larger bandgap energy $W_g$ which allows them to operate at temperatures up to 300˚C with higher thermal conductivity $\lambda$ while for Si-based semiconductors the maximum temperature is around 150 ˚C. At these temperatures, electrons excite to the conduction band and thus WBG allows for safer operation compared to Si-based semiconductors in elevated temperatures.

• **Higher breakdown voltage**: Higher $E_{\text{crit}}$ justifies the higher breakdown voltage of WBG semiconductors compared to Si. As long as the electric breakdown field strength is larger in SiC compared to Si, SiC power electronic components can be made significantly thinner which reduces the resistance during conduction of current. The effect of electric field on the size of a Schottky diode can be seen in Fig. 2.4.

• **Lower ON-state resistance**: Higher electron mobility $\mu$ means that the speed of electrons under an electric field is higher indicating less electrical resistance. ON-state resistance is also inversely proportional to the electric field energy. Consequently, an increase in $E_{\text{crit}}$ as stated in Table 1.1, explains the lower ON-state resistance of SiC-based devices [9].

• **Higher switching speed/frequency**: Switching between ON- and OFF-states is higher for WBG materials as $\varepsilon_r$ is lower thus allowing higher switching speeds and frequencies due to the significantly reduced switching losses.

• **Higher thermal conductivity**: In SiC, thermal conductivity $\lambda$ is about three times larger than Si which means that their thermal resistance is lower and that junction temperature rises at a lower rate compared to Si devices. Therefore SiC-based applications have lower cooling requirements thus reducing the size, volume and complexity of cooling systems [9].

Figure 2.5 summarizes the aforementioned comparative analysis between SiC, GaN and Si characteristics observed in power electronics.
Fig. 2.5: Comparison between Si, SiC and GaN electrical characteristics [7]

The benefits of this type of materials has upgraded the operation of power converters as well. By exploiting the special characteristics of SiC and GaN transistors and diodes, the efficiency of power converters can be increased significantly resulting in reduction of power losses. Specifically, the introduction of WBG materials has the following impact on the converters’ operation:

- **Higher efficiency**, as a result of reduced switching and conduction losses in the power electronics.

- **Lower harmonic distortion** due to an inherent ability to operate at higher frequencies where harmonics are generated at higher frequencies in the Fourier domain and thus can be easily filtered.

- **Reduced cooling requirements** due to the combination of reduced losses and ability to operate at higher temperatures.

- **Reduction in size and volume** which is indicative of the lower volume of transformer’s winding and filter’s inductor.

2.2.3. **Applications based on WBG Materials**

The inherent advantages of WBG semiconductors have been identified throughout the last years and various applications have benefited by utilizing this material in power electronics components. In a way, WBG materials have paved the way towards energy savings in various applications and achieving the desirable reduction in power dissipation. WBG-based power devices can be found from high voltage all the way to low voltage commercial applications.
Considering the aforementioned benefits regarding the operation of power converters, below are listed some applications where SiC and GaN materials have been utilized and their impact on the efficiency is discussed:

- **Renewable Energy Sources**: Wind energy generation systems can experience high efficiency operation for higher frequencies and almost constant with the increase of the MOSFET’s junction temperature while, at the same time, size and cost of the system is critically reduced [11]. On the other hand, apart from the increased PV inverter’s efficiency, Schwarzer et al. [12] discusses the various cost models of a PV inverter, mainly the heat sink, magnetics and power modules, where the effect of SiC power components resulted in a 20% reduction of the system’s total cost. Additionally, SiC devices can ensure high reliability and lifetime even when operating in harsh environmental conditions [13].

- **Railway Traction Converters**: Traction converters are utilized to either change the frequency and magnitude of the voltage or rectify the electrical network’s AC voltage to DC. Fabre et al. [14] examined the impact of SiC MOSFETs introduced in traction power converters in railway networks and demonstrated that an increase in frequency can reduce the switching losses up to 60% compared to Si-based converters and consequently impacting the volume and specifications of the cooling system.

- **Automotive**: High power density, increased efficiency, lightweight and compactness are anticipated benefits from the utilization of WBG power components and will impact the powertrain design of electric and hybrid vehicles. Indicatively, the converter model of Toyota Prius 2010 was considered by Shang et al. [15] where WBG-based power electronics were utilized. The advantage of these materials was evident for high switching frequencies. The application of SiC power electronics in automotive will be discussed in detail in the next sections.

- **Aerospace**: Small mass and volume, high temperature operation and protection from radiation are some of the requirements imposed by spacecrafts. Even though the majority of these advantages have already been mentioned, WBG materials are also less susceptible to radiation damage which reduces the additional mass from radiation shielding [6].

- **Data Centers**: A 7,5 kW, 3-phase AC rectifier was designed for a data center utilizing SiC-based power semiconductors by Zhang et al. [16]. The converter’s efficiency reached a value of 98,5% operating at full load. Moreover, a necessary part of the converter was an LLC resonant converter designed with GaN power electronics. Results showed a peak efficiency of 96,1% at full load, values that could not be achieved, for the same operating conditions, with Si transistors and diodes.
• **Microgrids**: The implementation of microgrids in order to reinforce sustainability will require high-efficiency low-volume power converters that currently cannot be achieved with conventional Si-based components. Furthermore, the potential utilization of DC transmission and distribution networks must ensure minimum energy losses dissipated in power converters which currently can be achieved only with WBG materials [17].

Fig. 2.6 makes a demonstration of where SiC can be utilized from medium-voltage applications such as photovoltaic inverters to high-voltage electric grids and transportation.

![Fig. 2.6: WBG applications based on operating voltage [18]](image)

In low voltage applications, SiC devices cannot offer substantial performance boost compared to commonly utilized Si DC-DC converters. The achievements in efficiency and power density are outweighed by the increased cost of SiC devices and therefore there will be no benefit from the utilization of SiC. Medium to high voltage applications i.e. greater than 600 V, can be benefited from SiC, as already stated, due to increased efficiency in PV inverters, which will balance the increased cost of inverters, and due to higher operating temperatures in automotive. However, in high power and voltage applications, SiC’s superiority is undeniable as its performance cannot be achieved by Si. A case in point is a 5-kV converter where an efficiency equal to 99% could be achieved with SiC devices [19]. This group of applications is expected to be the main focus of SiC without excluding medium voltage, especially when the cost of SiC is continuously decreasing.

### 2.3. Current Status of the SiC MOSFET

The evolution of SiC MOSFETs before market launch faced many obstacles, the majority of which related to the gate oxide material, which resulted in severe reduction in carrier...
mobility and was responsible for instabilities of the threshold voltage. The channel mobility caused relatively high on-state resistance thus hindering its overall reliability [20].

However, the advancements of SiC MOSFET technology eventually led to the widely available 1,2 kV SiC MOSFET where threshold voltage had become stable, oxide lifetime had increased and mobility was enough to ensure the readiness of this technology and its reliable operation. A case in point is [21] where researchers studied accelerated lifetime tests implemented on Monolith Semiconductor’s MOS technology which showed that the gate oxide’s lifetime can exceed 100 years even when operating at junction temperatures up to 300 °C. As far as the voltage threshold stability and blocking voltage, no significant shift was observed during testing at 175 °C under varying applied gate and drain-to-source voltage respectively. As a result, obstacles had been overcome and a stable and reliable device had been launched.

Based on the aforementioned test results, the wide penetration of SiC power MOSFETs is a result of multiple suppliers providing high-quality reliable products considering customers’ needs. Since 2011, the normally-off n-channel power MOSFET with blocking voltage between 600 V and 1,2 kV was widely available. In fact, manufacturer CREE Wolfspeed initialized a power MOSFET with breakdown voltage of 1,2 kV and ON-state resistance 80 mΩ with maximum current capability at 42/ 24 A depending on junction temperature. Similarly, Rohm Semiconductor introduced the 35 A/ 1,2 kV – 80 mΩ device while the main goal was to introduce the 120 A/ 1,2 kV fully operated SiC device (SiC MOSFET with anti-parallel SiC Schottky diode) for operation at frequencies higher than 100 kHz [7].

Recent advancements in the SiC MOSFET technology include the newly-launched ST Microelectronics SiC MOSFET with extremely low ON-state resistance, $R_{DS,\text{on}} = 22 \, \text{mΩ}$ at 150 °C, 650 V which aims to increase the efficiency of electrified vehicle inverters up to 3% and therefore achieving longer battery life and lighter units [22]. In a similar manner, CREE Wolfspeed launched a new device of 900 V, 10 mΩ SiC MOSFET which can achieve blocking voltage capability across the operating temperature range. The device resulted in an almost 78% reduction in switching losses which allows electric vehicles to reap the benefits of the SiC technology [23]. Other manufacturers such as Rohm Semiconductor, Microsemi and Infineon have launched the 3rd generation of SiC MOSFET with improved characteristics which aim to accomplish high efficiency rates while preserving the quality and reliability of the device.

2.3.1. Comparative Analysis between SiC MOSFETs and Si IGBTs

The target applications of SiC MOSFETs are those where Si IGBTs were previously dominating, mainly between some hundreds of volts to some thousands of Volts depending on the application, according to Fig. 2.7. The purpose of exploiting the inherent characteristics of SiC technology is to increase the system’s efficiency, while achieving significant reductions
Having high ON-state resistance, Si IGBTs have been so far the optimal solution for high voltage applications compared to Si MOSFET. Due to the injection of minority carriers in the drift region, IGBTs eventually achieved lower values of ON-state resistance resulting in their dominance in power converter applications over MOSFETs. On the contrary, the minority carriers were responsible of a current tail during turn-OFF which increased the switching losses and thus limiting the operating frequency [10]. This compromise that had to be made was dictated by the fact that no other power semiconductor could achieve both the aforementioned features.

The losses introduced by the existence of current tail in IGBTs are not found in SiC MOSFETs as no conductivity modulation is required to reduce the ON-state resistance. Consequently, the operating frequency of SiC MOSFETs is substantially higher than IGBTs with clearly lower switching losses. Rohm Semiconductor examined the effect of current tail in the amount of losses where it can be observed that the turn-OFF energy ($E_{OFF}$) of SiC MOSFETs is almost 90% lower than of Si IGBTs for the same operating conditions [10]. In addition, current tail of IGBTs is increased with temperature, whereas in SiC MOSFETs there is no such dependence. Fig. 2.8 gives a graphic representation of current tail in IGBTs and MOSFETs. The current tail is marked in the Si IGBT turn-OFF graph, whereas it is negligible in the SiC MOSFET.
The performance properties of these two types of semiconductors were highlighted by CREE Wolfspeed in a research project where a 11-kW DC-AC inverter was designed for the evaluation of Si IGBT and SiC MOSFET [24]. The purpose of the project was to utilize a 1,2 kV, 100 A transistor of each type and examine the impact of SiC on the inverter’s efficiency compared to the widely utilized Si IGBT. More specifically, one leg of the converter consisted of a SiC MOSFET and the other with a Si IGBT using unipolar PWM. When one leg switched at high frequency of 20-40 kHz, the other one switched at 60 Hz. As the conduction loss is almost independent of the switching frequency, the loss difference depends on the applied frequency at each leg and depicted the effect on the inverter’s efficiency and total losses.

The project demonstrated an independence of the switching losses from the operating temperature in case of SiC MOSFETs compared to IGBTs which indicate an almost flat efficiency curve for the range of operating temperatures. Moreover, Fig. 2.9 compares the switching losses of the Si IGBT and SiC MOSFET for the utilized frequencies. It can be observed that the utilization of SiC MOSFETs resulted in significant reduction in the switching losses leading to an efficiency of 98.5% at 40 kHz.
The blue curve in the left and right graph of Fig. 2.9 represent the power component's switching losses. Introducing a SiC MOSFET in the DC-AC inverter resulted in almost 80% reduction in the switching losses, for the 40 kHz case thus demonstrating the ability of SiC MOSFET to operate efficiently in higher frequencies.

ST Microelectronics made an experimental evaluation of the efficiency of DC-DC boost converter operating at 50 kHz with different output power levels [25]. The devices utilized include a 1,2 kV – 80 mΩ SiC MOSFET (SCT30N120) and a 1,2 kV 25 A Si IGBT in order to demonstrate the differences at various switching frequencies. The converter also employed the same type of anti-parallel SiC diode, despite the switching device. Therefore, the results presented below correspond to the shift from Si IGBT to SiC MOSFET.

The results had shown that although the IGBT is still a viable solution for 25 kHz operating frequency, SiC MOSFET's switching losses are lower resulting in higher efficiency for the same output power. As far as the 50 kHz operating condition is concerned, IGBTs have reached their maximum allowing operating temperature and therefore it is not considered a potential candidate. On the other hand, SiC MOSFET’s operation demonstrated excellent results with almost flat efficiency curve for various output power levels as shown in Fig. 2.10.

![Fig. 2.9: Total loss comparison in IGBT (left) and SiC MOSFET (right) for a 11 kW DC-AC inverter [24]](image)

![Fig. 2.10: Efficiency comparison of SiC MOSFET and Si IGBT for 50 kHz DC-DC boost converter [25]](image)
In Fig. 2.11, it can be seen that for frequencies higher than 50 kHz, the converter’s overall efficiency is higher than 98% regardless of the switching frequency for the evaluated loading conditions. The ability of operating safely at such frequencies is one of the defining characteristics for their wide implementation.

![Converter’s efficiency for different loads at 100 kHz and at 125 kHz switching frequency](image)

**Fig. 2.11: Converter’s efficiency for different loads at 100 kHz and at 125 kHz switching frequency [25]**

Another interesting result from this research is the case temperature behavior of the Si IGBT compared to SiC MOSFET for various loading conditions, according to Fig. 2.12. By increasing the output power, the IGBT’s case temperature increases abruptly whereas the MOSFET’s temperature presents a smoother increase. The fast increase in the case temperature of IGBT limits the operation of the DC-DC converter at 5 kW output power. On the contrary, SiC-based converter is allowed to operate safely at higher output power due to the significantly lower case temperature of the transistor.

![Case temperature comparison for various loading conditions for a 50 kHz DC-DC boost converter](image)

**Fig. 2.12: Case temperature comparison for various loading conditions for a 50 kHz DC-DC boost converter [25]**

The advancements in the operation of power electronic converters, as stated so far, owing to their implementation with SiC-based devices, can drive the design of power converters to a new direction. The ability of operating above 100 kHz of switching frequency allows for a substantial decrease of the size and weight of the converter’s LC filters, i.e. inductors and capacitors, thus resulting in a more compact converter. This is a result of the
shifting of harmonics to higher frequencies which justifies the need for smaller passive components to achieve a desirable harmonic content in voltage and current. Furthermore, the high switching speeds are related to the reduced noise in the circuit design and therefore reduced space of electromagnetic interference (EMI) filters [13]. In addition, the converter’s cooling systems are affected by the significant reduction in power losses and the ability of operating at junction temperatures which allows for simplifications in their design.

2.4. Challenges & Limitations of SiC

SiC power electronic components are not only responsible for the performance boost in the converter operation, but also for a number of challenges that have arisen with their deployment and are not found in common Si-based components. The reviewed challenges are related to the manufacturing of SiC-based electronic components but, more importantly, to the power converter module during operation which, in the latter case, can limit the converter’s performance.

Production cost of SiC material is the most important drawback of this technology. SiC is not available the same way as Si in nature and therefore complicated manufacturing methods are followed to produce the material from Si which increase the overall cost. Adding to this, the need to reduce different types of material defects and produce large wafers of SiC further introduce additional costs which are avoided during the production of Si components.

The elimination of the aforementioned defects is one of the most complicated tasks in the manufacturing process of SiC components. The intrinsic defects observed in the interface of SiO₂ (silicon dioxide) with SiC are not related to impurities or dopants. These defects are responsible for the reduced reverse voltage blocking capability and temperature performance as well as the low channel mobility in SiC [26]. The latter is justified as the defects appeared as traps in the energy gap of SiC. In order to deal with this issue, the quality of the metal-oxide semiconductor interface must be improved. Currently, a nitridation process is adopted that reduces significantly the presence of defects in the interface thus improving the reliability of SiC electronic components [27].

Eliminating these defects, however, results in a significantly smaller chip area in SiC than Si. The first issue that occurs in this case is that the thermal resistance decreases with the chip area which means that more emphasis should be put on heating dissipation [28]. Since the body diode shares the same chip with the MOSFET, the current load will increase leading to substantially more losses that need to be cooled away. Consequently, the utilization of heat spreading mechanisms and integrated heat sinks have increased the complexity of SiC MOSFETs.
Operating SiC electronic components at high-temperature environments reinforced also the need for more advanced packaging materials than the simpler ones utilized in Si MOSFETs. Package reliability is important so that the transistor can operate in, for example, automotive motor drives, space power supplies and military applications where the ambient or coolant temperature can be higher than 150 °C. In addition, proper packaging increases the power handling capability in various applications. Indicatively, the SiC advantages cannot be realized if traditional packaging methods are utilized and the MOSFET operates at high frequency as low thermal efficiency is achieved. This happens because the MOSFET's performance is negatively affected by wave propagation effects [29].

2.4.1. Challenges in Converter Design & Operation

When utilizing SiC MOSFETs in converters, a trade-off must be made between the high switching frequency and the fast switching transients that occur in the device and package which are sources of electromagnetic parasitics. These transients provide additional energy to the parasitic inductance and capacitance in the circuit and cause voltage and current overshoots, parasitic turn-ON and ringing.

For example, a parasitic inductance which is formed between the equivalent series inductance (ESL) of the DC capacitor, the inductance of the printed circuit board (PCB) and the inductance of the package is the main source of voltage overshoots during turn-OFF and Electromagnetic Interference (EMI) in converters. Moreover, a parasitic inductance is formed between the gate driver circuit and the gate of the semiconductor which causes ringing in the gate signal as a result of the resonance circuit that is formed with the gate-source capacitance. On the other hand, parasitic capacitances provide paths for high frequency currents that produce overcurrent spikes during switching, increase EMI emissions and slow down voltage transients [28]. As a consequence, additional design considerations must be made in order to deal with these issues that will reduce the performance and efficiency of the converter.

Fig. 2.13 demonstrates the turn-OFF switching transient, given by the blue waveform, occurred in two identical converters implemented with SiC MOSFET (left) and Si IGBT (right), respectively, for similar $\frac{dv}{dt}$ which shows how fast the voltage rises over time. Although there is significant overshoot in both cases given by $V_{OS}$, high frequency oscillations occur when the MOSFET is turned OFF and reach almost 26 Mhz. On the other hand, the ringing is absent when the IGBT is turned OFF because IGBT’s tail current functions as turn-OFF snubber circuit thus suppressing the ringing effect [30]. To reduce either the overshoot or the oscillations to an acceptable level, the parasitic inductance must be reduced or a lower switching frequency should be utilized. In the former case the complexity of the circuit is increased substantially while in the latter, the switching losses are increased.
Fig. 2.13: Turn-OFF transient for SiC MOSFET (left) and Si IGBT (right) for the same $\frac{dv}{dt}$ [30]

EMI is also an important issue that must be addressed when fast switching speed are utilized due to the high rate of $\frac{di}{dt}$ when charging and discharging the MOSFET’s internal capacitance. Depending on the application, EMI must be kept within permissible levels in order to avoid damage of the adjacent electronic circuits or the load that is connected to the converter. For instance, EMI can cause significant damage to electric motors and therefore measurements must be taken to reduce its presence in the electronic circuits [30]. The most common ones are the increase of the external gate resistance of the MOSFET and the implementation of EMI passive filters.

Fig. 2.14 shows the effect of gate resistance on the ringing and current overshoot for a SiC MOSFET given by the red waveform. Increasing the gate resistance from $R_g = 1 \, \Omega$ on the left graph to $R_g = 5 \, \Omega$ on the right graph resulted in significant reduction of both the current overshoot $I_{OS}$ and ringing. However, it is evident that $\frac{di}{dt}$ has decreased when the gate resistance increases resulting in slower turn-ON which consequently increases the switching losses of the converter and affects negatively the efficiency.
The alternative solution is the implementation of common mode (CM) filters to reduce the EMI in power converters. CM noise occurs in all electronic circuits due to the flow of current through parasitic capacitance between the circuit and the common ground. To deal with CM noise, a filter is utilized which is comprised of two magnetically coupled coils. CM currents will not flow through the filter as it results in zero potential difference between the two coils. Dos Santos et al. [31] utilized SiC components in inverters for aircraft applications and evaluated the utilization of CM filters to EMI. When the gate resistance of the MOSFETs reduced from $R_g = 10 \, \Omega$ to $R_g = 1 \, \Omega$, the maximum $\frac{dv}{dt}$ increased by 50% and therefore larger CM filters were required. A larger filter, however, introduces greater resistance due to the wiring of the coil and thus additional losses. Therefore, it is obvious that in both cases a trade-off between losses and EMI must be made for the inverter.

Finally, another limitation in the design of SiC converters is the gate driver circuit. In order to reduce the parasitic inductance between the driver and the MOSFET, the two must be placed close to the converter circuit. However, the challenge is that the driver must provide $+20 \, V$ and $-5 \, V$ with minimum output impedance and high current capability [32]. Negative bias voltage is important as it can solve the parasitic turn-on effect that is caused by the gate-drain capacitance and thus ensure that the MOSFET is OFF. In addition, the driver must be capable of driving the MOSFET fast and ensure rapid response time when a short-circuit occurs. For all these reasons, common IGBT drivers cannot be utilized and thus more sophisticated ones must be implemented.

### 2.5. Market Trends of SiC

The past few years SiC devices have steadily gained momentum and credibility in applications where high-power densities and increased efficiency are required. For example,
In the USA, the energy consumption will grow up to 30% by 2040 [33] and with the increasing number of power electronic applications, such as EVs and HEVs, SiC is expected to possess a larger share in the semiconductor market than they currently do.

The most crucial impediment in the wide utilization of SiC devices is their increased market cost compared to Si-based power semiconductors. Since 2001 when the first Schottky diode was introduced, the production cost of SiC diodes from wafers has dropped from $5000/wafer to almost $600/wafer by 2012 [33]. At the same time, the sales of SiC devices have almost tripled since the beginning of 2000s. In addition, Fig. 2.15 represents the price trends of the most common SiC devices since 2012 when the only players in the SiC market were CREE Wolfspeed and Infineon. It is interesting to observe that SiC MOSFET’s price dropped by 50% in 2015 compared to its initial value in 2012. With the distribution of the market share currently growing and more competitors already manufacturing SiC components such as Rohm Semiconductor and ST Microelectronics, the average selling price (ASP) of SiC MOSFET is expected to drop to less than $2,000 by 2025 [2] which could be yielded to the improved quality of SiC wafers.

![Fig. 2.15: SiC devices price trends since 2025 [2]](image)

From an application point of view, the market size of SiC devices is estimated to be more than $500m and expected to reach almost $1.2b by 2022, which can be attributed to the significant price reductions of the devices [34]. Currently, the largest portion of the market is held by Power Factor Correction (PFC) power supply and photovoltaic (PV) inverters possessing almost 80% of the shares as it is estimated by Fig. 2.16. However, the advent of EV and HEV applications is promising and expected to contribute more in the upcoming years with a current annual growth rate (CAGR) raising up to 40% by 2020 [34]. The adoption of SiC power devices will be more apparent after 2020 when the market of xEVs is estimated to rise exponentially. The market size of SiC devices based on several applications is illustrated in Fig. 2.16.
Focusing more on SiC applications in automotive, in Fig. 2.17 a cost comparison is being made for a 60 kW, 3-leg power inverter employed in HEVs and implemented with Si, SiC and GaN power electronics components [35]. The total cost of the inverter implemented with SiC power transistors and diodes is almost 60% higher than its Si counterpart in the 2013 research. By 2020 the overall cost of SiC inverters is expected to decline significantly despite the fact that it will still be higher than Silicon by 19% due its higher manufacturing cost. However, the increase in efficiency, in combination with lower losses and significant reductions in size and volume of the inverter, might justify the additional cost from SiC. Indicatively, SiC power devices almost eliminate the need for water cooling thus allowing for a more compact design.

However, an alternative solution to Si could be the implementation of the inverter with GaN power transistors as, according to Fig. 2.17, the total cost of the converter with GaN is lower than with Si-based transistors by almost 6%. GaN has the WBG advantages that have been mentioned as well as managed to achieve a lower inverter cost. Consequently, it could be a more viable solution than SiC in the specific scenario.
Although a promising technology, the higher cost of SiC devices must be taken into consideration as it might work as an impediment towards the wide implementation of this technology. In applications such as EVs, power switching devices account for almost 50% of the converter’s cost [15] therefore replacing Si with SiC will only make matters worse. Adding to this the low productivity of SiC devices, which will inevitably keep prices high, SiC technology doesn’t appear to be an economic alternative. On the other hand, the advantageous features of SiC will reduce the cost of peripherals such as heat sink and output filters, which in some cases can decrease the cost substantially, thereby bringing a balance to the total inverter cost. Taking all these into consideration, SiC-device prices must be further reduced in order to be regarded as a cost-effective solution for future applications.

2.6. Research on SiC MOSFETs in Automotive

Admittedly, the price liquidity of oil, in combination with its probable unavailability in the future and the need for reducing greenhouse emissions, has driven many automotive companies towards electrified vehicles to replace the conventional fossil fuel engine vehicles. Their gradual introduction to the market, though, reinforced the need to increase their efficiency while, simultaneously, reduce their size and volume which can affect the vehicle’s overall design and operation. Towards this direction, vehicle traction systems will undergo significant changes in the future mainly due to the wide penetration of SiC-based power converters which are expected to satisfy the two aforementioned needs. As a result, the research trend focuses more on the impact of SiC in high-power density vehicle converters.

The inherent features of SiC devices will affect both the efficiency of the converter and the losses of the vehicle’s propulsion system. Even when light-loaded, vehicle’s traction
System efficiency is higher compared to its Si-IGBT counterpart due to the aforementioned performance improvements that SiC technology has achieved on the design and operation of power converters in the vehicles. Indicatively, Ding et al. [36] demonstrated that the overall efficiency of the inverter-motor traction system is distinctively higher when SiC devices are employed reaching almost 99% compared to 96% with Si-IGBTs.

A similar research had the same outcome regarding the significant reduction in converter-motor losses. Fig. 2.18 demonstrates this impact as well as the reduction in losses due to harmonics.

![Fig. 2.18: Loss comparison in converter-motor traction system for Stockholm Metro [37]](image)

According to the results, the replacement of the IGBT converter with a SiC and the subsequent increase in the switching frequency resulted in a total reduction of 34% in motor and converter losses. In addition, the lower cooling requirements from the replacement of IGBTs resulted in a reduction of converter’s volume and weight by 51% and 22%, respectively [37], which clearly demonstrates the potential benefits from SiC-based converters.

Research has also been carried out on inverters and DC-DC converters implemented on actual EVs and HEVs such as the case of Toyota Prius 2010 [15]. In the corresponding research, a bi-directional buck-boost DC-DC converter was implemented similar to the one employed in HEV Toyota Prius 2010. The scope of the research was to employ the same DC-DC converter SiC-based transistor, either MOSFET, JFET or BJT and diodes, and compare its efficiency with the original Si-IGBT converter. Fig. 2.19 demonstrates the percentage (%) of power losses calculated with respect to the IGBT losses as a function of switching frequency. By increasing the switching frequency of the converter, the losses in the SiC transistors are reduced significantly compared to the IGBT converter.
Another interesting aspect on the implementation of SiC converters on HEVs is whether there is a correlation between the efficiency and weight of the converter with the vehicle’s fuel consumption, something that was simulated by Zhang et al. [38]. According to this research, the implementation of an only-SiC inverter in the Toyota Prius 2004 HEV improved the system efficiency up to 15% leading to an improvement in the fuel’s economy from 3.94 L/100 km, when a Si-based inverter was utilized, to 3.36 L/100 km. In addition, a Plug-In Hybrid Electric Vehicle (PHEV) was designed with all-electric operation range of 48 km and increased battery capacity. The result was a 21% increase in the system’s efficiency corresponding to a fuel economy shift from 1.32 L/100 km with Si to 0.96 L/100 km with SiC clearly demonstrating the positive effect of reduced volume and mass of the vehicle’s powertrain on the fuel consumption.

Furthermore, the effect on urban driving was studied by Kim et al. [39] where a vehicle model was simulated and the parameters of Nissan LEAF were incorporated into the scenario. The system was comprised of a DC-AC inverter and a Permanent Magnet (PM) motor and the potential shift from a 600 V to a 1.2 kV inverter was examined. The simulation was able to include the driver’s behavior both during urban and highway driving. The simulation indicated a reduction in urban driving losses by utilizing high voltage motor and inverter and, more importantly, when utilizing SiC-based power electronics.

The applications oriented around EVs and HEVs are endless and the aforementioned cases are some examples of the ongoing research in the field. Similar cases include converter modules of fast electric chargers utilized for PHEVs [40] or even potential changes in the architecture of powertrain and inverters that could be implemented in future vehicles [41] or even on-board battery chargers utilizing SiC power devices [42].
3. **Design Parameters of the DC-DC Converter**

This chapter handles the procedure of designing the DC-DC converter utilized for testing the MOSFETs. It starts with a brief introduction of the main components of an EV and HEV as well as the types of DC-DC converters found in electric vehicles. Subsequently, the design of the corresponding converter parts such as LC filter, heat sink, PWM generation etc. is described together with the components utilized in the final prototype and the assumptions made in the process.

### 3.1. **EV Powertrain Architecture**

Key components of a typical EV powertrain are the electrical machine (EM), power electronic parts, mainly a DC-AC inverter and a DC-DC converter, and the energy storage systems (ESS). The interconnection and interaction of these components is given in Fig. 3.1. The most common types of EMs utilized in electrified vehicles are either permanent magnet (PM) AC machine or induction machine that is common in Tesla models. Another potential solution would be a switched reluctance DC machine which is capable of very high rotating speeds, yet it is rather costly compared to the induction EM [19]. In the case of hybrid vehicles, an internal combustion engine (ICE) is also part of the architecture, however, it is ignored in Fig. 3.1 for simplicity.

The EM is fed by the DC-AC inverter which must allow bi-directional flow of power so that the machine can operate in two modes: as a motor and as a generator. When the machine operates as a motor, the DC voltage is provided by the 650 V battery pack and is converted to AC via the DC-AC inverter that drives the electrical machine. The flow of power follows the red arrows in Fig. 3.1 with direction from the battery pack to the load. In the second operating mode, when the vehicle decelerates, the power flows to the opposite direction causing the machine to operate as a generator. The power flows through the converter, which operates as an AC-DC rectifier, and provides the DC voltage to charge the battery pack. Therefore, the kinetic energy from braking is recovered by the EM, a process called regenerative braking.

The DC-DC converter implemented on Fig. 3.1 is responsible for feeding the 24 V electrical loads such as lights and electronic circuits of the vehicle as well as to charge the 24 V lead-acid batteries based on the orange indicators. The voltage from the 650 V battery pack is stepped-down through the DC-DC converter to a suitable voltage level. The converter also allows bi-directional flow of energy allowing the 24 V battery to discharge through the converter. The advantage of this topology is that the converter can supply the low voltage system even when the engine is not operating, simply by discharging the high-voltage battery. This is even more important for HEVs as the system works regardless of the operating state of the ICE.
In the case of HEVs where an ICE powertrain exists, the vehicle can operate either as fully electrical by discharging the 650 V battery pack or as hybrid where both the ICE and the battery pack will drive the vehicle. The advantage of the hybrid powertrain architecture is that the high voltage battery pack can charge simply by operating the ICE.

### 3.1.1. DC-DC Converter Modules

During the operation of a DC-DC converter module in the EV powertrain, an amount of energy provided by the input source is temporarily stored in the magnetic or electric field of the converter components (inductors, capacitors) and subsequently is released to the output giving a voltage of different level. The amount of power flow is not arbitrary but monitored by adjusting the duty cycle of the topology. Basically, by adjusting the operating time of the power semiconductor devices employed in the converter, the output voltage and current can be controlled and thus the power that is delivered to the connected load. Almost all DC-DC converters can be modelled to offer bi-directional flow of energy between the two voltage levels. The DC-DC converter topology implemented in EV powertrains is sometimes referred as energy management converter [43].

Various converter topologies can be implemented based on their complexity and application requirements. In any case, there are two distinctive groups of DC-DC converters:

- **Non-isolated DC-DC Converters**: which are utilized in cases where electric isolation is not required. In general, this group of converters allow voltage changes in small ratio, otherwise there will be severe stress on the employed switching devices. Common types are the buck, boost, buck-boost, half-bridge, full-bridge and Ćuk DC-DC converters which are normally utilized in low-power applications. Non-isolated type converters can be found in hybrid EVs as the battery pack is not charged by the
electrical grid and therefore the safety precautions imposed in EVs are not required.

- **Isolated DC-DC Converters**: where an isolation transformer is deployed. Normally, these converters can be utilized when the voltage magnitude between DC input and output is some hundreds of volts and electric isolation is required. For instance, isolated converters are employed in EVs so that the battery pack can be protected while connected to the electrical grid. Common types are Flyback, Push-Pull and Forward converter. Due the presence of a transformer, these converters are bulkier and more complex.

For the purpose of this project, a simple non-isolated half-bridge DC-DC converter has been implemented to allow bi-directional flow of energy.

### 3.2. The Half-bridge DC-DC Converter

Apart from its simplicity, the half-bridge DC-DC converter topology offers easy and reliable operation, minimum number of components compared to e.g. the full-bridge topology, cost-effectiveness and high efficiency (which is increased further due to the utilization of SiC MOSFETs). These reasons, along with the lower device stress compared to the rest of the topologies, make the half-bridge converter an ideal candidate for the testing requirements of this project and is currently being implemented in various market available HEVs.

The implemented converter consists of two SiC power MOSFETs, \( T_1 \) and \( T_2 \), which are controlled by a PWM signal that drives the gate of each MOSFET. The two PWM signals must be complementary to each other so that a short-circuit could be avoided as a result of a simultaneous turn-ON of the two MOSFETs [44]. The freewheeling diodes, \( D_1 \) and \( D_2 \), shown in Fig. 3.2 correspond to the body diode of each SiC MOSFET. An LC filter has also been deployed and comprised of an inductor \( L \) and a capacitor \( C_2 \) to reduce the current and voltage ripple, respectively, as well as the total harmonic distortion. The input capacitor \( C_1 \) filters the voltage ripple of the input voltage source. The converter allows bi-directional flow of energy which means that the current can flow on both directions depending on the conduction state of the MOSFETs and the stored energy in the inductor. The half-bridge DC-DC converter circuit model is given in Fig. 3.2 where the four operating states of the MOSFETs are demonstrated.
Fig. 3.2: Half-bridge DC-DC converter model for different current conduction paths

Fig. 3.3: Waveforms for half-bridge DC-DC converter operation
According to the current waveform of Fig. 3.3, in order to describe the operation of the converter, four states are observed depending on the current path and the component that conducts the current [44]. The analysis starts from the state labelled as (1) of Fig. 3.2 where the transistor $T_1$ is ON and the current flows, through the inductor, to the load with a voltage equal to $V_2$. The output current in the last waveform of Fig. 3.3 increases gradually to a maximum value $I_{max}$ due to the energy that is stored in the inductor. When $T_1$ is switched OFF, the current cannot flow from path (1) and finds an alternative path, given by (2), through the body diode, $D_2$, of transistor $T_2$. In the meantime, $T_2$ has been switched ON, according to the second waveform of Fig. 3.3. Throughout this time interval, the energy stored in the inductor is released to the load resulting in a decrease of the current which reaches a zero value by the end of time interval (2) as there is no energy left in the inductance field.

After this time interval, the current is zero and transistor $T_2$ can finally enter into conduction mode marking the beginning of state (3). According to Fig. 3.2 and Fig. 3.3, the output current becomes negative and flows in the loop that is created by $T_2$ and the voltage level $V_2$, as shown in state (3) of Fig. 3.2. The inductor current further decreases to reach a minimum value equal to $I_{min}$ until $T_2$ is switched OFF by the end of the switching period $T_s$. During this time interval, energy is stored again in the electromagnetic field of the inductance. After $T_2$ is switched OFF, $T_1$ is turned ON and the energy from the inductance field is transferred to capacitor $C_1$. The current flows through the path denoted with (4) via the body diode, $D_1$, of transistor $T_1$, until the inductor current reaches the zero value and the whole energy has been released. After this moment, $T_1$ is ready to conduct a positive current again thus restarting state (1). Based on the fact that the average inductor voltage is equal to zero for a switching period, and considering the third waveform of Fig. 3.3, the voltage $V_2$ can be calculated via the equation:

$$V_2 = D \cdot V_1$$  \hspace{1cm} (3.1)

From eq. (3.1), $D$ is the duty cycle of transistor $T_1$ which correspond to the amount of time that $T_1$ is conducting in relation with the switching period. In addition, based on the location of the minimum and maximum inductor current, $I_{min}$ and $I_{max}$ respectively, the average output current can be either positive or negative. The following paragraph will focus on the design process of this DC-DC converter including the relevant parts that are demonstrated in Fig. 3.2.

### 3.3. Converter Design

The design process of the utilized DC-DC converter includes all the relevant components from the LC filter to PWM generator based on certain assumptions for optimal converter operation. The design considerations and the list of the components utilized in the converter are given in Table 3.1 and Table 3.2, respectively.
Table 3.1: DC-DC converter design considerations

<table>
<thead>
<tr>
<th>Design Assumptions</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage $V_1$</td>
<td>50 – 200 V</td>
</tr>
<tr>
<td>Output Voltage $V_2$</td>
<td>24 V</td>
</tr>
<tr>
<td>Switching Frequency $f_s$</td>
<td>80 kHz</td>
</tr>
<tr>
<td>Maximum Load Current $I_{o,\text{max}}$</td>
<td>20 A</td>
</tr>
<tr>
<td>Input Voltage Ripple $\Delta V_{1,pp}$</td>
<td>0.2 V</td>
</tr>
<tr>
<td>Output Voltage Ripple $\Delta V_{2,\text{max}}$</td>
<td>0.1 V</td>
</tr>
<tr>
<td>Inductor Current Ripple $\Delta i_{L,\text{ripple,max}}$</td>
<td>1 A</td>
</tr>
<tr>
<td>Maximum Ambient Temperature $T_{a,\text{max}}$</td>
<td>50 °C</td>
</tr>
<tr>
<td>Maximum Junction Temperature (Type 1 &amp; 2 MOSFETs) $T_{j,\text{max}}$</td>
<td>150 °C, 200 °C</td>
</tr>
<tr>
<td>PDMS Insulator Thermal Resistance $R_{th,cs}$</td>
<td>0.18 $\text{W/}°\text{C}$</td>
</tr>
</tbody>
</table>

Table 3.2: List of components utilized in half-bridge DC-DC converter

<table>
<thead>
<tr>
<th>Component</th>
<th>Model</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiC MOSFETs, $T_1$, $T_2$</td>
<td>Supplier A, Type 1 MOSFET, Supplier B, Type 2 MOSFET</td>
</tr>
<tr>
<td>Input Capacitor $C_1$</td>
<td>4 x 300 μF Suncon Aluminum Electrolytic Capacitor, 100 V,</td>
</tr>
<tr>
<td></td>
<td>3 x 10 nF Ceramic Capacitor, 200 V</td>
</tr>
<tr>
<td>Output Capacitor $C_2$</td>
<td>1 x 47 μF Suncon Aluminum Electrolytic Capacitor, 50 V</td>
</tr>
<tr>
<td>Inductor $L$</td>
<td>SMP Custom Made Inductor, 300 μH, 300 V</td>
</tr>
<tr>
<td>PWM Generator</td>
<td>Arduino MEGA 2560</td>
</tr>
<tr>
<td>Gate Driver IC</td>
<td>Infineon Half-Bridge Driver IR211</td>
</tr>
<tr>
<td>Gate Driver Diode</td>
<td>1N5819 1A Schottky Diode, 40 V</td>
</tr>
<tr>
<td>Driver Input Capacitor</td>
<td>1 x 4.7 μF Folie Polypropylene, 1 x 470 nF Ceramic Capacitor</td>
</tr>
<tr>
<td>Driver Bootstrap Capacitor</td>
<td>1 x 470 nF Folie Polypropylene, 1 x 47 nF Ceramic Capacitor</td>
</tr>
<tr>
<td>Common Emitter Circuit BJT</td>
<td>BC546 Small Signal NPN Amplifier Transistor, 65 V</td>
</tr>
<tr>
<td>Common Emitter Circuit Diode</td>
<td>1N4148, Small Signal Switching Diode, 100 V</td>
</tr>
<tr>
<td>Common Emitter Circuit Capacitor</td>
<td>1 x 1 nF Ceramic Capacitor</td>
</tr>
</tbody>
</table>
3.3.1. PWM Generation & Voltage Controller

For a given input voltage, the output voltage of a DC-DC converter is controlled by monitoring the $t_{ON}$ and $t_{OFF}$ duration times of the switch. The method utilized in this case, which requires constant frequency operation, adjusts the switching times of the employed MOSFETs and is commonly known as pulse-width modulation (PWM). A PWM signal can be generated by comparing a constant voltage control signal $u_{control}$ with a repetitive sawtooth signal $u_{st}$ of frequency equal to the switching frequency of the converter. It is also common that the generated control voltage is the amplified error of the difference between the actual, $V_{o, actual}$, and the given reference voltage, $V_{o, ref}$. In any case, the control voltage varies slowly in relation to the high frequency sawtooth signal allowing the comparison between the two. Therefore, when $u_{control}$ is greater than $u_{st}$, the switch control signal becomes high resulting in conduction of the MOSFET. Otherwise, the control signal is set low. The duty cycle $D$ that is utilized is the ratio of the period that MOSFET $T_1$ is switched ON. Fig. 3.4 and Fig. 3.5 give the block diagram and waveform comparison for the PWM signal generation, respectively.

![PWM signal generation diagram](image)

**Fig. 3.4: PWM signal generation diagram [4]**

![Waveform comparison diagram](image)

**Fig. 3.5: Waveform comparison between sawtooth signal carrier $u_{st}$ and constant voltage $u_{control}$ [4]**

The approach that was followed in this project is more simplified compared to the aforementioned description, although it is based on the PWM signal theory. The PWM signal
is generated by an Arduino MEGA 2560 platform that utilizes the library “PWM.h” that is available in the Arduino community. This library exploits the available Arduino timers to produce a PWM signal of frequencies up to 100 kHZ. Based on the library script, the program allows the specification of the switching frequency as well as the duty cycle of the PWM signal based on the input and output voltages.

Apart from the basic function of the “PWM.h” script, the implemented code has been extended in order to allow for a voltage control operation. The Arduino is able to sense the output voltage that is divided by means of a voltage divider and compared with a predefined reference value given in the core script. Subsequently, based on the difference between the output and reference voltage, the Arduino increases or decreases the duty cycle of the PWM signal resulting in an output voltage close to the reference value given. Fig. 3.6 shows the produced PWM signal with a duty cycle $D = 0.5$.

![PWM signal generated by Arduino MEGA 2560](image)

Apart from the main PWM circuit that consists of the Arduino platform, an additional common emitter BJT circuit is implemented to work as a voltage amplifier. The PWM signal varies between 0 and 5 V which is not high enough to drive effectively the SiC MOSFETs of the converter. Therefore, the generated PWM signal is directed on a BJT transistor circuit that is fed by a voltage $V_{cc}$ and the signal is applied on its gate. When the gate is kept to zero voltage, the output is equal to $V_{cc}$, whilst when the gate is at 5 V, the BJT allows the flow of current leading to an almost zero voltage at the collector of the BJT. As a consequence, the common emitter circuit amplified the voltage of the PWM signal in a level that is suitable to drive the SiC MOSFETs. The schematic for the common emitter circuit that was designed for this purpose is given in Fig. 3.7.
The signal is then fed to the gate driver circuit as shown in Fig. 3.7 which produces two identical and complementary PWM signals in order to drive the MOSFETs of the half-bridge converter. The signals’ amplitude varies between 0 $V$ and $V_{cc}$ which is the input voltage of the driver. In the prototype, $V_{cc} = 20 V$ and the PWM signals are shown in Fig. 3.8 for $D = 0.5$. The advantage of the IR2111 gate driver is that it introduces a delay between the two PWM signals meaning that when a MOSFET is switched OFF, there is a time interval of some nanoseconds before the other one is turned ON thus eliminating a potential short circuit in the converter.
3.3.2. LC Filter

This section analyzes the design of the inductor \( L \) and the capacitor \( C \) of the converter's LC filter. The magnitude of the inductor determines the slew rate of the current indicating that higher inductance leads to lower current ripple. A small inductor size, although allows for faster transient response in the circuit, but increases the current ripple. As the requirement is to design a high-efficiency converter, the magnitude of the inductance is chosen rather large in order to achieve as low current ripple as possible. The low current ripple is also compelled by the connected load which is assumed to be a 24 V battery, according to Fig. 3.1. Moreover, the high saturation current required for the circuit justifies its rather large size.

On the contrary, the capacitor provides a path for the harmonic currents while the dc component flows through the load. Generally, the filter capacitor is responsible for reducing the output voltage ripple and overshoot which otherwise would have caused damage to the connected load. Furthermore, an important requirement for the capacitor is the low equivalent-series resistance (ESR) in order to minimize losses and increase the efficiency of the overall design.

3.3.2.1. Inductor \( L \)

For the design of the inductor, the voltage-drop in the MOSFET when conducting is too small compared to the magnitude of the input and output voltage and therefore it will be ignored, assuming ideal switching transistors. For the magnitude of the inductance, the desired current ripple will be taken into consideration assuming that when the converter operates at \( V_1 = 200 V \) and \( V_2 = 24 V \) the inductor current will be zero by the end of each switching period. This way, the converter will give the maximum current ripple as the peak of the triangular current will have its maximum value and maximum power will be transferred between input and output. The condition under which the inductor was designed is given approximately in Fig. 3.9. When the converter operates with maximum ripple, only 2 states are observed in comparison with Fig. 3.3.

![Fig. 3.9: Maximum current ripple of half-bridge DC-DC converter](image-url)
The duty ratio is defined when MOSFET $T_1$ is conducting during each switching period which is written:

$$ D = \frac{t_{ON}}{T_s} = \frac{V_2}{V_1} $$

(3.2)

where $t_{ON}$ is the conducting time of $T_1$ and $T_s$ is the switching period. Performing simple circuit analysis and assuming that the output voltage is always constant and equal to $V_2$ the inductor current is calculated by the differential equation:

$$ L \frac{di_L}{dt} = V_1 - V_2 $$

(3.3)

Therefore, assuming steady state operation and that the initial current in the inductor is non-zero, i.e. $i_L(0) = I_{L,\text{min}}$, $i_L(t)$ for the time interval $0 \leq t \leq DT_s$ is calculated by integrating eq. (3.3):

$$ i_L(t) = \frac{V_1 - V_2}{L} t + I_{L,\text{min}} $$

(3.4)

From eq. (3.4), it is clear that the inductor current is increasing linearly to its maximum value, $I_{L,\text{max}}$ which is the high-peak current and is given when $t = DT_s$. Therefore, the peak-to-peak current which defines the current ripple $\Delta i_{L,\text{ripple}}$ of the inductor is given by eq. (3.5):

$$ \Delta i_{L,\text{ripple}} = I_{L,\text{max}} - I_{L,\text{min}} = \frac{V_1 - V_2}{L} DT_s \overset{\text{eq.(3.1)}}{=} $$

(3.5)

$$ \Delta i_{L,\text{ripple}} = \frac{V_2}{L} (1 - D)T_s $$

The same result yields when the differential equation for the inductor current is solved for the time interval $DT_s \leq t \leq T_s$ where the current decreases from its peak to a minimum value, according to the equations below:

$$ L \frac{di_L}{dt} = -V_2 \implies i_L(t) - I_{L,\text{max}} = \frac{-V_2}{L} (t - DT_s) \overset{t=T_s}{=} $$

(3.6)

$$ \Delta i_{L,\text{ripple}} = I_{L,\text{max}} - I_{L,\text{min}} = \frac{V_2}{L} (1 - D)T_s $$

Based on the assumption for the maximum current ripple in the inductor given in Table 3.1, the minimum inductance is specified based on the mentioned operating condition where the duty ratio, $D$, takes its minimum value, $D_{\text{min}}$.
The inductance utilized in the half-bridge DC-DC converter fulfills all the necessary requirements for both operating modes. The calculated value is given on Table 3.2.

3.3.2.2. DC Capacitor $C_2$

Throughout the inductor design process, it was assumed that the output capacitor $C_2$ was so large that the output voltage, $V_2$, remained constant. In theory, the capacitance should be infinite in order to have a pure DC voltage in the output. In practice, the capacitor should be selected large enough in order to ensure as small voltage ripple as possible. The capacitor was selected based on the maximum voltage ripple of the half-bridge DC-DC converter and considering the operating condition of Fig. 3.9.

Assuming that the ripple component of the inductor current $i_L$ flows through the output capacitor while the DC average current $I_L = I_o$ through the load, the peak-to-peak output voltage ripple, $\Delta V_2$, can be calculated from the inductor current waveform considering that any variation from the average value in the inductor current causes additional charge in the capacitor showed by eq. (3.8):

$$\Delta V_2 = \frac{\Delta Q}{C_2} = \frac{1}{C_2} \frac{1}{2} \frac{\Delta I_L T_s}{2}$$

(3.8)

Taking into consideration eq. (3.6) for the inductor current ripple as well as the requirement for maximum allowed voltage ripple in the load, $\Delta V_{z,max}$, the minimum output capacitor, $C_{2,min}$, is calculated below:

$$C_{2,min} = \frac{1}{8 \Delta V_{z,max}} \frac{V_2}{L} (1 - D) T_s^2$$

(3.9)

The inductance, $L$, is the calculated value of the as demonstrated in the previous subsection.

3.3.3. Input Capacitor $C_1$

The EMI issue cannot be ignored when designing a half-bridge DC-DC converter and is attributed to the pulsating ripple current that is generated in the input during operation. Another source of EMI is the resistance and inductance introduced by the printed circuit board (PCB) which causes high-voltage ripple that can disrupt the normal operating condition of other electronic circuits utilized in the converter module. In order to deal with this problem and reduce
the input current and voltage ripple as much as possible, input capacitors were utilized to stabilize the voltage and reduce this current ripple by providing an alternative path through the capacitors.

Initially, the capacitor should be chosen in order to be able to withstand the operating input voltage range without risking the reliable operation of the converter. The requirement for low ESR applies in this case as well, otherwise the ripple and capacitor size would have been significantly higher. An estimate for the input capacitance size is given by eq. (3.10) [45]:

$$C_{in} \geq \frac{D(1-D)I_o}{\Delta V_{1,pp}f_s}$$  \hspace{1cm} (3.10)

The value of the input capacitance is calculated for the case where the duty cycle is maximum by, also, taking into consideration the aforementioned requirements. Apart from the voltage ripple, the capacitor must be able to withstand the thermal stress that might occur. In other words, it should be able to operate normally with the maximum RMS input ripple current, according to eq. (3.11) [45]:

$$I_{in,rms,\text{max}} = I_o \sqrt{D(1-D) + \frac{1}{12} \left( \frac{V_2}{L_fI_o} \right)^2 \left( 1 - D \right)^2 D}$$  \hspace{1cm} (3.11)

In order to reduce the ESR of the capacitor bank as much as possible, various capacitors connected in parallel were utilized. In addition, smaller ceramic capacitors were also incorporated in the final prototype to reduce phase-node ringing without affecting the overall efficiency of the designed converter.

### 3.3.4. Heat Sink & Cooling System

Thermal management has proven to be the most crucial element in the DC-DC converter design as removing the heat from the system can be quite a challenging task. During normal operation, the electronic components’ temperature can increase significantly especially when power transfer is high, which can lead to reduced life expectancy, decreased reliability and sometimes permanent damage of the components. The employment of a heat sink is a rather cost-effective solution with minimum design impact on the converter which can dissipate the generated heat effectively thus maintaining the device temperature well below its operating limit. In order to achieve this, a conduction path must be provided so that the heat can be transferred from the power device to the ambient.

The goal for the heat sink design is to keep the junction temperature, $T_j$, of the SiC MOSFET within reasonable levels by accounting for the maximum power losses generated from its operation. For this purpose, the worst-case scenario was considered where the
converter operates at maximum current and voltage whilst the maximum junction temperature of the MOSFET, \( T_{j,\text{max}} \), and the maximum ambient temperature, \( T_{a,\text{max}} \), were utilized. Furthermore, the maximum conduction and switching losses of the MOSFET, the body diode losses and reverse recovery losses were accounted by considering the duty ratio, ON-state resistance, current and reverse recovery charge. The maximum junction-to-ambient thermal resistance, \( R_{\theta,ja} \), is given by eq. (3.12):

\[
R_{\theta,ja} = \frac{T_{j,\text{max}} - T_{a,\text{max}}}{P_{\text{loss}}}
\]  

(3.12)

\( P_{\text{loss}} \) are the total losses during the operation of the converter. \( R_{\theta,ja} \) consists of the elements given by Fig. 3.10 and eq. (3.13). \( R_{\theta,jc} \) is the junction-to-case thermal resistance which is specified by the MOSFET manufacturer, \( R_{\theta,cs} \) is the case-to-sink thermal resistance defined by the insulator utilized and \( R_{\theta,sa} \), is the thermal resistance between heat sink and ambient. In order to maximize the heat dissipation capability of the system for the worst-case scenario, \( R_{\theta,cs} \) and \( R_{\theta,sa} \) must be minimized.

\[
R_{\theta,ja} = R_{\theta,jc} + R_{\theta,cs} + R_{\theta,sa}
\]  

(3.13)

![Thermal resistance diagram for heat conduction path](image)

Fig. 3.10: Thermal resistance diagram for heat conduction path [46]

The first step towards the heat sink design is the calculation of power losses for the worst-case scenario. In both operating conditions of the converter, when \( V_1 = 50 \, V \) and \( V_1 = 200 \, V \), the energy flows with a direction from the input to the output. This conclusion is drawn by the LC filter design assumption of Fig. 3.9 where it was assumed that at \( V_1 = 200 \, V \) the current ripple was maximum. In that case, the inductor current was set zero after a time interval equal to \( t_{T_2,\text{on}} \) which correspond to the time when \( T_2 \) was ON. When the input voltage decreases, the duration that \( T_1 \) is switched ON increases and thus the duration that \( T_2 \) is ON
is decreased. Therefore, the inductor current cannot be set zero, but rather reaches a minimum non-zero value. As a consequence, only the body diode, $D'_2$, of $T_2$ conducts the current for both input voltages.

As far as the calculation of losses, the conduction $P_{cond}$ and the switching losses $P_{sw}$ of SiC MOSFET $T_1$ were considered for the duration that the transistor was switched ON. When $T_1$ was OFF, the body diode of $T_2$ conducts the current and therefore the diode forward and the reverse recovery losses were accounted.

Considering the ON-state resistance of the SiC MOSFET, $R_{ds,ON}$, the instantaneous voltage, $u_D(t)$ and the ON-state current, $i_D(t)$, the average conduction losses were calculated by integrating the instantaneous power losses over a switching cycle according to eq. (3.14):

$$ P_{cond} = \frac{1}{T_s} \int_0^{T_s} u_D(t) \cdot i_D(t) dt = \frac{1}{T_s} \int_0^{T_s} R_{ds,ON} \cdot i_D^2(t) dt = R_{ds,ON} \cdot I_{D,rms,T_1}^2 \quad (3.14) $$

The RMS value of the MOSFET current, $I_{D,rms}$ varies depending on the $T_1$ conduction duration time. eq. (3.14) gives a general formula for the calculation of conduction losses, while eq. (3.2) gives the duration that $T_1$ is conducting the current. Combining these two equations, the value of current in eq. (3.14) is calculated as:

$$ I_{D,rms,T_1} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_D^2(t) dt} = \sqrt{\frac{1}{T_s} \int_0^{T_s} i_D^2(t) dt} = \sqrt{D} \cdot I_0 \quad (3.15) $$

For the estimation of the switching losses, the analytical method was utilized because it presents the worst-case scenario for the calculations. Details of the analytical method are given by Infineon et al. [47] and is strongly based on the switching-ON transient of the SiC MOSFET. Specifically, in order for a MOSFET to start conducting, the gate-to-source voltage must reach the threshold value, $V_{gs,th}$, with a time constant that depends on the gate resistor, $R_g$, and the MOSFET input capacitance, $C_{iss}$. Once $V_{gs}$ has reached the Miller plateau voltage, $V_{plateau}$, it is clamped on this value and the drain-to-source voltage, $U_{DS}$, starts to fall with a slope that is dictated by the gate current that flows through the gate-drain capacitance, $C_{GD}$. The overall time required for the voltage to fall depends on the non-linearity of the $C_{GD}$ which is considered in order to calculate the losses more accurately. A two-point method approximation is utilized assuming a linear drop of $U_{DS}$ which presents the worst-case analysis for the losses.

The fall time, $t_{fu}$, of the voltage is given by eq. (3.16) – (3.18):
\[ t_{fu} = \frac{t_{fu1} + t_{fu2}}{2} \]  

(3.16)

where:

\[ t_{fu1} = (V_{DS} - R_{ds,ON} I_D) R_g \frac{C_{GD1}}{V_{Dr} - V_{plateau}} \]  

(3.17)

\[ t_{fu2} = (V_{DS} - R_{ds,ON} I_D) R_g \frac{C_{GD2}}{V_{Dr} - V_{plateau}} \]  

(3.18)

The values of \( C_{GD1} \) and \( C_{GD2} \) are the gate-drain capacitance values as taken from the corresponding manufacturer’s waveform for the two-point approximation method. \( R_g \) is the internal gate resistor of the MOSFET taken from the datasheet and \( V_{Dr} \) is the applied gate-to-source voltage. In a similar manner, the rise time, \( t_{ru} \), of the voltage is given by eq. (3.19) – (3.21):

\[ t_{ru} = \frac{t_{ru1} + t_{ru2}}{2} \]  

(3.19)

where:

\[ t_{ru1} = (V_{DS} - R_{ds,ON} I_D) R_g \frac{C_{GD1}}{V_{plateau}} \]  

(3.20)

\[ t_{ru2} = (V_{DS} - R_{ds,ON} I_D) R_g \frac{C_{GD2}}{V_{plateau}} \]  

(3.21)

Taking all the above into consideration, the turn-ON and turn-OFF energy losses in the MOSFET, \( E_{ON} \) and \( E_{OFF} \), respectively, are calculated:

\[ E_{ON} = \int_0^{t_{ri} + t_{fu}} u_{DS}(t) \cdot i_D(t) dt = V_{DS} I_D \frac{t_{ri} + t_{fu}}{2} \]  

(3.22)

\[ E_{off} = \int_0^{t_{ff} + t_{ru}} u_{DS}(t) \cdot i_D(t) dt = V_{DS} I_D \frac{t_{ff} + t_{ru}}{2} \]  

(3.23)
From eq. (3.22) – (3.23), the rise and fall times of the current, $t_{rr}$ and $t_{fl}$ respectively were obtained from the SiC MOSFET datasheet. Therefore, the overall switching losses of each MOSFET is calculated by eq. (3.24):

$$P_{sw} = (E_{ON} + E_{OFF}) \cdot f_s$$

(3.24)

As far as the diode forward losses, $P_{diode}$, is concerned, the voltage drop across the diode when conducting, $V_{SD}$, as well as the continuous current flowing through the diode, $i_s(t)$ are considered. In a similar manner with the MOSFET conduction losses, the average diode conduction losses are calculated by integrating the instantaneous power losses over a switching cycle:

$$P_{diode} = \frac{1}{T_s} \int_0^{T_s} u_{SD}(t) \cdot i_s(t) dt = \frac{1}{T_s} \int_0^{T_s} V_{SD} \cdot i_s(t) dt = V_{SD} \cdot I_{dio,av}$$

(3.25)

The average current flowing through the diode, $I_{dio,av}$, was calculated by considering the duration that is forward bias. If the time that $T_s$ is conducting is given by eq. (3.2), then the diode conducts for the rest of the switching period. Considering this assumption, the average diode forward current is calculated by eq. (3.26):

$$I_{dio,av} = \frac{1}{T_s} \int_0^{T_s} i_s(t) dt = \frac{1}{T_s} \int_0^{T_s} i_s(t) dt = (1 - D) \cdot I_o$$

(3.26)

Finally, the reverse recovery losses, $P_{rr}$, in the diode must be considered as well when the converter is operating. To calculate these losses, the reverse recovery charge, $Q_{rr}$, and the voltage across the diode during the reverse recovery, $V_{orr}$, were considered. For the worst-case scenario considered, $V_{orr}$ is equal to the supply voltage of the converter i.e. the input voltage $V_1$. Considering all the above, the reverse recovery energy of the diode, $E_{onD}$, and the corresponding losses are calculated by eq. (3.27) and eq. (3.28), respectively [47]:

$$E_{onD} = \frac{1}{4} Q_{rr} V_1$$

(3.27)

$$P_{rr} = E_{onD} \cdot f_s$$

(3.28)

The next step is to define the sink-to-ambient thermal resistance, $R_{θ,sA}$, which will dictate the heat sink capability of dissipating the power. A combination of eq. (3.12) – (3.13) will give the maximum value of this thermal resistance that should not be surpassed. The value of junction-to-case thermal resistance, $R_{θ,jc}$, was obtained from the manufacturer’s datasheet.
in order to calculate the case temperature, \( T_c \) for each of the two MOSFETs:

\[
T_{c,T_1} = T_{j,max} - R_{\theta,jc} P_{\text{loss},T_1} \tag{3.29}
\]

\[
T_{c,T_2} = T_{j,max} - R_{\theta,jc} P_{\text{loss},T_2} \tag{3.30}
\]

Where:

\[
P_{\text{loss},T_1} = P_{\text{cond}} + P_{\text{sw}} \tag{3.31}
\]

\[
P_{\text{loss},T_2} = P_{\text{diode}} + P_{\text{rr}} \tag{3.32}
\]

From eq. (3.29) and eq. (3.30), it is clear that \( T_c \) is different for the two power MOSFETs and is mostly determined by the time that each MOSFET conducts. Therefore, for the design of the heat sink, the lowest value of the two calculated case temperatures, \( T_{c,T_1} \) and \( T_{c,T_2} \), is taken because otherwise it will result in a larger value of \( R_{\theta,sa} \) that could potentially damage the MOSFET.

As a proper insulating material, polydimethylsiloxane (PDMS) was selected due to its very low thermal conductivity at temperatures around 80°C [48]. The case-to-sink thermal resistance, \( R_{\theta,cs} \), is given in Table 3.1. In eq. (3.33), \( P_{\text{loss}} \) correspond to the losses that have given the minimum case temperature, \( T_{c,\text{min}} \). Utilizing this material will give a sink temperature \( T_s \) equal to:

\[
T_s = T_{c,\text{min}} - R_{\theta,cs} \cdot P_{\text{loss}} \tag{3.33}
\]

Considering eq. (3.29) – (3.33), the maximum value of \( R_{\theta,sa} \) is given by eq. (3.34):

\[
R_{\theta,sa,\text{max}} = \frac{T_s - T_{a,\text{max}}}{P_{\text{loss}}} \tag{3.34}
\]

The design of a simple passive heat sink such as the one mentioned above is an easy task offering significant advantages such as reduced cost and wide availability in terms of their thermal resistance as their surface area can be large enough to transfer the heat to the ambient. On the contrary, when very low thermal resistances are required, their reduced power dissipation capability as well as their potential size and volume might work as an impediment in their utilization. For this purpose, a fan was installed in the overall circuit to provide necessary cooling both to the MOSFETs as well as in the overall converter circuit.
4. Simulation & Prototype Analysis

Chapter 4 deals with the simulation results and the prototype manufacture. The 1\textsuperscript{st} part deals with the prototype utilized in the testing procedure, presents figures of the actual topology and explains the design considerations in EAGLE CAD. The 2\textsuperscript{nd} part presents the simulation results of the converter’s performance and gives an estimation of the switching and conduction losses along with efficiency measurements. Finally, the results from the utilization of the prototype are presented and compared with simulations.

4.1. Prototype Development

The prototype development is divided into two parts: the design of the printed circuit board (PCB) and the corresponding assembly (PCBA) based on the schematic. The design of the PCB was implemented in Autodesk’s EAGLE CAD PCB Design & Schematic Software which contains a variety of schematic and PCB layout editing tools and available libraries. The software facilitates the design of the circuit’s schematics and allows the user to utilize the wide selection of libraries that contain common electronic components or more sophisticated integrated circuits (ICs). In the case of ICs, components are represented exactly as they are manufactured making EAGLE a user-friendly software.

The PCB schematic and layout were created simultaneously and the components were automatically added on the layout avoiding any inconsistencies. Furthermore, the connections defined in the schematic were automatically added to the layout based on the auto-routing feature of connecting traces. The PCB layout can either be double or single-layered depending on the circuit. Moreover, the software contains features for changing the width of traces, adding pads or holes for drilling in order to avoid contact between the PCB and other objects. Considering the routing, EAGLE, through basic PCB design rules, can cross-check the implemented design for potential errors that might lead to nonfunctional PCB designs.

The implemented prototype was designed as a single-layered PCB for simplicity. The width of the traces was defined by the formulas utilized in IPC-2221, the copper thickness and the maximum current that flows through each trace. The design was checked by EAGLE for possible errors during the routing procedure in order to ensure that no traces were connected in a way that could cause short-circuits.

An important feature of the PCB design was the creation of a common ground plane which is a large area of copper that is connected to the ground point of the circuit and serves as return path for the current. One of the advantages of implementing the ground plane is the simplicity of connecting various traces to the ground resulting in a much easier circuit layout. However, the most important one is that the large area of copper returns current from all
components without inducing any significant voltage drops thus ensuring that all components have a common reference potential.

In the main converter topology of Fig. 4.1, two different ground planes separating the analog from the digital ground, i.e. the Arduino ground, had been implemented. The main reason for this separation is obvious: the split grounds prevent the current from one side to decouple with current from the other side thus eliminating a potential ground loop. A thin trace is normally utilized in order to connect the two ground planes to ensure reduced noise and interference from adjacent circuits. The connection point between the two ground planes can be found in the bottom left corner of Fig. 4.1. Furthermore, a power plane has been added to the final prototype to distribute the power from the voltage input to the respective components.

Some parts of the main PCB circuit such as the Arduino input pins, the fan connecting point as well as the input and output ports are highlighted. For the connection of MOSFETs, soldered pins were utilized as it allows the removal of the MOSFETs after electrical testing. Both the fan and the Arduino were mounted on the main PCB, while the MOSFETs were connected to the respective pins and mounted to the heat sink. The design followed the guidelines described in Chapter 3.

Fig. 4.1: Half-bridge DC-DC converter PCB circuit
An additional PCBA was designed for operating the fan. The fan circuit was fed directly from the 20 V input of the main circuit that is used for the gate driver operation and the common emitter circuit, as presented in Fig. 4.1. It is composed by a compact DC-DC converter of specific input and output voltages operating to feed the fan and two capacitors, in the input and output, respectively, that reduce the voltage ripple. Fig. 4.2 shows the PCBA circuit for the fan which was designed based on the pin allocation defined by the supplier.

![Fan PCB circuit](image)

**Fig. 4.2: Fan PCB circuit**

### 4.2. Simulation Results & Prototype Performance

In order to simulate the half-bridge DC-DC converter topology before implementing the prototype, the PLECS Standalone product from Plexim Electrical Engineering software was utilized. PLECS is an ideal tool for high-speed simulation of power electronics systems as it offers an efficient approach to simulating and modelling with a variety of available libraries. Among the most common utilized ones, the active components library uses a simplified semiconductor model that is based on the ideal switch. However, the user can incorporate the manufacturer’s information or experimental measurements in order to emulate the actual semiconductor behavior and calculate switching and conduction losses. Passive components such as capacitors and inductors are also supported by the corresponding library that can model their non-ideal and parasitic characteristics.

The desired voltage control could be implemented by the control schemes that the software supports, such as error amplifiers, comparators and PID controllers offering a stable and robust system. The thermal behavior of the converter could also be simulated. The software is capable of providing a cooling solution for each application and simulate the
behavior of the semiconductor with regard to temperature. As a result, a broader scope of the semiconductor’s capabilities and operating conditions with respect to temperature could be presented.

The PLECS model has incorporated the MOSFET characteristics that correspond to the Supplier B’s SiC modules mainly due to their availability and compatibility with the software but also because no PLECS model existed for Supplier A’s SiC MOSFET due to its unavailability to the market. In addition, a voltage control loop was designed only for simulation purposes as, in the prototype, the voltage control is implemented by the Arduino code.

The presented results are given for the 50 V operating mode as it was mainly utilized for testing. The graphs give the operation of the converter both for non-regulated and regulated output voltage. It is also worth mentioning that, as of this point, only the buck operating mode of the converter will be taken into consideration as it is the main focus in the test results presented in Chapter 5.

### 4.2.1. Output Voltage & Inductor Current

In an ideal DC-DC converter, the output voltage is calculated from eq. (3.1) assuming zero voltage drop in the transistors when switched ON and constant duty cycle. In reality, however, due to the ON-state resistance of the MOSFETs, a voltage drop occurs resulting in lower output voltage compared to the ideally calculated value. In addition, the parasitic series resistance of both the inductor and capacitor in the prototype causes additional voltage drop which results in even lower output voltage. Although the latter assumption was ignored in the simulation, it is clear that, from Fig. 4.3, when the duty cycle of the MOSFETs is kept constant and equal to the calculated value, the output voltage is lower than the desired value.

In order to ensure fast charge rate for the battery, a constant voltage equal to the nominal value is expected. To meet this requirement, a voltage control loop was designed which regulates the duty cycle of the PWM signal based on the reference output voltage of 24 V allowing for a fully automated converter operation. Conceptually, the voltage control loop compares the output and the reference voltage which is directed to an error compensator. The produced signal is then compared with a sawtooth signal in the same manner as Fig. 3.4 with the exception that the duty cycle is regulated so that the output voltage can reach the reference. Fig. 4.3 gives the block diagram for the implemented voltage control loop in PLECS.
Fig. 4.3: Voltage control loop block diagram in PLECS

Fig. 4.4: Output voltage for uncontrolled voltage simulation

Fig. 4.5: Output voltage for controlled voltage simulation
Fig. 4.4 and Fig. 4.5 compare the output voltage waveforms of the two discussed operating conditions for two switching periods. The controller manages to maintain the voltage at a mean value of 24 V compared to the 22,945 V that is achieved in the uncontrolled case where the duty cycle is kept constant. By adjusting the voltage reference value, the controller will balance in a new steady state.

For the inductor, the desired current value is 20 A, assuming a simple ohmic load, which was achieved in the second case, while in the first case the mean value was around 19.108 A. Fig. 4.6 and Fig. 4.7 give the inductor current over a two-period switching cycle. In the uncontrolled voltage case, the maximum current is lower than the desired 20 A current in the load, whilst, in the second case, the required value was achieved. With regard to the simulation results, the prototype managed to operate effectively in collaboration with the voltage control.

![Fig. 4.6: Inductor current for uncontrolled voltage simulation](image-url)
Fig. 4.8 gives the output voltage as measured from the DC-DC converter prototype for Supplier B’s SiC MOSFETs. Observing Fig. 4.8, a voltage overshoot of around 7 V from the average value occurred periodically and appeared in the output voltage. A possible explanation for this overshoot is the fast switching of MOSFET $T_1$ in each period which causes the voltage to overshoot. On the other hand, as the body diode of MOSFET $T_2$ conducts, no overshoot is observed in the output voltage that could be attributed to the switching of $T_2$. In addition, Fig. 4.9 zooms in the output voltage waveform where EMI is obvious. The aforementioned EMI sources as well as the electronic load components affect the output voltage by introducing additional noise to the waveform. Even though, the output voltage is close to the reference 24 V.
Fig. 4.8: Prototype output voltage

Fig. 4.9: Parasitics in the output voltage waveform

As far as the inductor current is concerned, Fig. 4.10 shows the output current of the converter for a 10 A load test. The voltage control loop utilization has increased the current as well which now has an average value of 9.9 A. In a similar manner as the output voltage, parasitics appear in the inductor current as well due to EMI and noise from the adjacent circuits as shown as well in Fig. 4.11. Regardless of that, the current ripple is around 0.6 A peak-to-peak which is well below the specifications of Table 3.1.
4.2.2. Converter Losses

The difference between simulation results and prototype testing is demonstrated in the total converter losses regarding each case due to the assumptions and the method utilized for their calculation in PLECS. Mainly, the conduction and switching losses in PLECS are calculated through linear interpolation and extrapolation based on the data given in a lookup table. The assumption that the change in switching ON and OFF energy is linear introduces an overall error which is obvious when comparing simulation and test results. In addition, it is impossible to simulate the voltage and current transient phenomena during MOSFET switching which also contribute to the switching losses. As far as the conduction losses are concerned, PLECS assumes a constant ON-state resistance without considering its dependency from the junction temperature of the transistor. Besides this, the designed topology does not take into consideration the capacitor’s and inductor’s series resistance which can be a significant source of losses, especially when the load current is high.

Therefore, in order to highlight the various loss sources that exist when operating the test prototype, Fig. 4.12 makes a comparison between the total converter losses as calculated from the test prototype and the software for three different load currents: 5 A, 10 A and 15 A. The graph demonstrates that the discussed loss sources and simplifications that were ignored by PLECS contribute significantly to the total losses of the converter.

Fig. 4.13 considers the total losses in order to give an estimation of the converter’s overall efficiency for the three load current cases described in Fig. 4.12. The difference between the efficiency from the prototype and the simulation results is related to the higher losses that occurred from the prototype testing.
**Fig. 4.12:** Total converter losses comparison between simulation and prototype testing

**Fig. 4.13:** Converter efficiency as a function of load current for simulation and prototype testing
5. Environmental Test Results

A number of environmental and mechanical tests have been implemented on SiC MOSFETs and the results are presented in this chapter. Each subsection focuses on a specific test where the utilized environmental conditions are explained and the results both on transistor and converter level are presented and discussed. The tests have been conducted under specified conditions in the environmental testing lab at SCANIA and the transistors were provided by two different suppliers, Supplier A and Supplier B.

5.1. Test Setup

Initially, the prototype setup was tested at SCANIA lab under normal room temperature conditions. The MOSFETs were mounted in the DC-DC topology thus forming converter modules. The collected results can be divided into two distinctive categories: the ones related to the electrical characteristics of the MOSFET and the ones that evaluate the converter efficiency. For each test, the measurement conditions will be explained and kept constant among tests for better result comparison. Furthermore, the efficiency measurements and a switching loss estimation were facilitated with the utilization of Yokogawa’s WT1800 precision power meter and DLM2054 mixed signal oscilloscope that were provided for the purposes of this project.

The next phase involved the testing of SiC MOSFETs under specific environmental conditions. The selected conditions, which are presented in each corresponding subsection, are typical for testing electronic components in the automotive industry. SCANIA has performed various tests in automotive parts utilizing the same conditions which yielded the most interesting results. Therefore, previous experience has contributed to the choice of the environmental conditions that the MOSFETs were exposed to.

In each test, the components were placed inside the corresponding chamber or mounted on a metallic platform, in case of the mechanical vibration, for a number of testing hours. A simple schematic of the utilized chambers is given in Fig. 5.1 and Fig. 5.2 for each of the four implemented tests. The various elements marked in the schematics are given in Table 5.1 and Table 5.2 and are complementary for both figures.
The utilized environmental chambers were connected with a central lab computer where, via a user interface program, the operating parameters such as testing time, temperature, etc. of each chamber were set. In addition, the program allowed for monitoring the operation of the chamber, checking data regarding the real-time temperature, humidity or the vibration spectrum that was utilized and troubleshooting. For example, when the water level was low in the humidity chamber, an error message was sent in order to check the water tank. By the end of each time interval, the MOSFETs were removed and tested in the lab.
Table 5.1: Elements description of Fig. 5.1

<table>
<thead>
<tr>
<th>Element</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Water tank</td>
</tr>
<tr>
<td>2</td>
<td>Cooling fan</td>
</tr>
<tr>
<td>3</td>
<td>Tested MOSFET</td>
</tr>
<tr>
<td>4</td>
<td>Metallic mounting platform</td>
</tr>
<tr>
<td>5</td>
<td>Hot chamber</td>
</tr>
<tr>
<td>6</td>
<td>Cold chamber</td>
</tr>
<tr>
<td>7</td>
<td>Elevating pipe between hot and cold chamber</td>
</tr>
<tr>
<td>8</td>
<td>Connecting cable</td>
</tr>
<tr>
<td>9</td>
<td>Computer</td>
</tr>
</tbody>
</table>

Table 5.2: Elements description of Fig. 5.2

<table>
<thead>
<tr>
<th>Element</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>Temperature regulator</td>
</tr>
<tr>
<td>11</td>
<td>Shaker</td>
</tr>
<tr>
<td>12</td>
<td>Armature</td>
</tr>
<tr>
<td>13</td>
<td>Slip table</td>
</tr>
<tr>
<td>14</td>
<td>Metallic mounting fixture</td>
</tr>
<tr>
<td>15</td>
<td>Platform and table connection point</td>
</tr>
<tr>
<td>16</td>
<td>Table fixing point</td>
</tr>
</tbody>
</table>

The following sections describe the different environmental tests implemented as well as specify the conditions of each test. The results in MOSFET- and converter-level are presented and discussed.

5.2. Humidity Test

This group of tests aims to evaluate the impact of humidity in the operational characteristics of the MOSFET, mainly the gate-to-source threshold voltage, $V_{gs,th}$, and the ON-state resistance, $R_{ds,ON}$, that indicates failure of the device and increased conduction losses, respectively. For the purpose of this test, accelerated humidity conditions were utilized and the power devices were exposed to high temperature and humidity environment, specifically $T = 85 \, ^\circ C$ and $h = 85\%$ relative humidity. The test will demonstrate potential flaws in the encapsulation material of the MOSFET that will cause the presence of humidity in the metallization and integrated circuit die.

An efficiency evaluation was implemented in order to demonstrate the effect of the aforementioned conditions in the overall operation of the converter. The efficiency was measured prior and after each test in order to demonstrate an efficiency variation based on
with the testing conditions. A total of 500 h exposure in high humidity conditions was realized with an increasing duration after each test, starting at 48 h. The test was implemented in a total of 6 SiC MOSFETs grouped in two in order to formulate three converter modules. For this purpose, four Supplied A SiC MOSFETs (named H1 – H4) and two Supplier B MOSFETs (named H5 – H6) were utilized. In relation with the converter schematic of Fig. 3.2, the odd-numbered MOSFETs represent $T_1$ transistor, whereas the even-numbered MOSFETs represent $T_2$ transistor. The same definition applies for the rest of the conducted tests.

5.2.1. Threshold Voltage

The threshold voltage of the devices has been measured not only throughout the duration of the test, but also initially so as to demonstrate potential shifts from the reference measured value. For the purpose of this test, the gate and drain of each MOSFET were short-circuited and the source was grounded. The drain voltage, $V_{dd}$, was initially set to zero and was gradually increased until a current equal of $I_{ds} = 1\, \text{mA}$ started to flow between drain and source. This measured gate-to-source voltage was the threshold voltage of the MOSFET.

Fig. 5.3 and Fig. 5.4 highlight the possible shift in the threshold voltage, $V_{gs,th}$ as a result of the accelerated humidity conditions for Supplier A and Supplier B MOSFETs, respectively. The graph shows the evolution of $V_{gs,th}$ throughout the total number of test hours for the number of tested power transistors. Also, the graphs give the maximum, minimum and reference values provided by the manufacturer for $I_{ds} = 1\, \text{mA}$ and marked with the subscript “S”. If a measured value (subscript “T”) surpasses the upper or lower set limits, then the device is considered failed.

Before analyzing the graphs to a greater extent, the acquisition of the limits as well as the reference values for Supplier A MOSFETs should be explained. The particular MOSFET type that was utilized has not been launched yet in the market and no available datasheet existed in order to give a clear view on the upper and lower limits of the MOSFET as well as the reference value. In order to obtain these values, the threshold voltage of the MOSFETs prior to testing was measured and a mean value was calculated which was assumed to be the reference value utilized in the graphs from now on. This assumption is not entirely wrong as the $V_{gs,th}$ of Supplier A’s MOSFETs vary around this value. In addition, the minimum and maximum threshold voltage values were obtained based on ST’s research analysis et al. [49]. In this discussed application note of ST for the SiC MOSFET type SCT30N120, it is stated that if the threshold voltage of the tested MOSFET surpasses the limit of $\pm20\%$ from the reference value, then the MOSFET is considered failed. As a consequence, it is safe to say that these values represent the minimum and maximum allowed threshold voltage. This methodology is considered in all Supplier A’s MOSFET graphs for the threshold voltage and thus will not be repeated.
Fig. 5.3: $V_{gs,th}$ drift analysis for Supplier A’s SiC MOSFETs under accelerated humidity conditions

Fig. 5.4: $V_{gs,th}$ drift analysis for Supplier B’s SiC MOSFETs under accelerated humidity conditions

Test results indicated a shift in the initial value of $V_{gs,th}$ for both Supplier A and B tested subjects. For Supplier A’s MOSFETs H1 – H4, the shift did not exceed the boundary limits set
for the MOSFET and was smoother during testing. More specifically, both H1 and H2 almost reach the upper maximum value set for $V_{gs,th}$. As far as the Supplier B’s MOSFETs, both H5 and H6 devices faced a significant change in their threshold voltage values which started after 120 h of exposure. In particular, H6 had a very low value of $V_{gs,th}$ which is lower than the one specified by the supplier, while H5 demonstrated an increased $V_{gs,th}$, however it was within acceptable limits. The negative effect of high humidity on Supplier B’s MOSFETs can be justified by the different housing package utilized compared to Supplier A’s which apparently prevents humidity from penetrating the encapsulation material of the device and thus affecting its function.

5.2.2. ON-state Resistance

An estimation of the ON-state resistance, $R_{ds,ON}$, of the power device after each test can provide information regarding the conduction losses, and consequently, the efficiency variation that might occur. In order to obtain a reliable measurement, a simple circuit of a MOSFET and a connected load was modelled. The gate of the MOSFET was kept at $V_{Cy} = 20 \, V$, which is the recommended operating voltage by the supplier, and the drain was connected to a voltage source equal to $V_{dd} = 10 \, V$. An ohmic load of $I = 0.5 \, A$ was connected to the source of the MOSFET and the ON-state resistance was measured by monitoring the voltage drop, $V_{ds}$, across the MOSFET during conduction by applying Ohm’s law. The current was kept low in order to avoid abrupt junction temperature increase which would interfere with the measurements.

The acquisition of the $R_{ds,ON}$ reference value for Supplier A’s MOSFETs should be explained as well due to the lack of datasheet. In order to estimate a reference value for the ON-state resistance, measurements were taken for different $I_{ds}$ when the MOSFET was conducting and the voltage drop between drain and source was also measured. Based on the obtained data, the $V_{ds} - I_{ds}$ graph at low currents approximately approached a linear form for each SiC MOSFET of Supplier A. Therefore, it was assumed that the inverted gradient of this graph could give the reference value of the ON-state resistance. This method was applied for various Supplier A’s MOSFETs and a mean value of the resistance was defined. This approach was considered for all the implemented tests and therefore was not repeated.

The measurements of the ON-state resistance as a function of the total testing hours are given in Fig. 5.5 and Fig. 5.6 for Supplier A and B transistors, respectively. The measured resistance after each test was compared to the initially measured value prior to testing and the reference value provided by the supplier. For the MOSFETs H1 and H3 in Fig. 5.5, the initial value and the reference differed in comparison to the H2 and H4, where the initially measured and typical values were comparable. In addition, H1 and H2 MOSFETs of module 1 faced an increase in $R_{ds,ON}$ throughout the testing whilst H3 and H4 MOSFETs of module 2 decreased
over time as a result of exposure in humidity. The increased $R_{ds,ON}$ is related to the significant efficiency reduction observed in the figures below.

Fig. 5.6 represents the ON-state resistance of Supplier B’s MOSFETs for the total testing hours. The behavior of the two MOSFETs, according to the graph, was quite similar with the resistance decreasing over time and then followed an increase close to the reference value where it stabilizes until the end of the test. Observing the two graphs, Supplier B’s MOSFETs were more stable with respect to $R_{ds,ON}$ compared to Supplier A’s.

*Fig. 5.5: $R_{ds,ON}$ variation as a function of total testing hours for Supplier A’s MOSFETs under high humidity conditions*
5.2.3. Efficiency

Evaluating the impact of humidity on the overall converter operation was intertwined with the estimation of the efficiency while operating at different loading conditions. It was expected that these intense environmental conditions will affect either the conduction losses or switching losses by extending the rise and fall times of each MOSFET.

For the purpose of efficiency evaluation, two converter topologies have been utilized for each supplier. The 1\textsuperscript{st} is a reference topology comprised of power MOSFETs exposed only at room conditions whereas the 2\textsuperscript{nd} topology refers to power MOSFETs in the arrangement described before. The efficiencies of the tested and reference topologies were compared in order to highlight potential reductions attributed to the test. An assumption that was made here was that the efficiency of the reference topology was the same as the efficiency of the tested topology prior to the exposure in high humidity environment, i.e. all SiC MOSFETs of the same supplier were considered identical. Given the fact that SiC MOSFETs of the same supplier had the same electrical characteristics, with some minor differences, this assumption was acceptable and does not affect the accuracy of the results.

The efficiency of the converter was measured under various loading conditions. The results were only obtained for the 50 – 24 V operating mode of the converter and the load

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Fig. 5.6: $R_{\text{ds,on}}$ variation as a function of total testing hours for Supplier B’s MOSFETs under high humidity conditions
varies from $I = 5 - 15 \, A$. Fig. 5.7 to 5.9 show the efficiency variation of Supplier A’s and B’s modules as a function of total testing hours for the three loading conditions. The reference efficiency in each case is marked at $t = 0 \, h$ indicated by a dashed line. The results were obtained with a maximum measurement accuracy equal to $\pm 0.15\%$

Fig. 5.7: Efficiency variation of Supplier A’s converter module 1 at loading condition of 5A, 10A and 15A under accelerated humidity test

Fig. 5.8: Efficiency variation of Supplier A’s converter module 2 at loading condition of 5A, 10A and 15A under accelerated humidity test
What is interesting in Fig. 5.7 is the reduction observed in the end of the test. In Fig. 5.5, Supplier A’s module 1 MOSFETs (H1 and H2) faced an increase in $R_{ds,ON}$ which is translated to a reduced efficiency due to conduction losses. On the contrary, for Supplier A’s module 2 MOSFETs (H3 and H4), the decrease in $R_{ds,ON}$ resulted, overall, in lower efficiency reduction, as depicted in Fig. 5.8.

![Efficiency vs. Humidity Test Hours for Supplier B Module 1](image)

*Fig. 5.9: Efficiency variation of Supplier B’s converter module 1 at loading condition of 5A, 10A and 15A under accelerated humidity test*

The efficiency waveforms followed, for the most part, the reference value of the topology. Halfway through the test, the efficiency of each module was greater than the efficiency of the reference topology indicating the minor differences that exist among the power devices of the same supplier. However, these differences were negligible and did not affect the accuracy of the results. Observing the efficiency of each converter module, it is clear that high humidity conditions have a negative effect on the efficiency of the converter. After almost 300 h of testing, all converters demonstrated a slight reduction in their overall efficiency.

For Supplier A’s converter module 1, at 500 h the efficiency steadily decreased by 0.466% at 5 A, 0.315% at 10 A and 0.39% at 15 A load, while, for Supplier A’s converter module 2, the efficiency decreases by 0.186%, 0.237% and 0.373% for the same loading conditions. On the other hand, Supplier B module’s efficiency appeared unaffected at low loading conditions, according to Fig. 5.9, with the efficiency following closely the reference value. However, at 15 A, the efficiency reduced by 0.247%. This reduction could be a result of the increase in $R_{ds,ON}$ of the H5 Supplier B’s MOSFET, as already demonstrated in Fig. 5.6.
5.3. Temperature Shock

Temperature shock alternates the temperature in which the MOSFETs were exposed periodically between a hot and a cold chamber. Each cycle started in the hot chamber at $T = 140\, ^\circ C$ and then almost instantly, the MOSFETs were exposed to the cold chamber which was at $T = -40\, ^\circ C$. The dwell time for each chamber was $t = 10\, min$ and the interchange between chambers occurred within seconds. The applied temperatures were chosen to lie within the range of operating junction temperatures of each MOSFET type which are $T_j = -55\, ^\circ C$ to $T_j = 150\, ^\circ C$ for Supplier B and $T_j = -55\, ^\circ C$ to $T_j = 200\, ^\circ C$ for Supplier A, according to the corresponding datasheet specifications. This way, the negative effect of ageing and thus degradation of the material due to very high or low temperature is ruled out.

A total of six SiC MOSFETs were tested with the division being the same as the humidity testing, namely four Supplier A transistors (named T1 – T4) and two Supplier B transistors (named T5 – T6) thus creating three distinctive DC-DC converter modules. Several tests were implemented with a steadily increasing number of cycles in order to evaluate the effect of the testing conditions, completing a total of 1000 cycles. The transistor-level results include gate-to-source threshold voltage, $V_{gs,th}$, and the ON-state resistance, $R_{ds,ON}$ whereas, in the converter-level, the focus was on evaluating possible efficiency alterations.

5.3.1. Threshold Voltage

The effect of temperature shock on the threshold voltage on Supplier A’s and B’s MOSFETs is given in Fig. 5.10 and Fig. 5.11, respectively. The graphs evaluate the effect of temperature shock in the threshold voltage in each tested component for a total of 1000 cycles. Apart from the measured value in the test (marked as T), the graph included the minimum, maximum and typical values given by the supplier. Overall, no component failed during the tests.
Comparing Fig. 5.10 with 5.3, it is clear that temperature shock had a less severe effect on threshold voltage for the 1st module MOSFETs of Supplier A, compared to humidity. In both
cases, a shift from the initially measured value was observed, however, for temperature shock the effect was less dire with the voltage having a value close to the reference, as shown in Fig. 5.10, compared to humidity tests where the voltage was measured close to the maximum limit given by the supplier. Only T4 MOSFET had demonstrated a reduced threshold voltage as a result of temperature shock. On the other hand, in Fig. 5.11 the effect of the test on Supplier B’s MOSFETs had also affected negatively the electrical characteristics of the transistors with the voltage increasing steadily. Although the result lied within the limits, it is clear that expanding the test cycles will worsen the results.

5.3.2. ON-state Resistance

Fig. 5.12 and 5.13 demonstrate the variation of the ON-state resistance of the utilized MOSFETs as a function of the number of cycles. Fig. 5.12 represents the obtained measurements for Supplier A’s MOSFETs of each module. Concerning the 1st Supplier A module, the overall variation of the resistance was generally small compared to the initial value. For both MOSFETs, T1 and T2, the resistance appeared to decrease to a value closer to the reference after 300 cycles. On the contrary, T3 MOSFET of the 2nd Supplier A module demonstrated a significant increase in its $R_{ds,ON}$ of about $10 \text{ m}\Omega$, whilst T4 MOSFET showed a significant decrease of $8 \text{ m}\Omega$. The variation of the resistance affected the converter’s efficiency, as shown in the corresponding figures.

![ON-state resistance variation](image)

*Fig. 5.12: ON-state resistance variation with total number of cycles for Supplier A’s MOSFETs*
As far as the Supplier B converter module of Fig. 5.13, T5 MOSFET appeared to have a constant increase in $R_{ds,ON}$ after 100 cycles reaching the reference value given by the supplier, whereas T6 MOSFET appeared to be more stable with the value varying slightly around its reference. Nevertheless, Supplier B’s SiC MOSFETs are more stable than their Supplier A counterparts given their overall behavior in the temperature shock test, a fact that will be more apparent in the efficiency comparison in the next section.

5.3.3. Efficiency

The effect of temperature shock in the efficiency of the tested modules is given in Fig. 5.14 through Fig. 5.16. A percentage variation between the reference and measured efficiencies was calculated at different number of cycles. However, in order to relate this variation to the environmental test and not to the measurement error of the power meter, the calculated percentage should be greater than the accuracy error of the power meter.

Fig. 5.14 and 5.15 present the efficiency variation with respect to the number of cycles for both Supplier A’s converter modules. Concerning module 1, the efficiency stabilized around the reference value by the end of 1000 cycles at loads up to 10 A. On the other hand, the efficiency was reduced by 0.22% at 15 A, indicating reduced performance of the converter at high load current. When taking a closer look at the 2nd Supplier A module, the efficiency had a more stable behavior regardless of the connected load. More specifically, at 5 A load, the efficiency followed steadily the reference value. At larger loads, the efficiency showed a “valley”
at 600 cycles for 10 A and 15 A which was attributed to low output voltage compared to the rest of the testing cycles.

Regarding the effect of $R_{ds,ON}$ on the efficiency, for Supplier A module 1, the low resistance measured after 300 cycles resulted in an increase in efficiency, compared to the reference value. The subsequent decrease could be attributed to an increase in switching losses due to reduced behavior of the MOSFET as a result of the implemented test. For the 2\textsuperscript{nd} module, the increased and decreased $R_{ds,ON}$ of the two MOSFETs can be negated and therefore the efficiency was closer to the reference point up to 300 cycles. After this point, the increase in $R_{ds,ON}$ of T4 MOSFET instantly decreased the efficiency, especially in higher loading conditions as can be seen in Fig. 5.15 at 600 cycles.

![Efficiency vs. Number of Cycles for Supplier A Module 1](image)

*Fig. 5.14: Supplier A’s 1\textsuperscript{st} module efficiency performance under various loading conditions at temperature shock test*
Fig. 5.15: Supplier A’s 2nd module efficiency performance under various loading conditions at temperature shock test

Fig. 5.16: Supplier B’s module efficiency performance under various loading conditions at temperature shock test

Fig. 5.16 shows the performance of Supplier B’s converter module for different loading conditions. The behavior of the converter was comparable with Supplier A’s modules given the fact that they presented the same efficiency decrease in 600 cycles. At 1000 cycles, the efficiency was close to the reference value at 5 A and 10 A load. However, at 15 A the efficiency
slightly decreased by 0.245% from the reference value. It seemed that $R_{ds,ON}$ was not affecting the efficiency to the same extent as Supplier A and thus a possible explanation would be an increase in the switching losses of the MOSFET. Of course, an increase in $R_{ds,ON}$ of T5 MOSFET can justify the decrease of the efficiency profile. However, exposure to additional cycles would provide more information regarding the overall performance of the converter.

5.3.4. Cross-section Analysis on Supplier A’s SiC MOSFET

The maximum output current, determined by the inductor, is assumed to be equal to $I_o = 20 \, A$ which means that the input current will be slightly larger than $10 \, A$, but in any case, within the maximum current specified by the MOSFETs’ suppliers. In addition, the cooling system of the converter is able to dissipate the heat when this maximum output current is applied. Therefore, the converter should be able to operate constantly at such loading conditions without any damage caused to power MOSFETs.

However, when exposed to temperature shock test, Supplier A’s power MOSFETs exhibited an interesting behavior. Applying a $18 \, A$ load to the output, the converter was able to operate for an instant before short-circuiting the MOSFET and its function was disrupted. The measured current before damage was $I \approx 9.4 \, A$ which managed to destroy the MOSFETs even though these components were designed to withstand even higher currents. The odd-numbered MOSFET was short-circuited, a conclusion made by measuring the resistance between gate and drain and source, whereas the even-numbered MOSFET exhibited a damaged body diode. A possible reason behind this damage is shown in Fig. 5.17 which shows a cross-section x-ray of a damaged and a healthy MOSFET provided by Supplier A.

![Fig. 5.17: Cross-section X-ray of a functional (left) and damaged (right) Supplier A SiC MOSFET](image)

A careful examination of the two pictures presented in Fig. 5.17 will make apparent the difference between the damaged and the healthy MOSFET. On the right part of Fig. 5.17, the...
damaged MOSFET exhibit a detachment of the soldering material between the die and the lead frame indicated by the red markings on the MOSFET x-ray. However, on the left part, there is no such separation in the chip which may indicate the ability of the MOSFETs not exposed in temperature shock test to operate normally when exposed to the aforementioned loading condition following manufacturer’s specifications. A similar behavior was not exhibited by Supplier B’s MOSFETs whatsoever indicating that they were more robust when exposed to temperature shock test.

5.4. Accelerated Ageing

To address possible deterioration that might be caused in the material composition of each MOSFET due to ageing process, accelerated ageing test was conducted by exposing the SiC components to a high temperature environment. The temperature was chosen to be 10 °C above their maximum junction temperature, particularly \( T = 160 \, ^\circ\text{C} \) for Supplier B’s and \( T = 210 \, ^\circ\text{C} \) for Supplier A’s components. The transistors were placed inside of an oven of constant temperature for a total 500 h. At regular intervals, i.e. at 250 h of operation the MOSFETs were removed and tested in a component- and converter-level alike. In this test, focus has been given on the effect of the accelerated ageing process on the converter’s efficiency, while considering as well the MOSFET characteristics that were examined in the previous tests. Overall, two converter modules were utilized consisting of two Supplier A’s MOSFETs (named A1 and A2) and two Supplier B’s MOSFETs (named A3 and A4).

5.4.1. Threshold Voltage

The threshold voltage, \( V_{gs,th} \), results for the transistors involved in the accelerated ageing test are given in Fig. 5.18 for Supplier A’s and B’s MOSFETs. In the following figures, \( V_{gs,th} \) of each transistor is presented with respect to the total testing hours. Furthermore, the reference as well as the minimum and maximum values of each MOSFET type defined by the supplier are included. The total duration of the test was 500 h and none of the tested components failed during this test.
According to the obtained results, none of the tested power MOSFETs appeared to be affected by the accelerated ageing test, apart from Supplier A’s A2 MOSFET. The threshold voltage of the rest of the tested components vary little or nothing at all when exposed to these conditions. On the contrary, A2’s threshold voltage decreased by 0.3 V between 250 and 500 h thus approaching the minimum specified value. By increasing the exposing time for these components, it was possible that their reduced life cycle due to the high temperature was shifting the voltage from the reference value and the results become more evident.

As far as Supplier A’s MOSFET A2 is concerned, a possible explanation for the reduction in the threshold voltage is given in Fig. 5.19 which shows the back side of A2 MOSFET. After 250 h of testing, it exhibited a degradation of the heat sink plane which can be closely related to the reduction in the threshold voltage $V_{gs,th}$. 

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*Fig. 5.18: $V_{gs,th}$ drift analysis for Supplier A’s (left) and B’s (right) MOSFETs under accelerated ageing test*
5.4.2. ON-state Resistance

The behavior of the MOSFETs with respect to their ON-state resistance as a function of total testing hours is given in Fig. 5.20 which summarizes the value of $R_{ds,ON}$ for the total number of tested components. In the corresponding graphs of Fig. 5.20, $R_{ds,ON}$ is compared with the initially measured prior to exposing the device in the test conditions and the manufacturer’s specified reference value for the same testing conditions.

Observing the obtained results for Supplier A’s converter module, both MOSFETs exhibited a change in the ON-state resistance compared to their initial values. Although the increase in MOSFET A1 was rather small by the end of the test, MOSFET A2 showed a greater change which resulted in a lower $R_{ds,ON}$ of almost $20 \, \text{m} \Omega$, a result that could be related to the damaged heat sink depicted in Fig. 5.19. Supplier A’s MOSFETs follow the same pattern compared to the previous tests where the first MOSFET’s resistance is increased and second MOSFET’s decreased. The reason behind this could be the different stressing conditions for each MOSFET during the converter’s operation.

On the contrary, Supplier B’s MOSFETs demonstrated a constant increase in ON-state resistance, although significantly smaller compared to the aforementioned tests, indicating that this type of test can negatively affect their performance in the long run. It is obvious that this test had a more negative effect on Supplier B’s MOSFETs in terms of ON-state resistance, as shown in Fig. 5.20.
5.4.3. Efficiency

Fig. 5.21 and 5.22 evaluate the performance of the implemented converter modules in terms of efficiency as a function of the total test hours. In Fig. 5.21, the efficiency of Supplier A’s converter is demonstrated for the loading conditions of 5 A, 10 A and 15 A. At 250 h of testing, the converter showed an efficiency drop which can be attributed to the inability to regulate the output voltage precisely at 24 V as well as the significant increase in ON-state resistance of the MOSFET A1. Overall, the efficiency was not affected by the testing conditions considering that it reaches a value close to the reference one by the end of 500 h of testing. For the 15 A, however, an efficiency reduction of 0.23% was observed which may indicate potential reduced performance at higher loading conditions. The reduced efficiency at 15 A can be related to the damaged heat sink plane of MOSFET A2. The degradation of heat sink may result in higher junction temperature compared to the reference case thus higher ON-state resistance and conduction losses.
**Fig. 5.21:** Supplier A’s module efficiency variation as a function of total testing hours for three loading conditions

**Fig. 5.22:** Supplier B’s module efficiency variation as a function of total testing hours for three loading conditions

Fig. 5.22 shows the efficiency variation of Supplier B’s converter module for the total testing hours. Unlike Supplier A’s, this module followed the reference efficiency for the most part of testing showing little variation until the point of 250 h. Until the end of the test, at currents 5 A, 10 A the efficiency dropped which can be justified by the increased $R_{ds,ON}$ of both
MOSFETs that leads to a reduced efficiency by the end of the test for loads up to 10 A. At 15 A, the efficiency was almost equal to the reference indicating that the converter’s performance was not affected by high connecting loads. Overall, the efficiency drop was very low and thus increasing the exposing time of the devices is necessary to draw conclusions for the converter’s performance profile.

5.5. Mechanical Vibration

Focusing on the ageing effect in the MOSFET’s overall characteristics, one of the most crucial tests conducted was the mechanical vibration. For this test, a random vibration was induced onto the power electronic components that simulated common vibration forces during a vehicle’s motion, especially when the road surface is rough. An expected outcome of this test would be rupture or wear of the encapsulation of the MOSFET or even further damage to the die or metallization. In the latter case, the MOSFET would no longer been functional.

The DC-DC converters employed at SCANIA trucks are considered as chassis mounted components therefore the prototype implemented in this project was tested based on the chassis spectrum. The components were placed on a metallic base which was mounted on the shaker armature. Overall, four Supplier A’s MOSFETs (V1 – V4) and two Supplier B’s MOSFETs (V5 – V6) were subjected to vibration tests. The purpose was to verify whether the transistors were able to withstand accelerated vibration with a total duration of 8h. Then, the electrical characteristics of the components were measured in the lab and the efficiency of the converter was evaluated. Mechanical vibration tests were based on the IEC 60068-2-64Nb:2008 standard.

5.5.1. Threshold Voltage

Fig. 5.23 and Fig. 5.24 estimate the gate threshold voltage, \( V_{gs.th} \), variation of Supplier A’s and B’s power MOSFETs respectively for the total hours of vibration tests. More specifically, Fig. 5.23 shows the gate threshold voltage for Supplier A’s power MOSFETs tested in vibration conditions. The graph shows that the test had a negligible effect on the \( V_{gs.th} \) of each power MOSFET which maintained their initial value prior to testing.

The same conclusion could be drawn for Supplier B’s MOSFETs while examining the threshold voltage results for the tested components in Fig. 5.24. It is evident that \( V_{gs.th} \) did not shift for V6 MOSFET which remained constant at \( V_{gs.th} = 1,9 \, V \), while, for V5 MOSFET, the value had shifted from \( V_{gs.th} = 2 \, V \) to \( V_{gs.th} = 2,1 \, V \) which was within the specified limits. It is worth mentioning that this stability in the measured value could be a result of a small number of total testing hours.
5.5.2. **ON-state Resistance**

The effect of mechanical vibration on the ON-state resistance, $R_{ds,ON}$, of the tested SiC
power MOSFETs was examined. The graphs given in Fig. 5.25 and 5.26 compare the on-state resistance of each MOSFET utilized in the test with its reference value prior to exposure which was measured at lab conditions.

Fig. 5.25 gives the ON-state resistance for Supplier A’s MOSFETs utilized in the corresponding converter modules. It is obvious that the mechanical vibrations did not affect the value of $R_{ds,ON}$ which remained constant and equal to the reference value for most of the tests. For testing objects V1 and V4, the ON-resistances had shifted from the reference value. However, this could be more likely a measurement error rather than caused by mechanical vibration. The rest of Supplier A’s MOSFETs maintained their $R_{ds,ON}$ value.

![Graphs showing $R_{ds,ON}$ values as a function of mechanical vibration testing hours for Supplier A’s MOSFETs](image)

The same results occurred for Supplier B’s MOSFETs simply by observing Fig. 5.26. V5 MOSFET showed a variation from the reference value, however it was only 2 mΩ which could probably be a measurement error. V6 MOSFET of Supplier B’s topology maintained the initial ON-state resistance value regardless of the testing hours.
5.5.3. Efficiency

The chapter concludes the mechanical vibration results with regard to the converter’s overall efficiency for the two types of MOSFETs. The efficiency was measured throughout the testing process by means of a high-accuracy power meter. As earlier, the efficiency was measured at the three loading conditions \( (I = 5 - 15\, A) \).

Fig. 5.27 and Fig. 5.28 present the efficiency measurements for the two Supplier A converter modules from mechanical vibration testing. Observing the 1st converter module in Fig. 5.27, it is clear that the efficiency had insignificant change. For 10 A and loads, the efficiency followed the reference value. On the other hand, for 5 A the efficiency was 15 A constantly lower than the reference value. This is acceptable since the reference and tested topologies were different and the comparison was based on the aforementioned assumptions. As long as the profile of efficiency is constant throughout the test, it seems that the vibration tests did not have any effect on the converter’s performance.

An examination of Fig. 5.28 and the 2nd converter module yielded almost the same conclusions as the 1st module. Regardless of load, the efficiency maintained a constant profile. For instance, observing the value measures at \( t = 0\, h \) and the value obtained at \( t = 32\, h \), it is obvious that the efficiency did not change between these two points for the three load profiles. Consequently, the profile of the efficiency almost remain close to the initially measured value.
and the converter was not affected by the vibrations within the analyzed testing time despite the variations observed in the graph.

Fig. 5.27: Supplier A’s 1st module efficiency performance under three loading conditions at mechanical vibration test

Fig. 5.28: Supplier A’s 2nd module efficiency performance under three loading conditions at mechanical vibration test

Finally, Fig. 5.29 depicted the efficiency profile for Supplier B’s converter module. For
$I = 5 \, A$ and $I = 10 \, A$, there was almost no efficiency variation. In the former case, the efficiency profile followed the reference value after 16 h of testing, whereas, in the latter case, the profile was almost constant throughout the test indicating no change due to mechanical vibration. On the other hand, at $15 \, A$, the performance of the converter decreased at the end of the test with an efficiency reduction equal to 0.196%. This is the only indicator that the mechanical vibration might affect the converter’s performance at high loads within 32 h of testing. Certainly, more tests should clarify if the efficiency is reduced due vibration influence.

Fig. 5.29: Supplier B’s module efficiency performance under three loading conditions at mechanical vibration test
6. Conclusions & Future Work

6.1. Conclusions

This project investigated the improved features introduced by the SiC technology on power MOSFETs utilized in EV and HEV DC-DC converters. The objective was to expose the power devices on environmental conditions and estimate the effect on their electrical characteristics. The obtained results were evaluated in order to emphasize on how the implemented tests could impact the performance of the DC-DC converter by presenting and analyzing the efficiency profiles under certain loading conditions.

SiC MOSFETs improved significantly the design of the converter resulting in low-size LC filter and reduced cooling requirements with respect to the design considerations. As a consequence, the overall volume of the converter kept the design compact and robust. In addition, the utilization of SiC increased the efficiency of the converter even at high loading conditions with an efficiency greater than 90%. By reducing the EMI effect at high-switching frequencies, the efficiency can further increase.

With regard to testing on a component level, the threshold voltage demonstrated a significant variation from its initially measured values. Accelerated humidity conditions affected negatively Supplier B’s MOSFETs which displayed considerable variations from the initial value and failure due to low threshold voltage. Supplier A’s MOSFETs were affected negatively as well, but not to the same extent as Supplier B’s. Similarly, temperature shock impacted both MOSFET types where Supplier B’s had greater variations in the voltage compared to A’s. On the other hand, neither mechanical vibrations nor accelerated ageing test affected significantly the MOSFETs’ threshold voltage and thus additional exposing hours should be considered.

Humidity and temperature shock influenced the resistance measurements through time underlining a potential efficiency effect. Concerning the humidity conditions, Supplier A’s MOSFETs demonstrated almost identical resistance variation profiles based on their position in the converter. The same conclusion could be drawn for Supplier B where the resistance appeared to vary over time but close to the initial values. Supplier A’s components demonstrated abrupt increase or decrease in their resistance when exposed to high temperature or temperature shock tests compared to the initial values. On the contrary, Supplier B’s transistors showed very low resistance variations under the same conditions.

Transcending on a converter level, the most significant efficiency reductions were observed in the humidity tested components. Supplier A’s MOSFETs demonstrated a considerable reduction in efficiency by the end of the test which partly was attributed to the ON-resistance increase and partly to a potential change in the switching losses. The humidity
affected the electrical characteristics of the component possibly because the capacitance between gate and drain and source was affected negatively thus increasing the turn-ON and turn-OFF switching times. Besides Supplier A’s components, Supplier B’s MOSFETs were also monitored regarding the efficiency which exhibited changes in high loading conditions.

Furthermore, the performance evaluation of the converter for temperature shock tests highlighted the negative effect on the converter’s performance. The large reductions observed in the ON-resistance were translated in increased efficiency for the converter which, however, was not ongoing. By the end of the test, both MOSFET types caused efficiency reductions, especially when the output load was 15 A.

On the contrary, the obtained results from ageing tests showed significant efficiency reductions due to the acquired ON-state resistance profiles, but the converter managed to reach the reference value by the end of the test. Exposure of the components to mechanical vibration conditions did not affect the efficiency either regardless of the load. Nevertheless, by increasing the time of exposure for both tests could shift the efficiency profiles.

### 6.2. Future Work

Exposing the SiC in severe environmental conditions showed a slightly reduced performance of the converter and component, however, further testing in these conditions is necessary in order to evaluate their overall performance and breaking point. For instance, ageing and mechanical vibrations showed almost negligible efficiency reductions and therefore must be further examined to evaluate the behavior of the devices. Adding to this, electrical characteristics of power MOSFETs such as breakdown voltage and thermal resistance should also be examined as environmental tests might have a negative effect on them.

An important part of the project was the evaluation of efficiency for the tested components. Based on the ON-state resistance obtained results, a portion of the efficiency reductions could be result of increased conduction losses. Nevertheless, it would be interesting to further evaluate the impact of testing on the switching losses. It is possible that the inherent capacitances of the SiC MOSFETs might be affected by the environmental conditions and thus the switching ON and OFF times have increased.

An additional direction that the project could follow would be the further improvement of the existing topology by accounting for electromagnetic interference (EMI) from the MOSFETs during switching time or between other electronic components. Moreover, a comparative efficiency evaluation for a larger number of SiC MOSFET suppliers would be also beneficial as it will address potential failure mechanisms and deficiencies between different SiC MOSFETs.
Appendix: Project Budget

This section presents a total cost analysis by taking into consideration all the implementation costs throughout the duration of the project. The analysis covers various sources of cost that cover the manufacturing of the converter, for instance the cost for creating 2 different prototypes, one for each SiC MOSFET supplier, the cost of components damaged during lab and environmental testing as well as the cost of the inventory that is related to additional electronic components that are not accounted in the prototype cost.

Prototype manufacture costs include the cost of the components utilized in the prototypes. Based on the part of the converter that is being utilized, each individual component's cost is included in one of the 4 following groups: the gate driver and common emitter circuit, the main converter circuit, the cooling system and the PWM generator. The rest are included in the corresponding category. At this point, it should be noted that only the cost of 2 SiC MOSFETs is considered for each prototype as the rest are included in the inventory cost, even though they are utilized in the testing. Table A.1 gives the prototype manufacture costs of the project.

<table>
<thead>
<tr>
<th>Cost Description</th>
<th>Cost in Supplier A Prototype (€)</th>
<th>Cost in Supplier B Prototype (€)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Driver &amp; Common Emitter</td>
<td>7,62</td>
<td>7,62</td>
</tr>
<tr>
<td>Converter Main Circuit</td>
<td>129,93</td>
<td>147,13</td>
</tr>
<tr>
<td>Cooling System</td>
<td>50,91</td>
<td>50,91</td>
</tr>
<tr>
<td>PWM Generator</td>
<td>34,82</td>
<td>34,82</td>
</tr>
<tr>
<td>Rest</td>
<td>68,4</td>
<td>68,4</td>
</tr>
<tr>
<td><strong>Total Cost (€)</strong></td>
<td><strong>291,68</strong></td>
<td><strong>308,88</strong></td>
</tr>
</tbody>
</table>

The number of components that are considered as inventory correspond to the functional components as accounted the last day of testing. Moreover, the cost of the components that were purchased for the initial testing process of the converter but they are not utilized in the final prototype are included in the inventory costs as well given in Table A.2. On the other hand, the number of damaged components due to failure either during testing or while the converter was operating are included in Table A.3 for the damaged equipment costs. In both tables, the costs are grouped in the same manner as Table A.1.
Table A.2: Inventory Costs

<table>
<thead>
<tr>
<th>Cost Description</th>
<th>Amount (€)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supplier A’s MOSFETs</td>
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<tr>
<td>Supplier B’s MOSFETs</td>
<td>363,74</td>
</tr>
<tr>
<td>Main Converter Components</td>
<td>87,08</td>
</tr>
<tr>
<td>Other Equipment</td>
<td>34,16</td>
</tr>
<tr>
<td><strong>Total (€)</strong></td>
<td><strong>1027,62</strong></td>
</tr>
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</table>

Table A.3: Cost of Damaged Components

<table>
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<th>Cost Description</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Main Converter Components</td>
<td>94,4</td>
</tr>
<tr>
<td>PWM Generator</td>
<td>34,09</td>
</tr>
<tr>
<td>Gate Driver &amp; Common Emitter Circuit</td>
<td>1,98</td>
</tr>
<tr>
<td><strong>Total (€)</strong></td>
<td><strong>130,47</strong></td>
</tr>
</tbody>
</table>

Considering all the above, Table A.4 summarizes the final cost of the project as calculated from the aforementioned tables.

Table A.4: Total Cost of Project

<table>
<thead>
<tr>
<th>Cost Description</th>
<th>Amount (€)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prototype Manufacture</td>
<td>291,68</td>
</tr>
<tr>
<td>Inventory</td>
<td>1027,62</td>
</tr>
<tr>
<td>Damaged Components</td>
<td>130,47</td>
</tr>
<tr>
<td><strong>Total Project Cost (€)</strong></td>
<td><strong>1758,65</strong></td>
</tr>
</tbody>
</table>
Acknowledgements

Reflecting all my work in this thesis project, I would like to thank my supervisor at SCANIA AB, Dr. Samer Shisha, senior engineer in VCB Components Environmental Verification department. His guidance and support were crucial for the successful completion of this project. But, more importantly, I want to thank him for providing me with the opportunity to join SCANIA for my master thesis.

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Avraam Kyriakidis

Barcelona, September 2018
Bibliography


Performance Evaluation of SiC Power MOSFETs for Hybrid & Electric Vehicles DC-DC Converter


