Variations-Aware Circuit Designs for Microprocessors

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I. Introduction

As we enter the Deep Sub-Micron era, Integrated Circuits (ICs) manufacturers are facing the increasing amount of layout process variations that arise from the optical lithography manufacturing process and that pose many challenges for circuit design due to their effects in performance, power and yield.

In order to mitigate the impact of these process variations new Design For Manufacturability and Yield (DFM&Y) approaches are required [1-3]., where DFM&Y techniques can be defined for any given industry as the methodologies to ensure that products can be manufactured repeatedly, consistently, reliably and in a cost-effective manner. In the field of ICs, Resolution Enhancement Techniques (RETs) such as Phase Shift Mask (PSM), Optical Proximity Correction (OPC) and Off-Axis Illumination (OAI) have been used to greatly improve layout printability and to reduce process variations. However, these techniques are computationally expensive and very time-consuming for large integrated circuits with arbitrary layout patterns. That is why new DFM&Y regularity-based techniques, with a reduced number of layout patterns, like Gate Arrays or Structured ASICs are emerging as a possible solution for manufacturers.

Layout regularity helps to reduce the enormous data set to be treated by RETs applied to a huge number of layout patterns. For example, in a usual Standard Cell library consisting of 1000 standard cells there are approximately 2 million possible configurations to arrange a pair of standard cells. By improving layout regularity, RETs can work properly and efficiently to reduce the variations caused by lithography.

II. VCTA proposal

Our proposal is a new regular layout style called Via-Configurable Transistor Array (VCTA) that maximizes layout regularity at device and interconnect levels in order to maximize the benefits of layout regularity [4]. VCTA is a regular fabric based on a single configurable basic cell including transistors and interconnects. Fig. 1 and 2 show the VCTA basic cell and how it is connected to obtain the complete layout.

The expected benefits of layout regularity are: (a) a reduction of the amount of process variations by allowing RETs to more effectively mitigate lithography printability issues, (b) a reduction of the yield loss associated to circuit energy and delay unpredictability due to the reduction of process variations, (c) a reduction of the time-to-market by accelerating RETs and also due to the lower number of basic cells or layout patterns and neighborhoods to be optimized, (d) a reduction of design costs as a consequence of the previous benefits.

Based on the observation that regular designs such as SRAMs get to the market long before irregular conventional logic designs such as microprocessors, we believe that VCTA maximum regularity may allow to use the next technology node with commercial yield when Standard Cells use still the old one. To explore the whole regularity trade-offs, we also have to measure and take into account area, delay and energy overheads due to VCTA regularity.

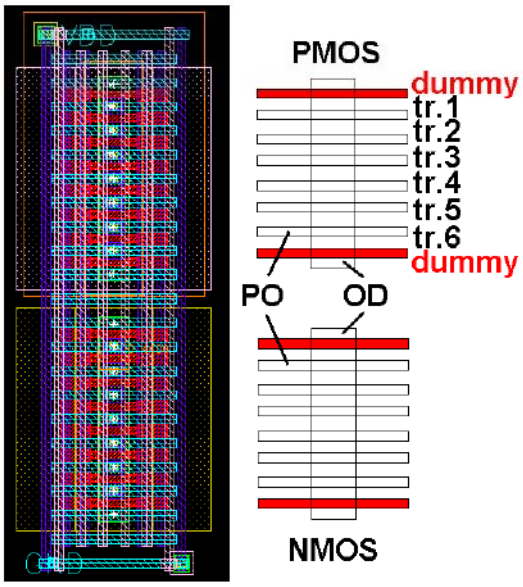

Figure 1. Transistor Array structure.

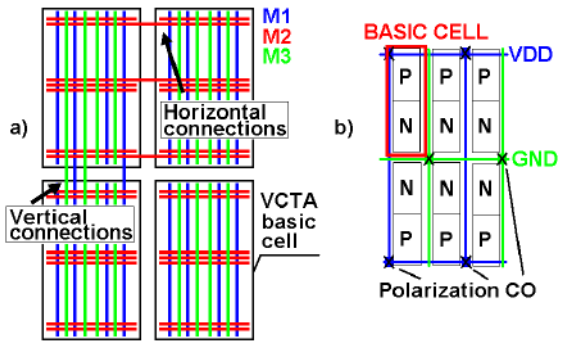

Figure 2. a) Metal grid structure b) Placement and power supply network of VCTA basic cells (6 cells in the picture).

III. Results

In order to illustrate that our VCTA regular design technique allows the implementation of complex circuits we focus on combinational logic circuits like binary adders that are usually included in typical IC designs.

In particular, we have developed complete layouts in the 90 nm technology node for a 32-bit Carry-Ripple adder (CR32) and for a 32-bit Carry-Lookahead adder (CLA32) using the VCTA structure and also the Standard Cell approach (STD) to evaluate the area, energy and delay overheads in two commonly used circuits.

III.A. CR32 and CLA32 without process variations

We have performed complete electrical simulations of the extracted layouts of CR32 and CLA32 in the

90nm technology node. We have evaluated both the adders designed with our VCTA regular design as well as those based on standard cells in terms of delay and energy for 10400 inputs that we have sampled from all 26 programs in the SPEC2000 benchmark suite. We have measured the delay from input variation to the associated output transition considering the cross at 90% of the voltage rise or fall swings. We have also measured energy for each input combination integrating the current demand at the power supply source during the sum. Finally, we have measured the area directly from the layout.

First, VCTA regular design implies an increase slightly smaller than 2x in area when compared to the STD approach. In terms of delay and energy, results are complementary for CR32 and CLA32. On one hand CR32 presents more than a 2x ratio for delay but less than a 2x ratio for energy, and on the contrary for CLA32. In fact overheads introduced by VCTA when compared to STD are very much dependent on the function to implement. STD uses different standard cells depending on the circuit optimization but VCTA always uses the same basic cell.

III.B. CR32 and CLA32 with process variations

In order to evaluate our VCTA proposal under device process variations, we have performed the same electrical simulations considering 3-sigma gaussian random local process variations on PMOS and NMOS parameters.

We expect that our VCTA proposal presents some process variation decrease because of its layout regularity. Estimating how much variations would decrease is fully technology dependent, so we have studied 3 variability scenarios: (a) Considering 100% of the Gaussian distribution 3-sigma deviation percents for the MOS parameters variations, (b) Considering 75% of the technology variations (25% reduction), (c) Considering 50% of the variations (50% reduction).

As expected, the reduction due to layout regularity of the amount of device process variations implies a decrease of the variability of delay and energy for our regular VCTA proposal. The decrease is almost linear with the reduction of process variations. The strength of VCTA is to reduce the amount of process variations and not to be more robust in front of the same amount of process variations.

IV. Conclusion

Our VCTA design technique explores the impact of maximizing layout regularity to maximize its benefits. Maximum regularity reduces the amount of process variations and therefore reduces drastically the time-to-market and the investments required to reach commercial yields. We expect that VCTA permits the use of a future technology node when the STD designs still use the old one.

CR32 and CLA32 Monte-Carlo simulations have shown that, as regular designs benefit from a process variation reduction, energy and delay variability are reduced and therefore the circuit predictability is improved.

However, simulations also show that compared to the STD approach in the same technology node there is an important decrease in circuit efficiency due to regularity. Our final objective is to achieve similar performance for VCTA in the future technology node and for STD in such a way that both of them may reach the market at the same time but VCTA reduces investments required to achieve commercial yield levels and also final product cost.

V. Acknowledgments

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VI. References

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