Review on suitable eDRAM configurations for next nano-metric electronics era

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Abstract: We summarize most of our studies focused on the main reliability issues that can threat the gain-cells eDRAM behavior when it is simulated at the nano-metric device range has been collected in this review. So, to outperform their memory cell counterparts, we explored different technological proposals and operational regimes where it can be located. The best memory cell performance is observed for the 3T1D-eDRAM cell when it is based on FinFET devices. Both device variability and SEU appear as key reliability issues for memory cells at sub-22nm technology node.

Keywords: eDRAM, FinFET, sub-V_T, SEU, reliability

1. INTRODUCTION

One of the core circuits for the electronics research field is the memory cells, due to their large use and the dependence of the technology evolution. Indeed, Random Access Memory cells (RAM) are one of the main building blocks for electronics researchers. Principally, due to the continuous dimensions scale down has entailed an increase of the reliability and power consumption relevance. To mitigate these negative effects, different strategies have been regarded, e.g. change on device materials and topology [1]. When the gate dielectric is highly scaled down (< 2nm) an intolerable increase of leakage current and electric field in the devices is observed, what implies lower carrier mobility and worse reliability [2]. To overcome it, the introduction of high-k dielectrics (e.g. hafnium oxide) has been a real option, to the point of improve the device performance beyond 65nm technology node [3]. To enhance carrier mobility some solutions are also contemplated, e.g. strained channels and III-V materials are introduced on the device by producing a band gap narrowing and causing a mean free path increase [4]. The introduction of vertical multi-gate devices (FinFETs) to substitute planar CMOS technology has involved to take a step forward for VLSI circuits beyond 22 nm technology nodes [5]. In particular, their better control over the channel involves lower short channel effects impact, steeper sub-threshold slope and a relevant variability reduction [6] are the main behavioral benefits. Although the electronics industry is obsessed on to scale down the device dimensions, researchers realize that detrimental impact of the device reliability on the memory cell performance is observed. Device variability highlights a more difficult predictable cell behavior. Besides, smaller devices also involve lower node capacitances, and as a consequence a more sensitive device in front of an ion impact is obtained, i.e. larger soft error rate (SER) [7]. In memory cells, latches or flip-flops an alpha particle and neutrons may induce single event upsets (SEU) producing a bit flip and, thus, a change in the circuit behavior. On the other hand, ultra-low power circuits are of increasing interest in the Internet of Things (IoT) era and in booming healthcare applications [8], [9]. To reduce the power consumption, circuits operative below threshold voltage (sub-V_T circuits) have come out as an innovative option. Their performance target has been reported for medium-speed applications (kHz-MHz regime), e.g. wireless sensor networks, medical applications and mobile signal processing [9].

All these issues (reliability and consumption) significantly threat the memory cell performance. Specifically, SRAM and DRAM cells are typically designed using minimum feature sizes for density reasons. The baseline memory cell is the 6T-SRAM [10], but is highly influenced by variability and SER, since it presents significant speed degradation and cell instability [11]. In this context, gain-cell embedded DRAMs (eDRAM) are considered as promising candidates to substitute SRAM in VLSI systems, since they are more attractive than other proposals due to their higher density (>2X) [12], compatibility to mainstream CMOS processes, and non-destructive read operation (in contrast to the typical 1T1C-DRAM). Different eDRAM cell proposals exist, e.g. 2T, 2T1D, 3T and 3T1D, being the last one the most attractive in terms of reliability [13]. The 3T1D cell is mainly presented as a suitable memory cell for L1 memory caches [11]. Fast access times are required and low retention times are architecturally masked. The memory storage node of the 3T1D cell is a capacitor (the gate capacitance in the gate-diode) and it stores temporarily the data. To lose the contents and to hold data for extended periods, a periodic refresh is required [11]. Moreover, we have identified the core memory cell (designed with minimum device dimensions) as the main source of variability when a complete system data path was analyzed [14], compared to the amount introduced by the rest of the system blocks (e.g. sense amplifier, multiplexer, and flip-flop).

We review the benefits of using the 3T1D cell in front of other eDRAM proposals. The remainder of the paper is organized as follows: Section 2 explains the device models used to simulate the gain-cell eDRAMs and their simulation environment. Section 3 compares the performance of the different gain-cell eDRAM configurations. Section 4 analyses the impact on the implementation of the eDRAM cells by using devices with different topologies and materials. Section 5 presents the suitability of the 3T1D cell to operate at sub-V_T range. Section 6 reports the findings of a reliability study (variability and SEU) carried out on all the memory cells and different device types. Section 7 presents some future proposals for next technological nodes seeking smaller footprint and lower power consumption. Section 8 presents the conclusions.

2. Simulation framework

The schematic of the 3T1D-eDRAM cell simulated along this review is illustrated in Fig. 1. To determine the best option to simulate this memory cell, we have used two different devices topologies (planar bulk and FinFET) under different reliability scenarios and with different channel configurations, e.g. strained or III-V/Ge. We used the device models from the High Performance Predictive Technology Models (HP PTM) [15]. For the planar-bulk MOSFET, we used the 22nm HP PTM. To simulate FinFET devices, we used the 10nm Multi-Gate version of the PTM (HP PTM-MG) [16] -which is based on BSIM models and jointly developed with ARM technology. The nominal supply voltage (V_{DD}) is defined as 1V. To analyze the eDRAM behavior, we have obtained in all the studies the following cell parameters:

a) Retention Time (RT), time required for the storage node voltage (V_S) in the cell to decay to V_{Smin} [17]. This is stated as our reference parameter to analyze the cells.

b) Write Access Time (WAT) defined as the time elapsed between $V(WL_{write})=(0.5*V_{DD})$ and $V_S=(0.9*(V_{DD}-V_T))$.

c) Read Access Time (RAT) defined as the time elapsed between $V(WL_{write})=(0.5*V_{DD})$ and $V(BL_{read})=(0.9*V_{DD})$.

d) Dynamic Power consumption (PW) obtained by the average value along one cycle.

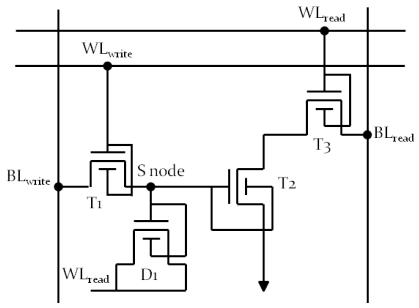

Figure 4. Schematic structure of the 3T1D-eDRAM cells analyzed during this work. WL is wordline and BL is bitline.

The relevance of the use of devices with strained channel and the III-V/Ge materials is analyzed as they enhance the device mobility. For a qualitative study, their introduction on 3T1D cell has been modeled by multiplying the nominal mobility parameter (U0) by a new parameter k_n, ranged from 1 to 5. In the case of the III-V/Ge MOSFET, we used models provided by the Device Modeling Group at University of Glasgow [18], developed using an atomistic simulator [19]. To study the impact of device variation on eDRAM cell parameters, 10,000 Monte Carlo simulations were run. The impact of variability has been modeled as a change in the memory cell's devices threshold voltage (V_T). A moderate (20%) variability level has been assumed along this work [6]. The variability relevance is evaluated by a statistical distribution with mean (μ) and standard deviation (σ), obtaining the $3\sigma/\mu$ ratio factor, expressed in percentage as impact factor. The environment temperature influence on the memory cell has been analyzed by considering 25º, 60º, 100º and 125ºC. FinFET self-heating effect is considered in all our simulations, by modifying their model. The radiation (SEU) sensitivity has been also analyzed, by simulating the impact of an ion strike with a pulse wave current has been modeled by a double exponential function [20]. SEU simulations are always under room temperature environment, since negligible temperature influence on Q_{crit} is observed [21]. Only, the strikes in the drain region are considered as they account for highest sensitivity region to soft error upsets [22]. For eDRAM cells the most sensitive region is the drain of the write access transistor. Since it is directly connected to storage node voltage (V_S), and the other ones are connected to the word line (WL) and bit line (BL) of the cell (Fig. 1), what involves a high load capacitance at those nodes and, consequently, larger robustness in front of soft errors.

3. Dielectric stack and channel material impact on 3T1D behavior

First, the influence of the gate dielectric material on the 3T1D cells was analyzed using the different 22nm HP PTM versions (1.0, 2.0 and 2.1) [17]. The former (PTM 1.0) is based on a MOSFET based on SiO_2 dielectric. The second (2.0) simulates a high-k based transistor. The last one (2.1) simulates a device with high-k dielectric and strained channel MOSFETs. Fig. 2 compares the 3T1D cell parameters obtained for all the device configurations. Unstrained cells based on SiO_2 or high-k gate dielectrics present the worst behavior, lower RT and high access times. The best performance is observed for the samples with strained channel and high-k dielectric. This is related to the lower leakage of the latter, due to the use of high-k dielectric; and better mobility, due to the use strained channel. On the contrary, the SiO_2-based sample shows the worst behavior as larger PW and lower RT are obtained.

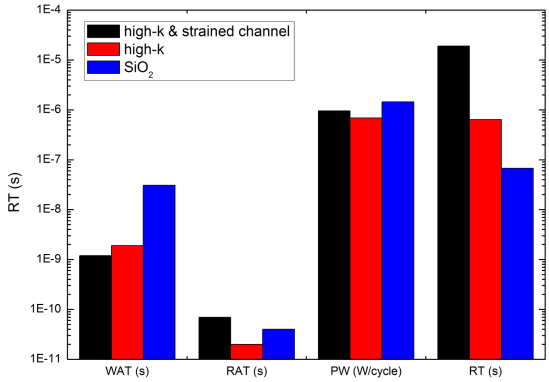

Figure 2. Analysis of the 3T1D cell behavior, when different PTM device models are used. The samples based on both high-k dielectric and strained channels present the best memoty cell bahavior.

Higher device channel strain in a memory cell has been shown as a valid option to enhance the memory cell behavior. For this, we analyze the impact of the mobility increase in the memory cell. Fig. 3 presents the evaluation of how a strain variation improves the RT values of 3T1D-eDRAM cells based on 22nm HP PTM devices. Two scenarios have been developed:

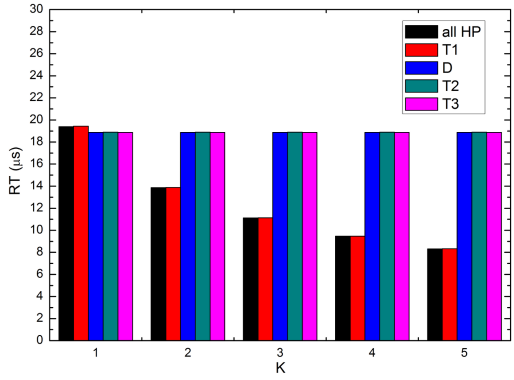

Figure 3. Influence of the strain variation on 22nm cell behavior when the strain magnitude is modified on all devices and one device at a time. T1 device shows the highest impact on 3T1D performance.

1) when the strain of all the cell devices is modified at the same time (all HP), and 2) when only the strain of one device is altered keeping the original value for the rest. Note that larger strain value will also lead to a worst aging performance [23], so a carefully decision about the optimum strain value must be taken. As the global cell strain (mobility) is increased equally for all the cell devices, faster cells are obtained. Fig. 3 shows that an increase of the T1 mobility ($k_n > 1$) would reduce the RT values of the memory cells. Meanwhile, the strain relevance is much lower for the gate diode (D1). The relevant influence of T1 (write access transistor) in the RT will be taking it into consideration for the 3T1D development, since this is the key parameter of the cell.

4. Optimization of the eDRAM cells

To achieve the best performance of the eDRAM cell, we simulated different scenarios always looking for a better cell behavior (larger RT).

4.1. **Impact of channel materials and device topology**

To improve the device behavior, a more complex approaches may consider changing together their materials and topology [24], by using III-V channels and a fin topology. The former takes advantage of a more standard device structure and by a not trivial channel material change a relevant device behavior improvement is obtained. The relevance of this topology change can be observed as FinFETs have become the current device manufactured for technology nodes beyond 22nm. We simulated the 3T1D cells by using these two proposals and we compared with the bulk MOSFET. Fig. 4.a illustrates the memory behavior (RT and PW) for each technology when V_{DD} is swept (0.4 - 1V). FinFET-based memories show the best overall cell behavior since they present the highest RT and the smallest access times (WAT and RAT [24]). Besides, III-V/Ge-based cells present the lowest RT and worst PW. We attribute these results to the higher leakage currents present in bulk and III-V/Ge technologies, in contrast to the FinFET one [5].

The environment temperature on 3T1D cell behavior was analyzed, and a clear dependence on it was observed, since the stored voltage is highly temperature dependent [25]. Fig. 4.b shows their impact on the 3T1D cells based on the different technology alternatives. Although the lowest RT value was shown for III-V/Ge devices, these present the lowest RT variation as temperature changes; in contrast to a significant RT reduction for the FinFET-based cells. This can be attributed to the self-heating effect produced in the FinFET structures [26], what when coupled with the high dependence of the RT on temperature [25] by leading to their significant shrink. So from this study we stated the use of FinFET device as a baseline device to enhance the eDRAM memory cells performance.

4.2. **3T1D cell optimization configuration**

Once we have stated FinFET devices as the best option to enhance the 3T1D-eDRAM behavior, we were interested to compare the 3T1D cell with other eDRAM cell proposals [13], e.g. 2T, 2T1D, 3T. First, we studied the V_{DD} relevance on the different eDRAM cells behavior with different configurations: a) nMOS-based (lines), b) pMOS-based (dash) and c) mixed (dotted). This mixed configuration follows the previous studies presented (Fig. 3), where the T1 device shows a relevant impact on the RT evolution of the 3T1D-eDRAM cell. For this, we define this device as a pMOS (less leakage) and the rest of the cell devices as nMOS. Fig. 5a shows the nMOS-based memories with the lowest RT values. When we compare the 3T1D cell performance fully simulated by pMOS, nMOS devices and by properly mixing both in the cell configuration. The former shows the highest RT values at every V_{DD}, whereas nMOS

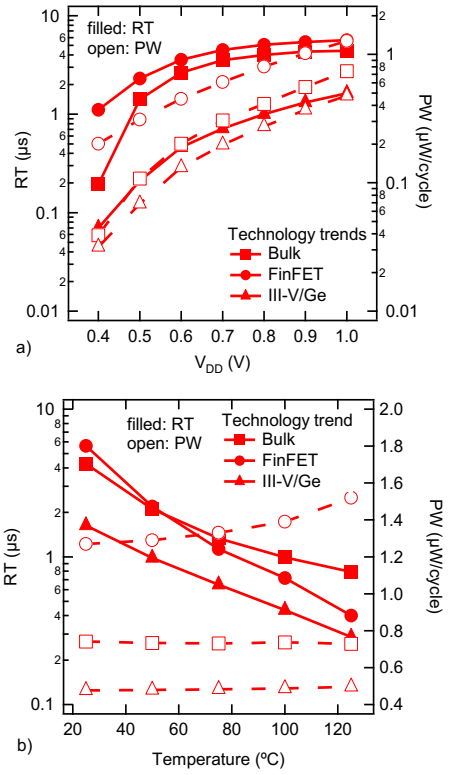

Figure 4. Impact of each technology option on 3T1D-eDRAM behavior measured as RT–PW, when a) V_{DD} is swept (0.4 – 1 V) and b) environment temperature is swept up to 125 ºC.

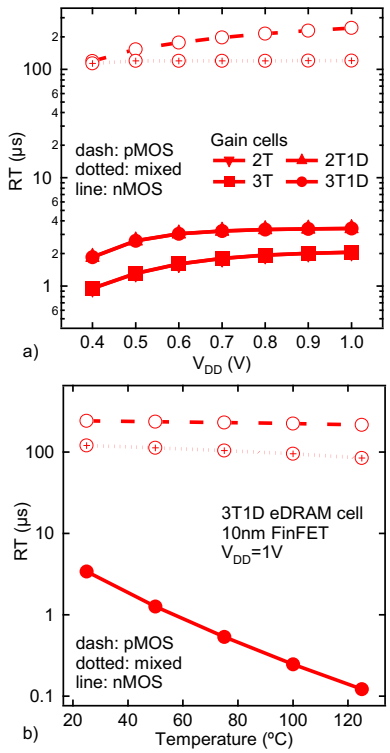

Figure 5. Impact of V_{DD} (a) and environment temperature (b) on the eDRAM cell performance, when all cell configurations are compared and different device types are used.

depicts always the smallest ones, due to their larger leakage currents. In the case of mixed cells, a high RT value is also observed, and we obtain a negligible influence of the V_{DD} sweep, showing a more stable behavior as V_{DD} scales down. Regarding environment temperature impact, Fig. 5b illustrates a significant reduction (>20X) in RT for nMOS cells as temperature increases, in contrast to the almost negligible effect for both pMOS and mixed ones. This poor behavior of the nMOS cell is again related to their larger leakage currents.

4.3. **Impact of the FinFETs topology on eDRAMs**

Memory design is always featured to be implemented to achieve the smallest area cell as possible, to obtain a denser circuitry with lower cost per chip. For this, FinFET use would enhance this relevant design aspect. Note that FinFETs are discrete devices, and their width is mainly limited by the fin height. Thus, the final device width can only be adjusted to the circuit requirements by modifying the number of fins. Indeed, FinFET area is mainly determined by the fin pitch, and as many fins are contemplated larger designs are implemented. To do so, we simulated [13] our cell with two different fin heights that involves a change of the FinFET aspect ratio (AR), determined by the ratio of the fin height (h_{FIN}) and fin thickness (t_{FIN}). The AR shift allows a higher layout area efficiency, but with a trade-off in design flexibility.

Then, seeking a more compact cell design one strategy can be the use of a multiple fins heights [27]. In this context, we design the 3T1D-eDRAM cells layout with two different fin heights, i.e. with two aspect ratios, one for the small devices and another for the wider ones, to try to optimize their layout. The cell area is computed, and this can be used to increase the aspect ratio of the wider devices [28] (D1 and T2, Fig. 1) and eventually reduce the overall cell area. We impose the cell performance to be -at least- the same as with the original aspect ratio. Fig. 6.a shows that increasing the cell aspect ratio the cell performance is maintained. The original aspect ratio value is set at ~2.5 [16]. To analyze the impact of AR change, we increased it to 3 and 4, by getting a consequent cell area reduction of ~5% and 10-20%, respectively. With these results we can consider the suitability of a multiple fin height strategy, since we significantly reduce the cell area. It should be noted that this results would be the same whether the cell is fully implemented by pMOS or nMOS FinFETs, since the same design rules would be used. Nevertheless, obviously, in the case of the mixed cells a larger cell area should be expected, since two different wells are required. But, in order to optimize the cell area a neighboring cell strategy [29] can be implemented to minimize the area overhead. Fig. 6.b depicts the relative cell area for the different gain-cell eDRAM

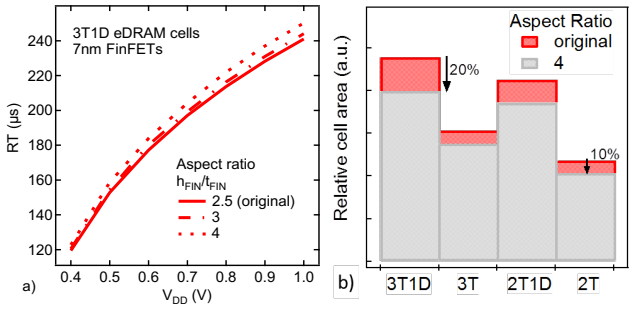

Figure 6. Multiple fin height proposal introduction into the gain-cell 3T1D-eDRAM cell implementation. The same RT performance is ensured when the aspect ratio is increased (a). Larger relative eDRAM cells area reduction is observed for both gated-diode cells (b) [13].

simulated; and while both gated-diode eDRAM cells (2T1D and 3T1D) require the largest cell area the aspect ratio reduction is larger (~20%) when a different AR is simulated for these gain-cell cells .

5. 3T1D cell suitability to operate at sub-V_T level

The reduction of the power consumption is always a milestone for every memory cell. Their suitability for the IoT environment and healthcare applications requires ultra-low power consumption. So, a valid strategy is design a memory cell able to operate at sub-V_T range. Then, we studied how to design the 10 nm FinFET-based 3T1D-eDRAM cell to be feasible at sub-V_T regime. Usually, for good sub-V_T memory cells behavior the device dimensions are resized to enhance their drive current [30]. We studied a resizing strategy of all cell devices by using: a) 2W, b) 2L, c) 2WL, and d) mWL. The mWL configuration is based on an enlargement of the channel length of the write access transistor, while the W dimension was increased for the rest of the cell devices. Fig. 7 points out larger RT when the cell dimensions were upsized. Specifically, when only the W or L was increased, a change on RT trend was obtained for the whole studied V_{DD} range (0.16 – 0.3 V). While the 2L-based cell had a better RT (2x) at the ultra-low V_{DD} level (0.16 - 0.24 V), beyond that point, the RT values tended to be similar to those of the nominal cell. In contrast, the opposite behavior was observed for the 2W cell: although the RT was initially almost the same as the nominal proposal, it improved (2x) as the V_{DD} increased. It is worth noting that the RT cross-point was observed around 0.25 V, close to the threshold voltage of the 10nm PTM pFinFET devices used in this study for the write access transistor. For the 2WL proposal, the RT showed a more uniform increase (2x) as compared to the nominal cell for the entire V_{DD} range. Finally, the largest increase in RT (3.5x) was obtained with the mWL strategy. This improved behavior of the asymmetrically upsized 3T1D-eDRAM cell can be explained by the larger sub-V_T slope values and lower I_{off} as L increased in the write access pFinFET. These results corroborate the larger RT values obtained when the gain-cell devices are up-scaled [31] in other memory cells and using different technologies.

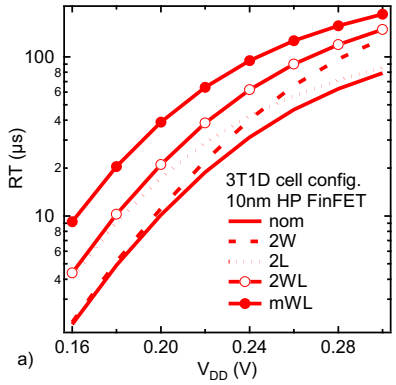

Figure 7. RT as a function of V_{DD} (0.16 - 0.3 V) when different 3T1D-eDRAM device dimensions were considered.

Another key parameter for the memory cell suitability is the working frequency determined by the longest access time (read or write) of the memory cell. In terms of access times, as expected, the different device dimensions resulted in a variation of WAT and RAT values. Thus, Fig. 8.a shows the working frequency for different 3T1D-eDRAM cell proposals (nominal, 2W, and mWL). The largest values were obtained for the 2W, due to the larger drive current resulting from the cell devices' doubled W. In contrast, the mWL proposal had the lowest frequency value, although it was still within the usual

operational range (> 100 MHz) of sub-V_T memory circuits. Note that these values are obtained regarding the performance of a single gain-cell memory. It is worth to mention that a full memory data-path is not considered in this work, what could finally involve lower frequency behavior.

Ambient temperature would significantly influence on the different 3T1D-eDRAM cell device size configurations, as it is usually considered a limiting factor of circuit behavior. Fig. 8.b shows how temperature variations affect RT values. As temperature increases, we observe a relevant RT reduction at ultra-low V_{DD}, due to the larger relevance of the leakage current, in relation with the large impact on I_{SUB} -driving current of the sub-V_T circuits. This study compared the nominal-dimension cell with the mWL proposal. In general, all the cells had longer RTs when operating at -30ºC (significantly so at ultra-low V_{DD}); likewise, all the DRAM cells showed a significant reduction in RT as the temperature rose up to 100 ºC. In particular, the mWL proposal shows less RT degradation (49x) as a result of ambient temperature than the nominal case (64x).

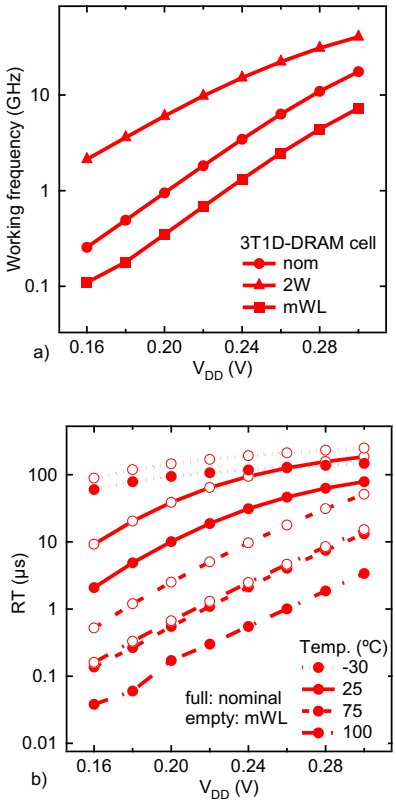

Figure 8. a) Working frequency considered for the different 3T1D-eDRAM cell proposals at sub-V_T level; b) Influence of ambient temperature on the baseline and mixed cell configurations.

6. Reliability study of the 3T1D-eDRAM

Two main reliability subjects threaten the memories behavior as they are scaled down, i.e. device variability and SEU. Next section reviews different results obtained for the corresponding studies focused on device variability [13], [24].

6.1. **Impact of device variability on 3T1D behavior**

For a realistic analysis of the device variability impact, we simulated a complex system based on 3T1D-eDRAM cells. To do so, we computed the manufacturing yield of a 32kB cache memory block based on all FinFETs 3T1D cells, under the different variability scenarios. The circuit was evaluated with a reconfigurable array of 512 cells per column, for 512 columns, followed by 24 redundant columns [32]. For this analysis, 3T1D cells with RTs lower than 714 ns were considered defective, as such an RT value only ensures that the performance loss in a system based on 3T1Ds will be within ~2% of an ideal 6T design [11]. Please note that this RT limit (714ns) could seem a very aggressive statement regarding the refresh period, but there exist different proposals as "refresh-free" cells and dual-ported memories, where refresh operations have priority in one of the ports allowing a better refresh strategy [11]. Fig. 9 shows the RT values for a 32kB memory block based on 3T1D cells with a yield of 99%, when a moderate (20%) variability level is considered. Different 3T1D cell configurations have been analyzed: a) bulk-based, b) III-V/Ge, c) FinFET, sub-V_T and d) mixed gain cell. Mixed gain cells based on FinFET devices present the highest RT value with a yield of 99%. It is important to remark the large RT value of the sub-V_T cells after their device resize.

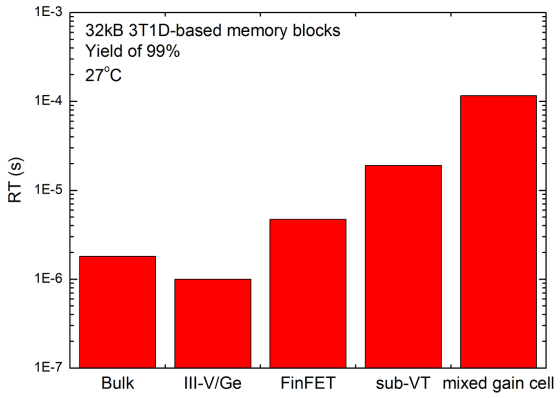

Figure 9. RT values for a 32kB memory block based on 3T1D cells under moderate variability level. Different 3T1D-eDRAM cell configurations has been evaluated.

6.2. **Soft error impact on 3T1D-eDRAM cells**

It is worth noting that to study the soft error impact, we only consider the ion impact produced in the drain regions [20] of the devices connected to the storage node, since it is the most sensitive node of the cell. The device most significantly affected by an ion strike is the write access device (T1), because the other devices are either connected to high capacitance lines, e.g. bit and word line (BL and WL, respectively) [33]. Indeed, this could highly affect the storage node voltage, and consequently the cell RT. First, we have compared the relevance of the 3T1D cell implementation with different device types, i.e Bulk, III-V/Ge and FinFET. Fig. 10.a shows that memory cells based on FinFETs have minimal sensitivity to charge deposited by an ion, as larger charge is required to upset the storage node voltage (V_S). We analyzed the SEU robustness in hold mode, i.e. no voltage is applied to the cell. In this context, we impose the time criterion of 714ns in order to retain the stored data. Fig. 10.a shows the lowest SEU sensitivity for FinFET-based cells, since they require a larger injected charge (~5X) to lose the stored data. In hold mode, the required injected charge to upset the node reduces as time goes by, due to the large leakage currents present in storage node.

In the context of the sub-V_T study, we compared the relevance of the different configurations with the upsized

device dimensions used to implement the gain-cell eDRAM when it was designed to operate at sub-V_T level (V_{DD} = 0.2 V). Fig. 10.b shows the influence of the resizing of the device dimensions when considering a V_S-shift of $V_{DD}/2$ (i.e. loss of the stored data) as opposed to the critical charge required upsetting the node. The greatest robustness was observed for the mWL proposals, as a larger Q_{crit} (~1.9x) was needed to upset the storage node. This is related to the relevance of the upsized devices in the SER, specially for the W increase, which significantly affects the node capacitance [21].

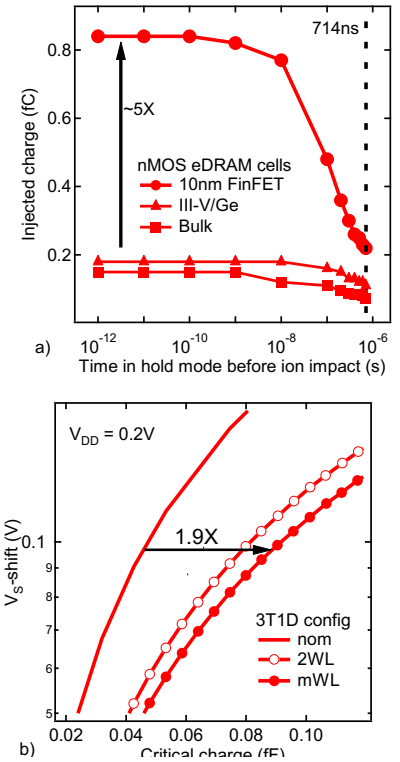

Figure 10. Study of SEU impact into the 3T1D cells configurations. a) In hold mode, the FinFET-based cells show a larger SER robustness, as more IC is required to lose the stored data. b) When the cells are designed to operate at sub-V_T level the largest SER robustness is found for the mWL configuration.

7. SET, future device to implement a memory cell beyond 10nm technology node

Although FinFET device is well established for next technology nodes, beyond the 10nm FinFET seems to present a more cast doubts on future. In this context, researchers are seeking for a future device able to provide a high level of integration and ultra-low power consumption. Single-electron transistor (SET) fulfils both conditions, and arises as a promising option to be considered for next device generations [34]. SET manufacturing process is CMOS compatible, but unlike MOSFETs their channel is definition as a small island, or quantum dot (QD), sandwiched between source and drain regions (tunnel junctions) where a single electron will be located. To be operative at room temperature their QD dimensions should be smaller than 10nm, what involves a high level of integration [35]. Currently, there are a lot of efforts [36] to develop this device and improve its characteristics to operate at room temperature. In fact, there are several works that have simulated the behavior of memory cells based on SET [37] and more complex systems by mainly using SET devices [38]. The benefit of using circuits solely based on SET and FET devices entails a significant reduction of the power consumption in front of the CMOS counterparts [38]. Moreover, a recent study has analyzed the variability impact on SET-based circuits showing a significant small impact on it [39]. Although it is a very relevant device, the fabrication features need device sizes approaching physical limits what involves a relevant development [36].

8. Conclusions

We have reviewed our recent studies focused on a reliability study focused on eDRAM cells performance. The introduction of high-k materials as a gate dielectric, the use of strained channels and the change in device topology (FinFET) have boosted the eDRAM cells performance, e.g. larger RT and higher variability tolerance. To optimize the cell behavior at nominal conditions different device types are merged in a same memory cell, i.e. mixing p-/nMOS devices, to significantly enlarge the retention time of the memory cells. Moreover, the use of FinFET devices allows a relevant reduction of the cell area (~20%) when a multiple fin height strategy is regarded. In the case of memory cell operation at sub-V_T level, we observed that a different relation of the device dimensions have shown as a feasible strategy to enhance the memory behavior. The 3T1D reliability has been studied when it is subjected to device variability and SER and again FinFET-based cell presents the most reliable behavior. Finally, the SET device has been proposed as a possible future device to implement complex circuits (e.g. memories, sensors) for denser circuits and into ultra-low power consumption environment.

Acknowledgements

This work received support from the 2012 Intel Early Career Faculty Honor program. It was also partially funded by the Spanish Ministry of Economics and Competitive (MINECO) and the European Regional Development Fund (ERDF) (TEC2013-45638-C3-2-R) and (TEC2015-69864-R). The European Union's Horizon 2020 research and innovation program founds under grant agreement No 688072 (Ions4SET).

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