

Crystalline silicon solar cells beyond 20% efficiency

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Abstract—This paper describes a fabrication process to obtain high efficiency c-Si cells (> 20%) based on the Laser Fired Contact Passivated Emitter Rear Cell (LFC-PERC) concept. Photovoltaic efficiencies beyond 20% have been achieved using thermal SiO₂ as a rear passivation layer on 2 cm x 2 cm solar cells with 0.45 Ωcm Fz c-Si substrates. Efficiencies up to 22% are expected for material resistivities in the 0.4–5 Ωcm using an optimized rear contact grid.

Keywords- solar cell; laser-fired contact; crystalline silicon; high efficiency; light induced plating;

I. INTRODUCTION

In LFC-PERC solar cells (see Fig. 1), a laser fires the aluminium through a dielectric passivation layer, e.g thermal SiO₂ or Al₂O₃ (Atomic Layer Deposition ALD deposited), into the silicon wafer to form the rear electrical contacts to the p-type c-Si bulk [1]. This laser technique is a cost effective interesting alternative for the fabrication of both laboratory and industrial scale high efficiency c-Si solar cells. LFC processing has been successfully applied to form the rear contact of PERC high efficiency c-Si solar cells with photovoltaic efficiencies higher than 20% using several passivation dielectric materials at the rear side [2] [3].

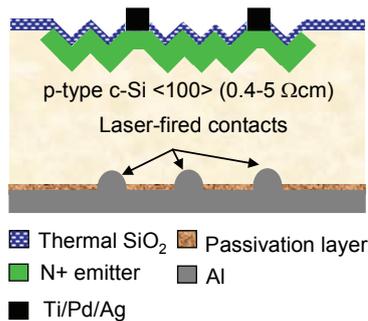


Figure 1. LFC-PERC solar cell concept.

II. BASELINE FABRICATION PROCESS

Solar cells have been fabricated in p-type <100> FZ c-Si 4” wafers with resistivities ranging from 0.5 to 5 Ωcm. The main stages in the fabrication process (see Fig. 2) are: a) the process starts with a thermal SiO₂ growth (240 nm thick) to mask texturization and phosphorous diffusion. b) Inverted or random

pyramids are created in active zone using anisotropic etching with TMAH. c) Phosphorous diffusion is made using planar diffusion sources creating a homogeneous emitter (70-150 Ω/sq). d) After remove mask SiO₂, e) a high quality thermal dry 110 nm thick SiO₂ film is grown for passivation and antireflection coating purposes. Simultaneously phosphorous is driven-in to the final doping emitter profile. Alternatively, rear passivation layer can be changed at this stage etching rear SiO₂ layer and depositing another passivation film (e.g Al₂O₃ by ALD technique). f) Aluminum evaporation on both wafer sides. A sintering step (*annealing*) with forming gas is performed at T=425°C t=10 min to improve front and rear surface passivation. g) Front Al etching in active zone. h) Front contacts are opened and e-beam metallization of Ti/Pd/Ag (35/35/1000 nm) is made. Front grid metallization is patterned by lift-off and a last annealing at T=370°C t=20 min is carried out to recover damage in the e-beam deposition and to ensure good ohmic contacts. i) LFC process at the rear side using a IR (1064 nm) Nd:YAG pulsed laser and finally j) a silver Light Induced Plating LIP stage to thicken the Ag layer in fingers (~5 μm) and busbar (~25 μm) (see section III for details).

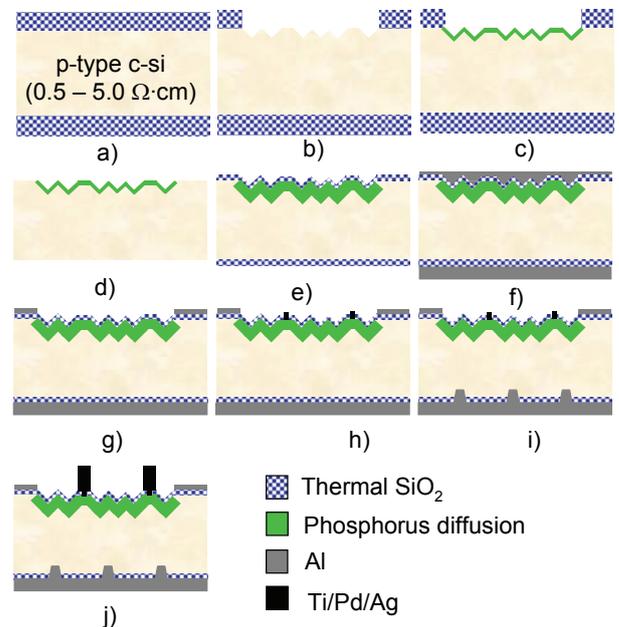


Figure 2. Main stages in the LFC-PERC solar cell fabrication.

III. OUTSTANDING TECHNOLOGICAL FEATURES

A. Low front metallization resistance

Front metallization grid is designed to have low shadow losses (<3%) with a little impact in the series specific resistance ($\sim 0.25 \Omega\text{cm}^2$). This goal is achieved combining standard photolithography to define front metallization grid, with thick silver layers (up to $50 \mu\text{m}$) grown by Light Induced Plating LIP [4]. The working principle of the LIP process is sketched in Fig. 3. In the LIP process a solar cell is placed in an illuminated electroplating bath. The bath consists of a cyanide-free solution (ENLIGHT™ 620 Rohm and Haas Electronic Materials) that is kept to a constant temperature ($35\text{-}40^\circ\text{C}$). The rear side of the cell is connected to the negative electrode of a dc voltage source. The positive electrode of the power supply is also connected to a silver anode placed inside the electrolyte. The anode provides the positive Ag ions necessary in the silver growth. The solar cell emitter is on a negative potential and attracts positively charged Ag metal ions to the front metallized areas. In the process photogenerated electrons recombine with the Ag ions and then the silver is deposited onto the existing metal layer (seed).

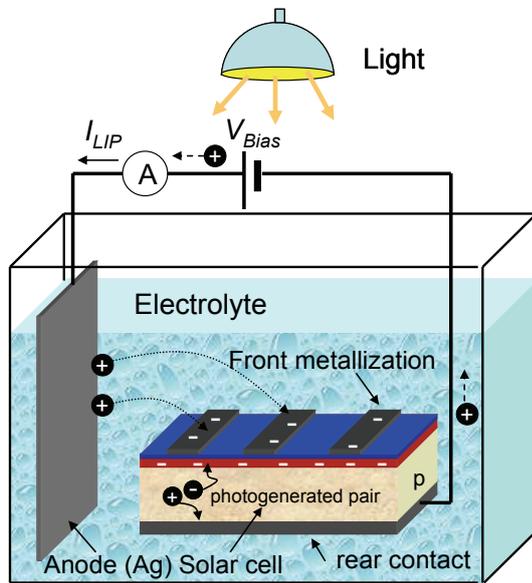


Figure 3. Scheme of the Light-Induced Plating process.

LIP is especially beneficial for solar cells, since it is not necessary to contact the narrow lines of the front side. On the other hand, the fully metallised Aluminum rear side is easy to contact. LIP growth can be selective using photoresit as a mask in the growth, see Fig. 4c, allowing high aspect ratios (up to 2:1 depth:width). Deposition rates, ranging from 0.1 to $2 \mu\text{m}/\text{min}$ typically, can be easily controlled adjusting the light irradiance and monitoring the current I_{LIP} in the external circuit during the LIP process. High light irradiances (high I_{LIP} currents) increase rate deposition but the metal layer quality is poorer (higher porosity) than the case of performing the LIP process at lower rates, affecting adherence with the seed (see Fig. 4(d)) in very thick Ag layers, and increasing metal layer sheet resistances.

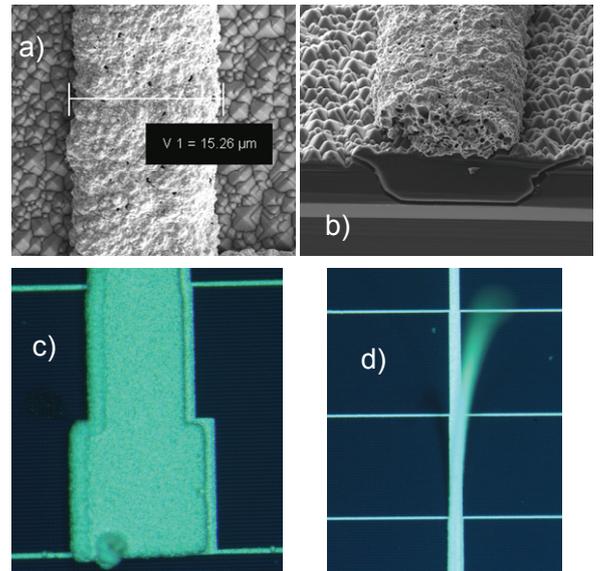


Figure 4. a) A close view and a cross section SEM image of a finger after the LIP process is concluded. The silver layer was thickened to $\sim 5 \mu\text{m}$ with a deposition rate of $\sim 0.5 \mu\text{m}/\text{min}$. b) A cross section SEM image of a finger.

Porosity of the silver layer grown can be seen clearly. c) An optical microscope image of the busbar (pad electrode) after a second selective LIP stage. d) Loss of adherence of a thick layer ($\sim 50 \mu\text{m}$) deposited with a very high rate ($4 \mu\text{m}/\text{min}$).

B. Low front reflectance

Weighted reflectances R_W 's, below 5% have been measured in our devices considering the AM1.5G spectrum using inverted or random pyramids (see Fig. 5). Optical confinement is improved thanks to a back reflector consisting of $110\text{nm-SiO}_2/2\mu\text{m-Al}$.

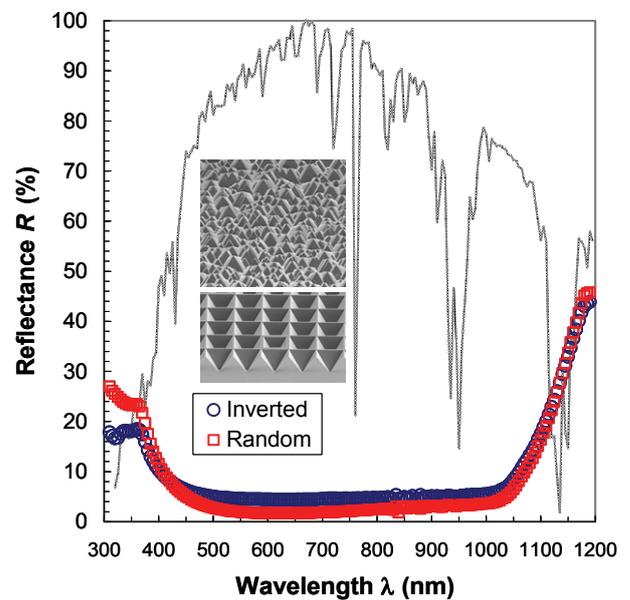


Figure 5. Measured reflectance for our textured surfaces using inverted or random pyramids (see SEM images in the inset). Normalized spectral density of photons considering AM1.5G solar spectrum is also included in the graph.

C. Low front and rear surface recombination

To preserve lifetime and surface passivation RCA1 and RCA2 cleaning sequence was used before each high temperature process. Additionally thermal oxidations were performed with Dichloroethylene DCE ambient and oxidation tubes were also routinely cleaned with DCE. In fact excellent rear passivation with surface recombination velocities SRV's lower than 25 and 2.5 cm/s for thermal SiO₂ and ALD Al₂O₃ films respectively. SRV values are extracted at @1Sun level injection from QSS-PC lifetime measurements (see Fig. 4) using (1), where W is the wafer thickness, S_{Rear} the SRV at the rear surface and τ_{in} the intrinsic bulk lifetime limited by the Auger and band to band recombination mechanisms [5].

$$\frac{1}{\tau_{eff}} \cong \frac{2S_{Rear}}{W} + \frac{1}{\tau_{in}} \quad (1)$$

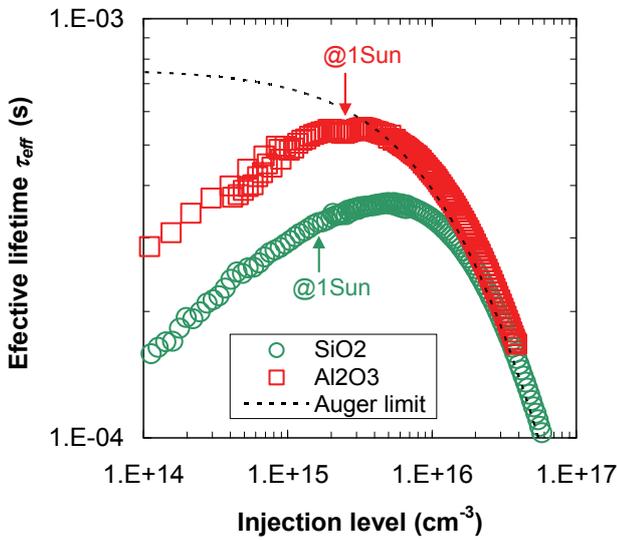


Figure 6. Effective lifetime vs. injection level using QSS-PC lifetime measurements for two samples passivated (both surfaces) with 110 nm thermal SiO₂ and 50 nm ALD Al₂O₃. Samples were annealed with forming gas 425°C 10 min. 0.45 Ωcm 280 μm thick substrates were used.

On the other hand front surface passivation have been determined extracting emitter saturation current density J_{oe} from QSS-PC measurements (see Fig. 7) using (2) [6]. Where N_{Bulk} is the base p-type doping and n_i the intrinsic carrier concentration ($8.65 \times 10^9 \text{ cm}^{-3}$ @25°C).

$$\frac{1}{\tau_{eff}} \cong \frac{1}{\tau_{in}} + \frac{2J_{oe}(\Delta n + N_{Bulk})}{qn_i^2 W} \quad (2)$$

Taking into account data shown in Fig. 7, we can conclude that an outstanding J_{oe} value ~50 fA/cm² are achieved in our fabricated emitters, considering a contribution of 40 fA/cm² and 850 fA/cm² of passivated and contacted regions (1.5% is contacted) respectively.

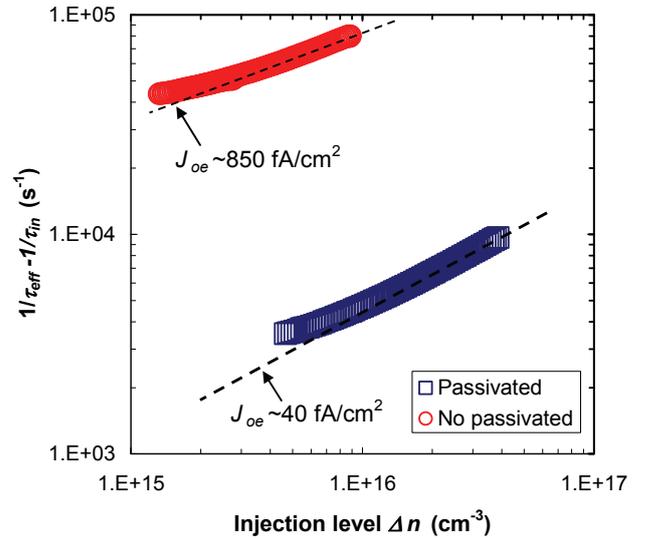


Figure 7. $1/\tau_{eff} - 1/\tau_{in}$ vs. injection level using QSS-PC lifetime measurements for a symmetrical n+ doped (70 Ω/sq) textured (random) sample after drive-in. Surface was passivated with 110 nm thermal SiO₂ annealed with forming gas 425°C 10 min (square blue symbols). The same sample was also measured after etching SiO₂ (circle red symbols). A 2.4 Ωcm 265 μm thick substrate was used.

D. Optimized Laser-Fired Contact LFC process

Laser-fired process has been optimized (power and number of laser pulses) to obtain very low specific contact resistances at the rear LFC points (below 0.05 mΩcm²) using several passivation rear layers [7]. Furthermore rear contact grid has been designed as a trade-off between base resistance and passivation at the rear side as it is explained in detail in reference [8]. For instance, photovoltaic efficiency η vs. contacted fraction area f_c is shown in Fig 8.

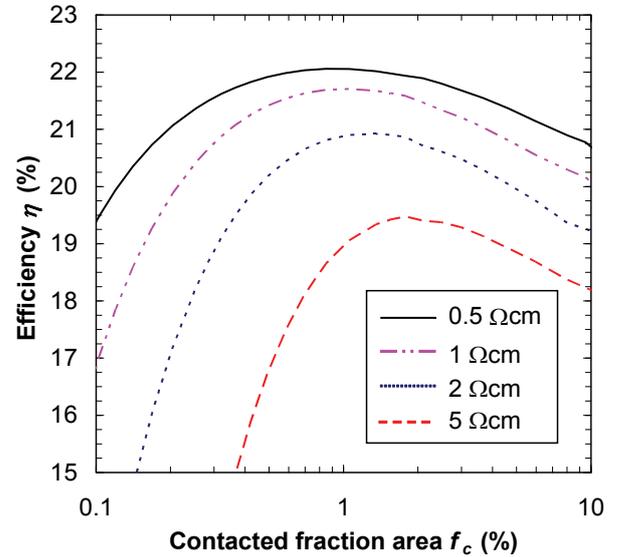


Figure 8. Simulated photovoltaic efficiencies vs. contacted fraction area f_c considering no passivation at the contacts. A rear SRV of 10 cm/s (non-contacted regions) and a laser spot radius of 50 μm have been considered.

This study is a worst case considering no back surface field at the contacts. Maximum efficiencies ranging from 22.0% and 19.5% are possible using f_c 's between 0.8 and 3% depending of the substrate resistivity, corresponding with pitches p 's between LFC points between 1 mm to 0.5 mm respectively.

IV. RESULTS AND CONCLUSIONS

Fabrication process has been evaluated using p-type Fz c-Si single side polished 4" wafers (0.45 Ωcm 280 μm thick). Inverted pyramids were used to reduce front reflectance and emitter and rear surface were passivated with *Aln* thermal SiO₂ (425°C 10 min). Laser firing processing was performed using 3.9 W laser power (8 kHz pulse repetition frequency) and 125 pulses were used in each LFC point.

Electrical measurements, current voltage I - V and power voltage P - V characteristics, have been obtained using standard test conditions (AM1.5G @1 kW/m², T=25 °C) as it can be seen in Fig. 9(a). Photovoltaic efficiency values higher 20% for 1 and 4 cm² cells (see table I) have been achieved with outstanding photocurrent densities J_{ph} 's up to 40 mA/cm². The External quantum efficiency EQE of the best 2 cm x 2 cm cell is also shown in Fig. 9(b).

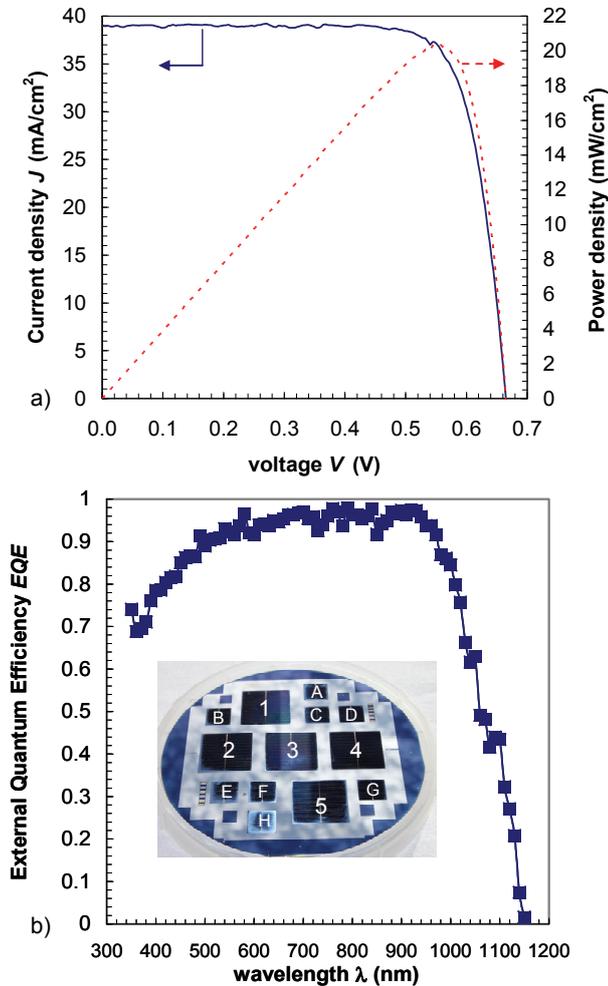


Figure 9. a) Measured Current density and power density vs. voltage, and External quantum efficiency EQE b) for the best 2 cm x 2 cm (cell 4). Device labelling is shown in the inset of Fig. 9(b).

TABLE I. MAIN PHOTOVOLTAIC PARAMETERS FOR SOME FABRICATED LFC-PERC SOLAR CELLS.

Cell	Area (cm ²)	p (mm)	f_c (%)	J_{ph} (mA/cm ²)	V_{oc} (mV)	FF (%)	η (%)
# E	1	0.4	4.9	38.04	650	78.47	19.40
# G	1	0.7	1.6	39.12	665	79.02	20.59
# D	1	1.0	0.78	38.34	670	80.51	20.68
# A	1	1.4	0.4	38.75	670	78.93	20.49
# 1	4	1.0	0.78	38.90	663	78.48	20.24
# 4	4	1.0	0.78	38.93	665	78.91	20.43
# 5	4	1.0	0.78	39.96	663	76.26	20.20

Comparing experimental results with simulations (see Fig. 8) we conclude that efficiencies closer to the simulated values are possible ($\sim 22\%$). This goal will be achieved in future devices, increasing Fill Factor FF ($\sim 81\%$) and open circuit voltage V_{oc} (~ 680 mV) by decreasing leakages currents (diode ideality factors close to $n=1$, now $n\sim 1.3$), improving rear passivation with the use of Al₂O₃ films and optimizing the growth of silver in the LIP stage.

ACKNOWLEDGMENT

Authors wish to thank to Saint-Gobain Advanced Ceramics Corp. for the delivery of Planar Diffusion Sources (PDS[®]), as well as the Centre de Recerca en NanoEnginyeria CRNE to use their facilities and to Dr. Trifon Trifonov for his help and comments to obtain the SEM images. And finally authors like to express special thanks to Dr. Michael Vetter for his initial contribution in developing the technology to manufacture high-efficiency solar cells in the MNT group.

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