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Approach to the Modeling of LDO-Assisted DC-DC Voltage Linear Regulators

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Abstract. This paper presents the design of a LDO-assisted DC-DC converters in Cadence Virtuoso based on a 350-*nm* CMOS technology. This kind of voltage regulators consists of a switching converter together with a classic or LDO (low drop-out) linear voltage regulator. While the linear regulator provides the constant output voltage, the switching converter conducts nearly all the current provided in the output load, and keeping the regulator current close to zero where the higher efficiency is achieved. In addition, current article shows the modeling in Matlab/Simulink. This modeling is mandatory in order to predict and assure the stability of the circuit. In addition, it can allow improving the performance of the circuit.

Key words

DC-DC converters, LDO regulators, Power electronics, Matlab/Simulink

1. Introduction

There are substitute renewable energies that are known as a technology, which will be fundamental component of electrical energy grid in the future that require power electronic devices to enlarge the possibility of integrating into the grid since they cannot be connected directly. As Power converters are quite more flexible in terms of control, have become the most concerning technology for researchers in modern power system. DC-DC power converters are widely used in variety of applications in terms of their high efficiency and low output ripple, such as portable devices, energy-harvesting applications and Radio Frequency (RF) power amplifiers that are in need of highly efficient and stable power supply [1, 2, 3].

There are two approaches for the design of DC-DC power converters such as using either the switching regulator or the linear regulator. DC-DC switching regulators could provide ripple in the output voltage due to the switching process. Thus, the use of linear regulator would be necessary to eliminate this ripple and produce the surplus of the current that is not provided by the switching regulators [4]. The linear-assisted hybrid converters usually consist of a switched capacitor (buck) converter with a linear regulator (standard NPN Darlington, LDO or quasi-LDO) to conduct the desired current in the output load with regulated constant output voltage. Previous researches have been done to minimize the existing impediments such as low efficiency and high power dissipation [5, 6]. Other researches have proposed topologies to optimize the performance of buck converter or improve the control techniques [7, 8, 9]. Another have optimized the design using push-pull linear regulator [10].

In this paper, a Low Dropout (LDO) regulator is used that has benefits of maximizing the usage of available input voltage and can yet regulate the input voltage while the input/output values are close and has the minimum internal power loss. In this structure, the conventional linear regulator is replaced by LDO to obtain the better performance (lower output ripple and better efficiency) and the circuit modeling is presented to analyze the stability based on critical parameter's variation. In this article, a proposal of linear-assisted DC-DC converter and its modeling is presented to inquire the control loop stability. In fact, in order to carry out the stability study, a model of the whole system is necessary.

2. Structure of the proposed LDO-assisted converter

In the proposed circuit shown in Fig. 1, the switching converter is connected in parallel with a LDO regulator, providing the desired output current and voltage by the load. As it is well known, the LDO regulator with the feedback loop of R_1 and R_2 continuously compares the reference and the output voltages in the input ports in order to provide a constant output voltage. This output voltage is given by:

$$V_{out} = \left(1 + \frac{R_1}{R_2}\right) V_{ref1} \tag{1}$$

Since the output current is obtained by the sum of both the linear regulator and the switching currents, and is a constant value (in steady state), the conduction and cut off

the switch is controlled by the comparator (*CMP*) to conduct the majority of the output current by the switching converter. Consequently, the analog comparator compares a reference voltage, V_{ref2}, with the regulator's sensed current flowing through the linear regulator. This reference voltage, V_{ref2}, fixes a boundary current or threshold current, to control the switching frequency. The current sensing through the linear regulator is done by a low-value resistor (1 ohm in this case), and is defined by the following expression:

$$I_{\gamma} = \frac{V_{ref\,2}}{R_{sense}} \tag{2}$$

When the load current is below the threshold current, the output of comparator will be low and will set the switch off. Thus, the current through the inductor L will decrease, and the regulator current will increase to provide all the output current that flows through the load. However, on the other hand, when the load current increases, the comparator will pass to high and turns on the switch of the switching converter. Therefore, the inductor current I_L will increase. This makes the regulator current to decrease linearly as it can be seen in Fig. 2. All the simulations are based on a 0.35-µm CMOS technology in Virtuoso Cadence.

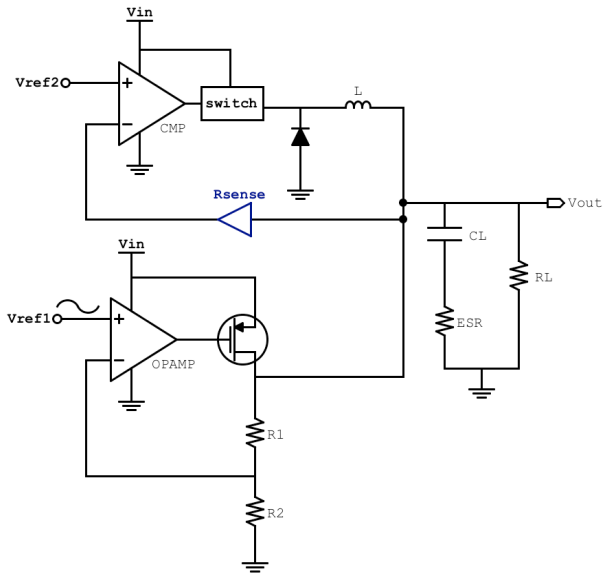

Fig. 1. Proposed schematic of the LDO-assisted DC-DC converter.

In this simulation, with the input voltage of 3.3 *V*, a constant value of 1.65 *V* is obtained at the output terminals, and the load current is fixed at 100 *mA* that is mostly provided by inductor current. Therefore, it keeps the regulator current close to zero. In Fig. 3, the transient response of the circuit with the variation of V_{in} from 3.3 *V* to 4.3 *V* is shown, and it demonstrates a good line regulation as well as the load regulation from 200 *mA* to 300 *mA* variation of load current I_{out}.

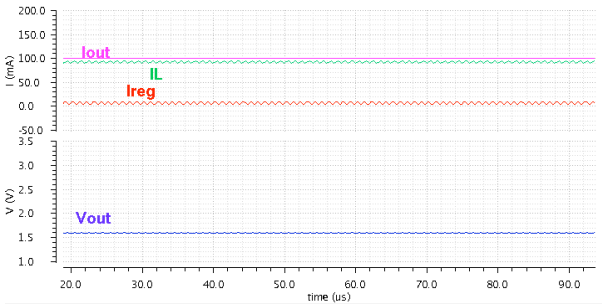

Fig. 2. Transient response of the proposed dc/dc converter

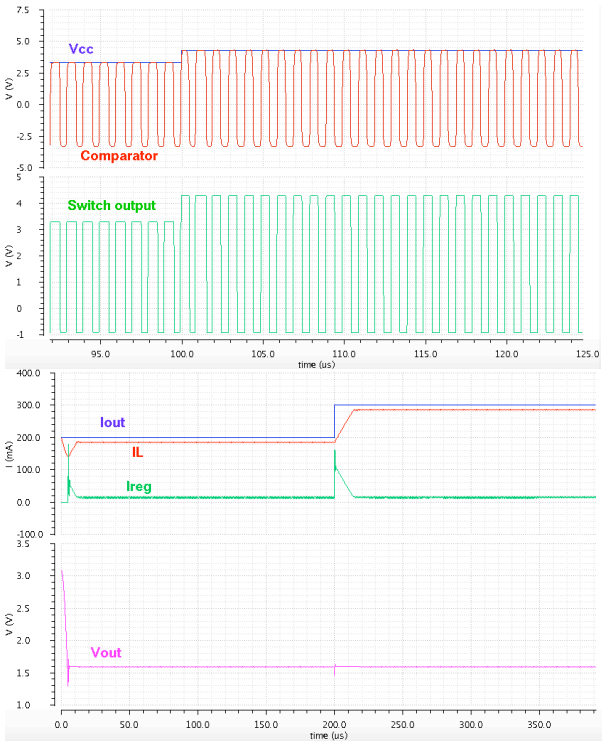

Fig. 3. Transient response for the line and load regulation respectively

3. Modeling of the proposed circuit

It is necessary to study the mathematical modeling of the proposed circuit to consider the critical parameters of the circuit, and analyze the circuit's behavior (possible instabilities) by the variation of those values to observe the stability of the whole system. In Fig. 4, a simplified modeling block diagram of the linear-assisted converter is shown. In this model, the linear regulator current (I_{LIN}) is obtained from the output current, I_{out}, and the switching converter current, I_{sc}:

$$I_{LIN} = I_{out} - I_{sc} \tag{3}$$

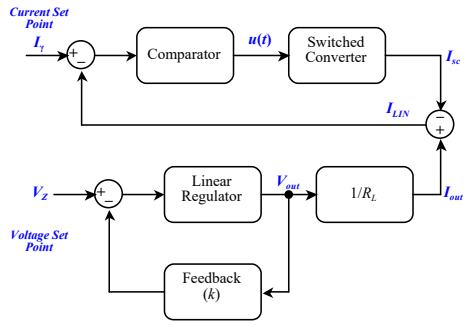

Fig. 4. Block diagram of the modeling of linear-assisted converter.

On the one hand, Fig. 5 shows the DC-DC buck converter circuit. The buck converter is considered with an ideal switch that has the switching period of T. When the switch is ON, the current through the inductor (L), load capacitor (C_L) and its equivalent series resistor (ESR) is derived from the equations below:

$$i_{sc}(t) = i_L(t) - i_c(t) \tag{4}$$

$$i_L(t) = \frac{1}{L}\int\left(v_{in}(t) - v_{out}(t)\right)dt \tag{5}$$

$$v_{out}(t) = v_c(t) + v_{ESR}(t) = \frac{1}{C}\int i_c(t)\,dt + ESR \cdot i_c(t) \tag{6}$$

$$i_c(t) = C\frac{dv_{out}(t)}{dt} - C \cdot ESR \cdot \frac{di_c(t)}{dt} \tag{7}$$

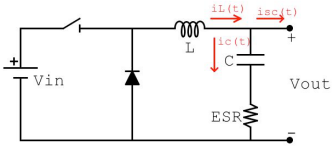

Fig. 5. Basic DC-DC buck converter circuit.

The obtained expressions (5) and (7) are implemented in Matlab/Simulink® as indicated in Fig. 6 using linear blocks (summing, gains, etc. blocks) subsequently applied to integrator and derivative blocks in order to obtain the switching converter's output current (i_{sc}). The inductor value used in simulation is 200 µH.

On the other hand, the linear regulator block consists of an error amplifier (Fig. 7), pass transistor and the feedback loop. To obtain the transfer function for each block, the equivalent circuits are shown below. The transfer function of the operational amplifier is given by equation (8) and it demonstrates two poles (P_1, P_2) and a zero (Z) made by miller capacitor (C_c).

$$H_{oa}(s) = \frac{V_m}{V_{ref}} = \frac{A_{oa}\left(1 - \frac{s}{Z}\right)}{\left(1 + \frac{s}{P_1}\right)\left(1 + \frac{s}{P_2}\right)} \tag{8}$$

$$\begin{cases} A_{oa} = g_{m1}g_{m2} \times r_{o1}r_{o2} \\ Z = g_{m2}/C_c \\ P_1 = 1/g_{m2}r_{o1}r_{o2}C_c \\ P_2 = g_{m2}/C_2 \end{cases} \tag{9}$$

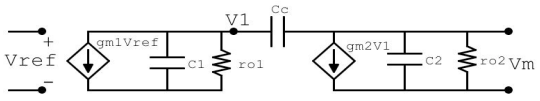

Fig. 7. Operational amplifier's equivalent circuit with miller effect (C_c).

Fig. 8 shows the equivalent circuit of pass transistor and the transfer function of pass transistor is calculated in expression (10) and it depends on the gain of transistor ($g_m r_{pass}$) and its capacitor C_{pass}.

$$H_{pass}(s) = \frac{V_{out}}{V_m} = \frac{g_m \times r_{pass}}{1 + C_{pass}r_{pass}s} \tag{10}$$

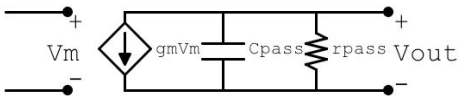

Fig. 8. Pass transistor equivalent circuit

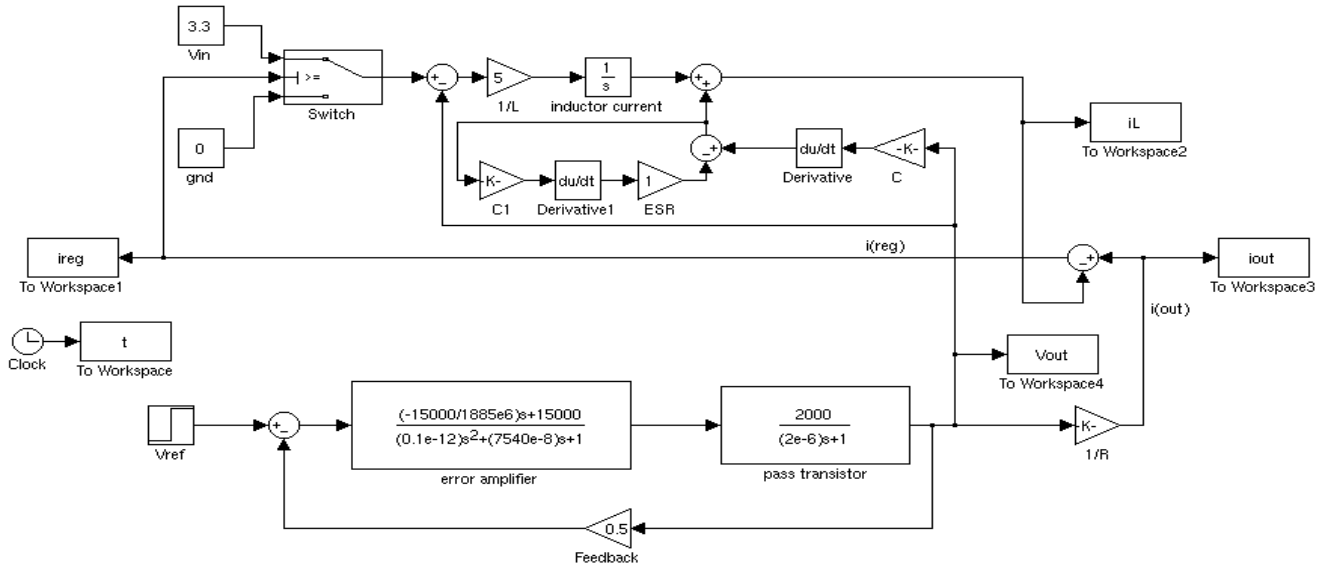

Fig. 6. Proposed linear-assisted converter modeling diagram.

The feedback value that we introduced earlier in equation (1) obtained from the ratio $R_2/(R_1+R_2)$ and is applied to the inverter input of the operational amplifier.

4. Simulations and results

The proposed model that is introduced in the previous section, guaranties the constant output voltage by linear regulator. Fig. 9 indicates the simulation results in Matlab/Simulink® that matches with the results obtained in Virtuoso cadence.

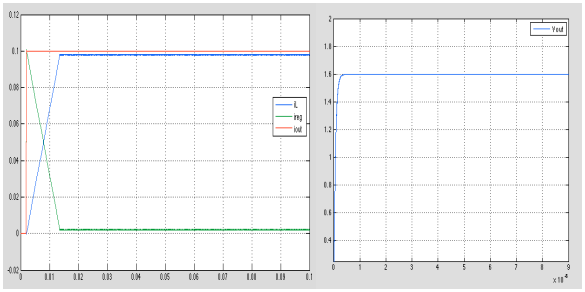

Fig. 9. Transient response of the proposed model in Matlab/Simulink®

The circuit could be unstable due to some parameters such as output capacitor and its equivalent series resistor. In fact, the existence of these parameters is important in order to predict the transient behavior of the converter. The frequency response of the circuit is also quite sensitive to output capacitor (C_L) and its ESR that is connected to the load resistor.

In Fig. 10, experimental results for different values of capacitor C_L are obtained. The closed-loop gain is 6 *dB* since we have an output voltage, two times bigger than input voltage. For an output capacitor of 100 *nF*, the gain and phase margin are 59.8 *dB* and 50 degrees, respectively. In these conditions, the gain margin for C_L=100 *pF* is reduced to 20 *dB*, and phase margin increased to 114º.

As it is obtained in fig. 11, for the C_L=10 µ*F* and ESR=0.1 Ω, a significant reduction in phase margin is observed and by changing the ESR to 1 Ω, gain margin of about 60 *dB*, and phase margin of 117º is calculated. It is also observed that varying the gain of operational amplifier does not affect the stability of the converter.

Since there are just a few capacitors with impedance more than 2 Ω, the upper limit of the ESR can be ignored but the typical lower limit is 0.1 Ω. Fig. 12 shows bode plot for C_L=4.7 µ*F* and ESR=0.01 Ω. It shows phase margin of 5.95° and gain margin of about 99 *dB*, which make the system unstable.

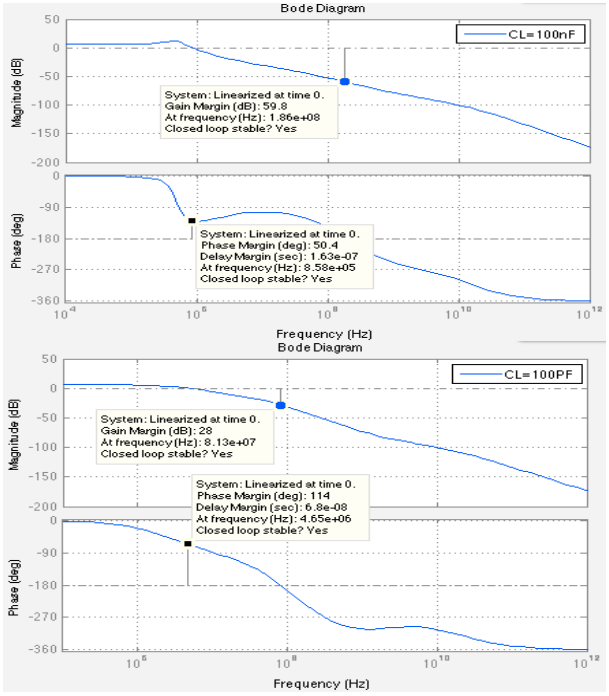

Fig. 10. Bode plot for C_L=100 *nF* and 100 *pF*.

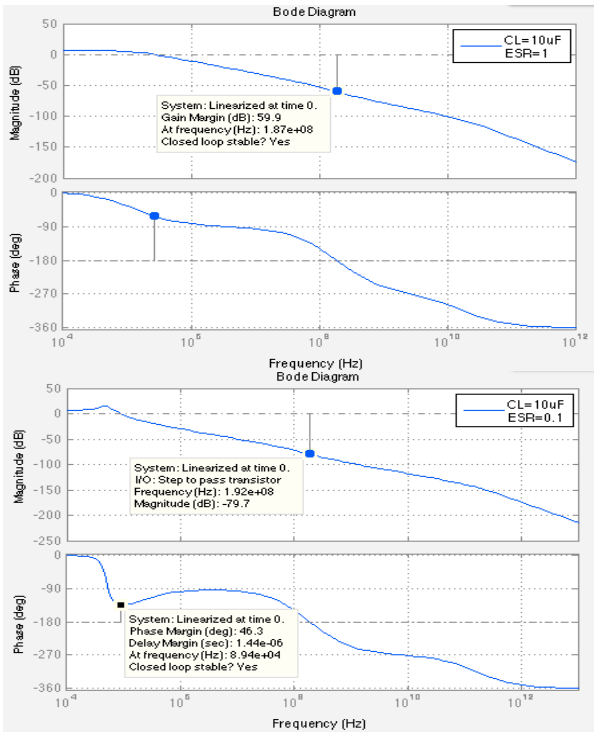

Fig. 11. Bode plot for C_L=10 µ*F*, and ESR=1 Ω and 0.1 Ω

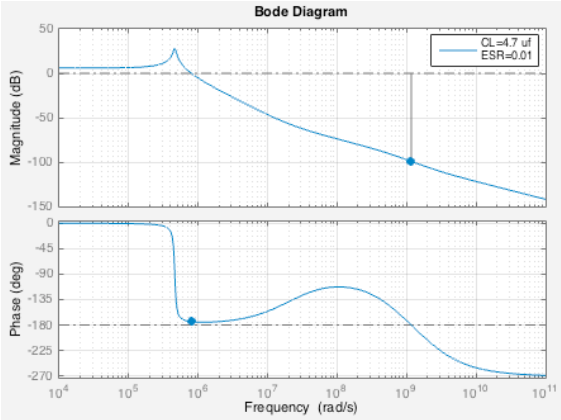

Fig. 12. Bode plot for C_L=4.7 μF, and ESR=0.01 Ω

5. Conclusion

In this paper, the simulation of LDO-assisted DC-DC converters based on 0.35 μm CMOS technology and its modeling in Matlab/Simulink® has been shown. In general, LDO regulators are prone to instabilities due to the position of their poles and zeroes. This is also the case in LDO-assisted topologies.

As a consequence, the proposed modeling will help to characterize the critical parameters such as output capacitance and its equivalent series resistance that have influence on these instabilities. From this modeling the performance of the system could be easily improved by varying the parameters value.

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