

# Second order sigma-delta control of charge trapping for MOS capacitors

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## **Abstract**

This paper presents the circuit topology of a second order sigma-delta control of charge trapping for MOS capacitors. With this new topology it is possible to avoid the presence of plateaus that can be found in first-order sigma-delta modulators. Plateaus are unwanted phenomena in which the control is locked for a certain time interval (possibly of infinite duration). In this case the control output is constant and therefore the controlled device is in fact in open-loop configuration. It will be shown that the presence of plateaus is avoided in MOS capacitors using the proposed approach.

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# Second order sigma-delta control of charge trapping for MOS capacitors

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**Abstract** - This paper presents the circuit topology of a second order sigma-delta control of charge trapping for MOS capacitors. With this new topology it is possible to avoid the presence of plateaus that can be found in first-order sigma-delta modulators. Plateaus are unwanted phenomena in which the control is locked for a certain time interval (of unknown duration). In this case the control output is constant and therefore the controlled device is in fact in open-loop configuration. It is shown that the presence of plateaus is avoided in MOS capacitors using the proposed approach.

## 1. Introduction

Charge trapping is a ubiquitous phenomenon present in almost any device containing dielectric materials. Among the devices for which charge trapping represents a reliability problem we find:

- MOS capacitors and related structures such as ultrathin gate oxides used in MOSFETs [1–4]. Charge trapping generates changes in the threshold voltage of the transistors, among other effects.
- Electrostatic MEMS/NEMS [5–7]. Charge trapping generates shift of the C-V characteristic of the device, shift of the pull-in voltage and even permanent stiction. This has been a particularly difficult problem for RF-MEMS switches [8].
- Organic FETs (OFETS). Charge trapping also generates changes in the threshold voltage of the transistors [9].

In general, this phenomenon alters device performance, affecting its circuitual features and even reducing its effective lifetime. The physical mechanisms responsible for charge trapping are rather complex and dependent on fabrication processes, temperature, and electrical stresses applied to the device [10–14].

Many research works focus on characterization and mitigation of the effects of dielectric charging from very different approaches. For example, specific geometries and dielectricless structures have been proposed for MEMS [15,16], while new dielectric

materials and stack arrangements allowing charge trapping reduction have been proposed for MOS structures [17–19]. Moreover, some circuit strategies to compensate dielectric-related degradation effects during device lifetime have been proposed for specific MOSFET applications [20,21].

Additionally, several actuation strategies using smart voltage waveforms have been proposed to mitigate and even control the effects of dielectric charging in MEMS [8,22,23]. These strategies are based on the opposite effects produced by bipolar voltages on the charge dynamics. Following this complementarity principle, a first order control of charge trapping for MOS capacitors was presented in [24]. This control allows to obtain a desired shift of the C-V characteristic of the device (and hence of the net trapped charge in the oxide) and then to maintain it. This is achieved through a control loop based on sigma-delta modulation that applies a proper sequence of bipolar voltage waveforms to have the average charge injection necessary to keep the desired charge level, see Fig. 1.

However, one of the known problems of first-order sigma-delta modulators is the appearance of plateaus [25]. If the sampling time is of the same order or greater than the shortest time constant of the charging and discharging processes of the device, the control may provide a constant output during certain time intervals in which the system is effectively in an open loop configuration. It must be noted that the charging and discharging time constants will depend on the applied voltages in a nonlinear way and that several processes may coexist in a single device, resulting in a complex dynamics that is generally difficult to predict beforehand.

The objective of this paper is to present a second order control of charge trapping for MOS capacitors. This topology effectively removes the presence of plateaus in the experimental measurements.

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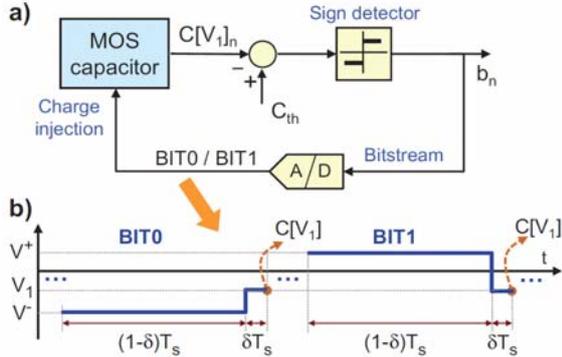


Figure 1: a) Block diagram of the first order sigma-delta control circuit of charge trapping. b) Voltage waveforms applied to the devices.

## 2. First and second order sigma-delta controls

The objective of the control proposed in [24] is to shift the  $C$ - $V$  curve of the device so that the value of the capacitance at a voltage reference  $V_1$  is set to a target value  $C_{th}$ , i.e.  $C[V_1](t) \approx C_{th}$ . To this effect, the sigma-delta loop applies a sequence composed of two voltage waveforms, namely BIT0 and BIT1, to the device. These waveforms are designed to obtain two separate results: 1) to allow periodical monitoring of  $C[V_1](t)$ ; 2) to apply the correct excitation to shift the  $C$ - $V$  in the adequate direction.

The corresponding circuit topology can be seen in Fig. 1. The circuit works at sampling period  $T_s$ . The value of the capacitance of the device at the reference voltage  $V_1$  is measured at times  $t = nT_s$ . Depending on whether the capacitance measured at  $t = nT_s$  is below or above the target value  $C_{th}$ , either a BIT1 or a BIT0 waveform is applied until the next sampling time  $t = (n+1)T_s$ . As commented above, these waveforms have been designed to shift in opposite directions the  $C$ - $V$  curve of the device. This results in a sliding motion in which the control places the device in the surface  $C[V_1](t) = C_{th}$  [26].

The block diagram of the second order control circuit proposed in this work is shown in Fig. 2.a. The main difference with the first-order topology discussed above is the use of an integrator before the sign detector. The addition of this element will result in a second order zero in the quantization noise at the output of the modulator, and also in the disappearance of the unwanted plateaus.

The controller was implemented with an Agilent E4980A precision LCR meter controlled from a computer. The LCR meter allowed both to measure the

MOS capacitance and to apply the voltage waveforms BIT0 and BIT1. The frequency of the AC test signal used in the capacitance measurements is 2 MHz, and the accuracy of such measurements was in the range of fF. A computer program executed the control algorithm following the synchronous strategy of Fig. 2.b.

The LCR meter was also used in open-loop configuration to characterize the MOS capacitors through voltage stress experiments.

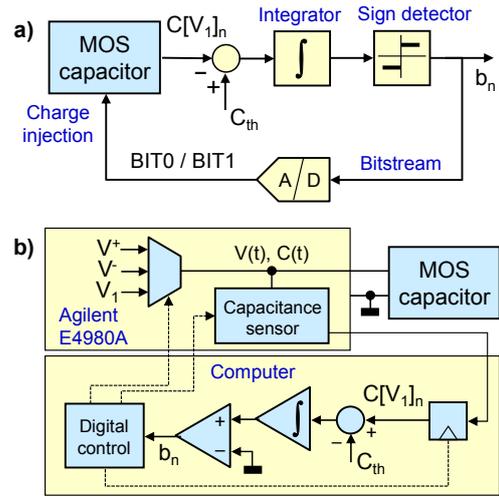


Figure 2: a) Block diagram of the second order sigma-delta control circuit of charge trapping. b) Experimental implementation of the second order control.

## 3. Capacitor fabrication and characterization

The MOS capacitors used in the experiments were fabricated in the Clean-Room facilities of the Technical University of Catalonia (UPC). The substrate was an n-type c-Si  $\langle 100 \rangle$  wafer of 280  $\mu\text{m}$  thick and a resistivity of  $2.5 \pm 0.5 \Omega \text{ cm}$ .

The process starts with a standard RCA clean followed by a thermal oxidation for 45 minutes with a temperature ramp between 850-1000  $^\circ\text{C}$ . A  $\text{SiO}_2$  layer of  $\sim 25 \text{ nm}$  thick is grown on both sides of the wafer. Next, the  $\text{SiO}_2$  of the back side is removed with HF etching, while the front side is being protected with photoresist. Then, Aluminium is deposited at the back side of the wafer by evaporation, resulting in a layer thickness of approximately 700 nm. Finally, the top electrode is conformed via a sputtering deposition of Aluminium using a shadow mask for patterning.

Two capacitors from this batch, labelled as MC-1 and MC-2 from here on, have been used in this work. Both devices have round-shaped contact areas, with a

measured radius of 747  $\mu\text{m}$  for MC-1 and of 819  $\mu\text{m}$  for MC-2. Figure 3.a shows a photograph of MC-1, whereas a vertical cross-section of the devices can be seen in Fig. 3.b.

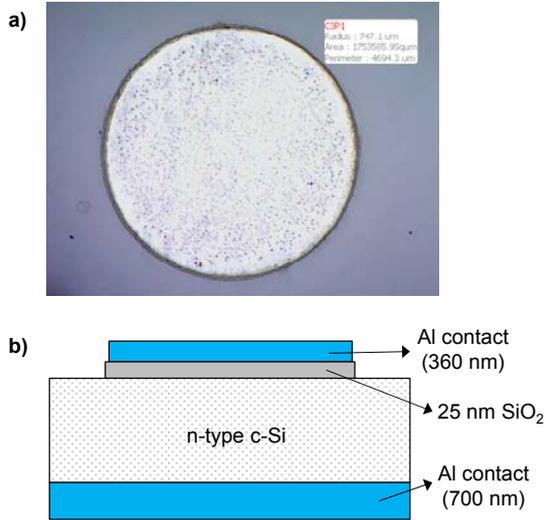


Figure 3: a) Top-view picture of the MOS capacitor MC-1 used in the experiments. b) Vertical cross-section of the devices (dimensions not to scale).

Let us note that the capacitors used in this work have been fabricated using a process similar to that in [24], but in this case no PECVD a-SiC<sub>x</sub> stack was placed at the back side of the wafer, no laser firing for doping was made and no final annealing was made. The objective of these changes was to reduce the built-in charge in the devices. This is seen in Fig. 4, where high-frequency C-V curves measured in pristine devices MC-1 and MC-2 are plotted. The horizontal shifts are around  $-0.5\text{V}$ , a small value against the  $-5.5\text{V}$  range of [1].

Fittings of the experimental C-V curves of Fig. 4 with the analytical model used in [24] have been performed. This model, derived from [9], uses only two parameters related to oxide charges. The first one,  $Q_{\text{ox}}$ , is an equivalent oxide charge that includes three components: 1) fixed positive charge (due to structural defects closer to the Si-SiO<sub>2</sub> interface), 2) mobile ionic charge (due to presence of positive ions such as Na<sup>+</sup> or K<sup>+</sup>), and 3) trapped charge (due to holes or electrons trapped in the oxide bulk). It is assumed that  $Q_{\text{ox}}$  variations produce horizontal-rigid C-V shifts and that both the fixed and the mobile ionic charge components depend on the fabrication process and they hardly vary with device use. Then, it is concluded that the C-V shifts produced by the voltages applied to MOS

capacitors are due to positive and negative variations of the charge trapped in the oxide bulk, being  $Q_{\text{ox}}$  always positive in the cases reported in this work.

The second parameter,  $D_{\text{it}}$ , is the interface trap density at the Si-SiO<sub>2</sub> interface, which produces an amount of charge that can be either positive or negative, depending on the surface potential, thus on the voltage applied. This causes opposite shifts in the accumulation and depletion sections of the C-V, a phenomenon known as C-V stretch-out [9].

Figure 4 shows the result of simulating devices MC-1 and MC-2 with the abovementioned model. A very good fit is obtained for MC-1 with  $Q_{\text{ox}} = 8.15 \cdot 10^{11} \text{ cm}^{-2}$  and  $D_{\text{it}} = 1.2 \cdot 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ . Same for MC-2 with  $Q_{\text{ox}} = 8.9 \cdot 10^{11} \text{ cm}^{-2}$  and  $D_{\text{it}} = 1.3 \cdot 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ .

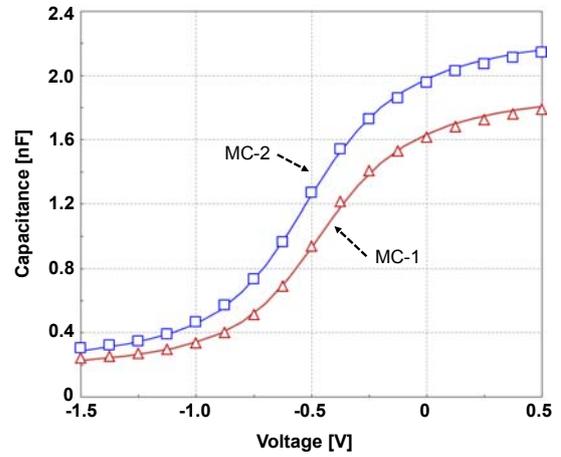


Figure 4: Measured (ticks) and fitted (solid lines) C-V curves for the capacitors MC-1 and MC-2.

Stress experiments applying constant positive and negative voltages to the devices have been performed. The results indicate that a constant voltage produces a horizontal-rigid C-V shift (i.e. only  $Q_{\text{ox}}$  variation) and that the charging dynamics of the devices are faster than those used in [24].

The stress experiments also allowed selection of the voltages used in waveforms BIT0 and BIT1 (see Fig. 1).  $V^+$  was chosen to set the devices into deep accumulation, so that positive charge is trapped in the oxide and therefore the C-V shifts to the left;  $V^-$  was chosen to produce weak inversion, which injects negative charge into the oxide and produces right C-V shift; finally,  $V_1$  was chosen in the depletion state to have enough sensitivity for C-V shift detection.

The values chosen, reported in Table 1, are the same in all the experiments reported in this work.

Table 1  
Parameter values used in BIT0 and BIT1 waveforms.

Device	$V^+$	$V^-$	$V_1$	$T_S$	$\delta$
MC-1	5V	-1V	-0.5V	0.35s	1/3
MC-2	6V	-1V	-0.5V	0.35s	1/3

#### 4. Results and discussion

An initial set of experiments was performed in order to evaluate the effectiveness of the sigma-delta control proposed in [24] with devices MC-1 and MC-2. As stated above, these devices exhibit fast charging dynamics than those used in [24].

In a first experiment, first order control was applied to device MC-1 to achieve a sequence of six target capacitances,  $C_{th} = \{0.98, 1.01, 0.99, 1.02, 0.975 \text{ and } 1.03 \text{ nF}\}$ . Each target-step lasted for 2 hours. The results of this experiment are shown in Fig. 5. It is seen there that the behaviour of the device capacitance  $C[V_1](t)$  agrees with the discussions of previous section. For example, at  $t=4\text{h}$  more BIT0s ( $V^-$  dominant) are applied by the control. This causes shifting of the C-V to the right and thus decreases  $C[V_1](t)$  until the target,  $C_{th}=0.99 \text{ nF}$ , is reached. From then to  $t=6\text{h}$ , the bit stream keeps the capacitance successfully at this target value. However, plateau-associated phenomena are also observed in three different time intervals. When the control becomes “trapped” in a plateau, it provides constant bit stream output, then the observed variable,  $C[V_1](t)$ , is in fact left uncontrolled and exhibits open-loop behaviour. The time length of such control-locking effect is unpredictable, therefore plateaus must be avoided when possible.

On the other hand, a fast C-V measurement was made at the end of each control step, revealing only rigid-horizontal shifts. As expected, the C-V fittings provide a constant value for  $D_{it}$  ( $\approx 1.2 \cdot 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ ) and different values of  $Q_{ox}$ , from  $8.15 \text{ cm}^{-2} \times 10^{11}$  (at  $t=0$ ) to  $8.55 \text{ cm}^{-2} \times 10^{11}$  (at  $t=12\text{h}$ ).

Figure 6 shows the results of an experiment similar to that of Fig. 5. In this case, first order control was again applied to device MC-1, now with four targets,  $C_{th} = \{0.95, 0.935, 0.96 \text{ and } 0.925 \text{ nF}\}$ , in 3h steps. A unique plateau is detected, but it implies that control was lost for approximately 145 minutes. Let us note that the zero value of the bit stream is the control point with the largest plateau [23, 25].

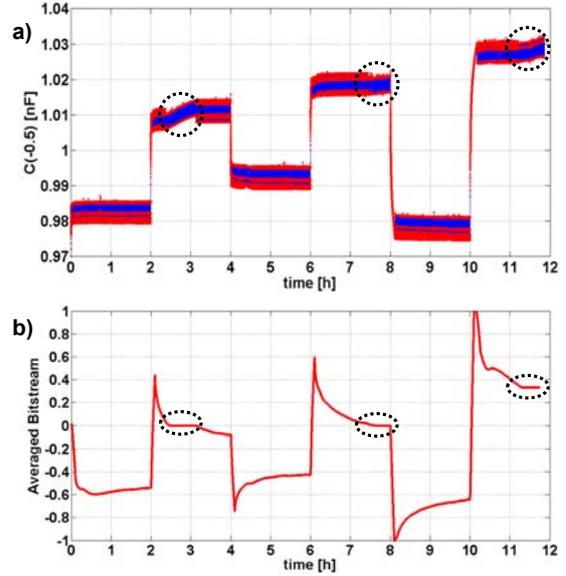


Figure 5: First order control applied to MC-1 to obtain a sequence of six target capacitances. a) Device capacitance measured during the experiment. b) Averaged bit stream provided by the control loop. Circles denote time intervals in which the control is in a plateau.

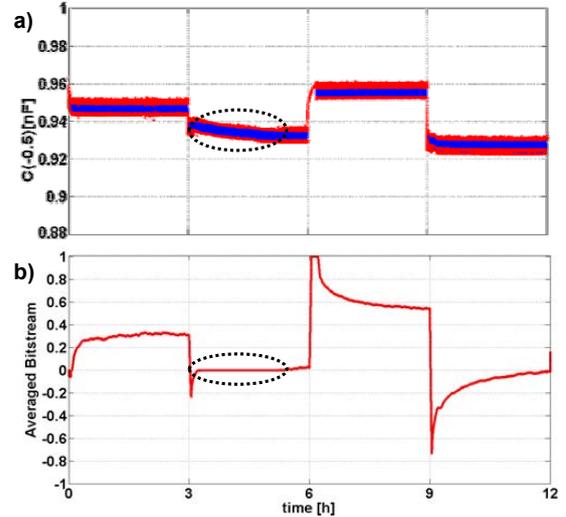


Figure 6: Results of first order control applied to MC-1 to obtain a sequence of four target capacitances. a) Device capacitance measured during the experiment. b) Averaged bit stream provided by the loop. The circle denotes an interval in which the control is in a plateau.

The aim of the next set of experiments was to investigate the eventual improvements provided by the second order control when it is applied to devices that

exhibit fast charging dynamics.

Figure 7 shows the result of an initial experiment, in which the second order control was applied to MC-2 to set a target capacitance  $C_{th}=1.48\text{nF}$ . It is seen that although the capacitance shows fast charging dynamics, no plateau-related episodes are observed during the experiment. It can be also observed that the control crosses the zero value in the control bit stream with no appreciable plateaus.

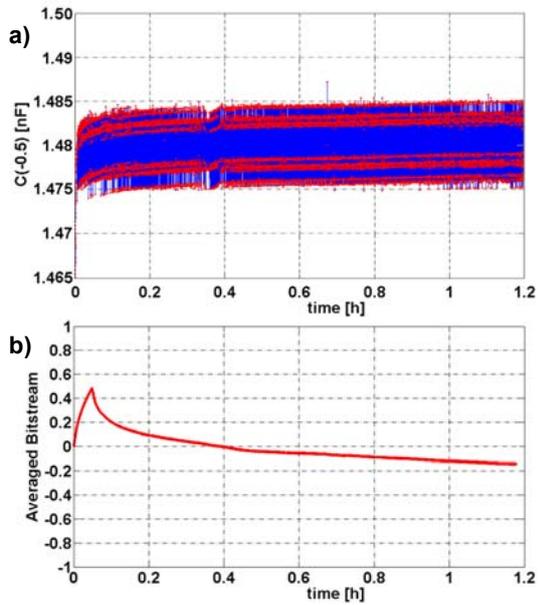


Figure 7: Second order control applied to MC-2 to set  $C_{th}=1.48\text{nF}$ . a) Device capacitance measured during the experiment. b) Averaged bit stream provided by the control loop. No plateaus are observed.

The next experiment replicated that reported in Fig. 6, now using second order control. Therefore the capacitance targets  $C_{th} = \{0.95, 0.935, 0.96 \text{ and } 0.925 \text{ nF}\}$  were set to device MC-1 in 3h steps. Figure 8 shows the results of the experiment. It is observed that the large plateau event of Fig. 6 is no longer seen when second order control is used.

Figure 9 shows two C-Vs, measured at times  $t=3\text{h}$  and  $t=12\text{h}$  of the experiment. Neither stretch-out nor other phenomenon different than horizontal shifting is observed. Furthermore, no significant changes related to interfacial states have been observed for the devices and the voltages applied.

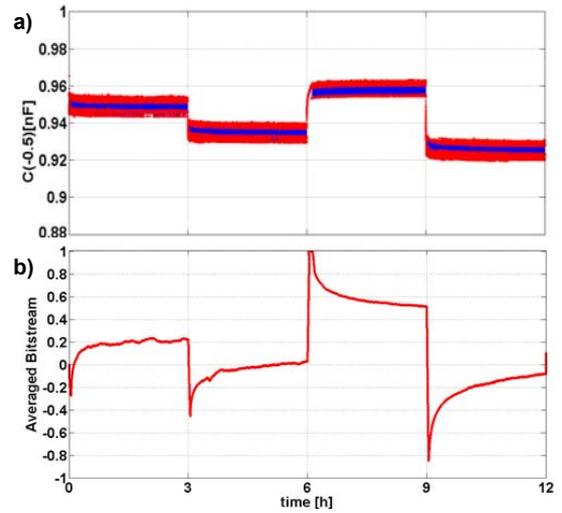


Figure 8: Second order control applied to MC-1 to obtain the same sequence of four target capacitances as in Fig. 6. a) Evolution of the device capacitance. b) Averaged bit stream. No plateaus are observed.

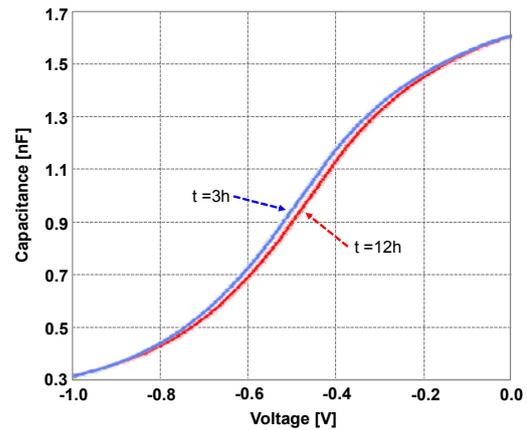


Figure 9: C-V measurements performed at  $t=3\text{h}$  and  $t=12\text{h}$ , from the experiment of Fig. 8.

The zooms of Fig. 10 illustrate how first and second order controls do work. In the first order case, the behaviours of the capacitance and of the bit stream are straightforward related: the next BIT changes each time  $C[V_1]$  exceeds  $C_{th}$ . However, the presence of the integrator makes this relationship not so easy to see in the second order controller, but the behaviour obtained fully agrees with the sigma-delta modulator theory [27] and with the experiments reported in [28].

Finally, Figure 11 compares the spectral power densities of the bit streams obtained from two experiments in which MC-2 was set to  $C_{th} = 1.33 \text{ nF}$  for 16 hours using both first and second order controls.

The presence of the additional integrator in the second order loop produces noticeable differences: the noise at low frequencies becomes reduced and the slope of the quantization noise rolled out of the band of interest increases in the second order control. These results strongly resemble those reported in [29] for thermal sigma-delta modulators, and in [28] for sigma-delta controls of dielectric charge for MEMS.

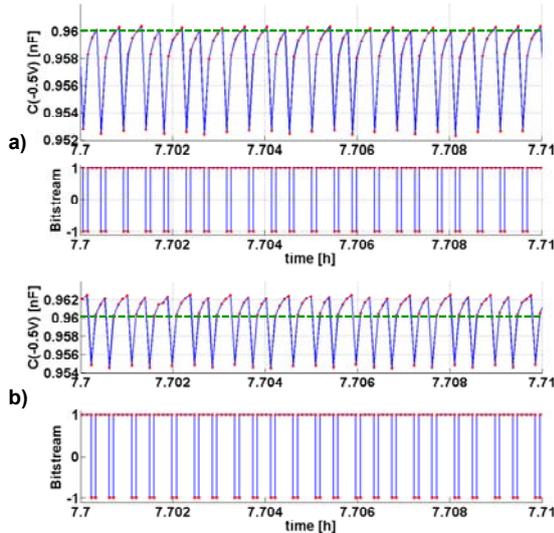


Figure 10: Sampled capacitance and bit stream taken from the experiment of Fig. 6 (a) and from the experiment of Fig. 8 (b), both in the  $C_{th}=0.96\text{nF}$  step.

Although further investigation of the applicability of the proposed control methods to other types of devices and scenarios is to be done, such controls can be seen as a first step towards the design of active controls allowing improving the reliability of MOS devices. Of course, control implementations will strongly depend on the specific application.

## 5. Conclusion

A new second order method of dielectric charging control for MOS capacitors has been presented and checked experimentally. The main advantages found are that the quantization noise shaping is second order and that the typical plateaus of first order sigma-delta controllers can be avoided. This type of controls can be seen as a first step towards the design of active controls that improve device reliability.

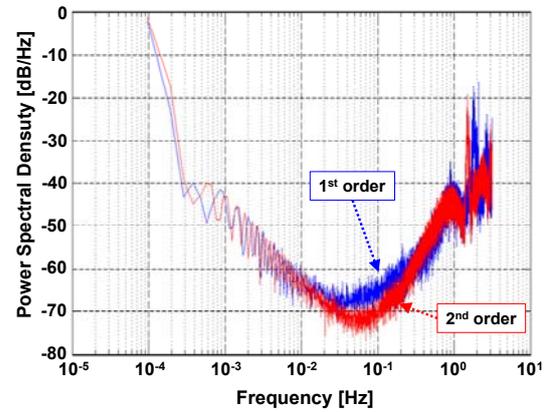


Figure 11: Power spectral density estimation, obtained using Welch's method in MatLab after  $10^5$  samples of the control bit stream. First and second order controls were applied to device MC-2 for 16 hours to obtain the same target capacitance,  $C_{th} = 1.33\text{ nF}$ .

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