mmWave propagation within a computing package

A thesis submitted for the degree of
Telecommunication Systems Engineering

by

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Abstract

Wireless Network-on-Chip (WNoC) appears as a promising alternative to conventional interconnect fabrics as current chip multiprocessors are scaled. There have been plenty of works analyzing the WNoC paradigm from the physical, network and architecture layers. However, the propagation of millimeter waves inside a computing package is still not fully understood. As a result, aspects such as the path loss or the delay spread have not been precisely evaluated yet. This thesis tries to address this issue by accurately modeling a processor chip within a flip-chip package and investigating the wave propagation inside it. Then, through parametric studies, a potentially optimal configuration for 60 GHz WNoC is obtained. Finally, path loss and delay spread are evaluated for a set of representative scenarios, showing that chip-wide attenuation below -34.3 dB and channel capacity above 100 Gbps could be achieved.
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Chapter 1

Introduction

A central processing unit is the electronic component within a computer that carries out the instructions necessary for running computer programs. It performs the basic arithmetic, logical, control and input/output (I/O) operations specified by the instructions.

Around mid-2000s, multi-core processors started to gain importance in the market to finally occupy in the 2010s the majority of the personal computer and servers market. This new kind of processors consist on a single computing component with more than one independent processing units (called "cores"), which are units that read and execute program instructions. This processor can run multiple instructions on separate cores at the same time, increasing overall speed for programs amenable to parallel computing [1].

Networks-on-Chip (NoC) are communication subsystems on integrated circuits [2]. The links of the NoC are shared by many packets coming from the different cores. A high level of parallelism is achieved, because all links in the NoC can operate simultaneously on different data packets. Therefore, as the complexity of integrated systems keeps growing, a NoC provides enhanced performance and scalability in comparison with previous communication architectures, which basically relied on shared buses. NoCs also provide a solution to overcome limitations in large designs from the physical design viewpoint, such as area that the wires occupy and dynamic power that dissipate.

NoCs are being consolidated as the way to interconnect the processing cores and the memory within a chip with multiple cores. However, as in the recent years there has been a significant increase in the number of cores per chip, conventional NoCs may not suffice to fulfill the increasing on-chip communication requirements given that the performance of such networks actually drops as the number of cores grows. Limiting the scalability of NoCs would lead communication between cores to become the next performance bottleneck in multicore processors. This could, in turn, limit the scalability of current multiprocessor architectures and set a performance wall that prevents the development of fast and programmable manycores. Therefore, new on-chip communication technologies are required to either complement or replace existing solutions [3].

Among other alternatives, the concept of Wireless Network-on-Chip (WNoC) has been studied, where on-chip antennas would provide enhanced network performance [4, 5].
Chapter 2

Motivation and Related Work

For the implementation of a wireless network in a NoC, research needs to be done in a wide spectrum of investigation fields in order to study its feasibility and know properly the amount of advantages and the level of enhancements compared with the cost of its deployment.

This research has been done during the last decade and can be segregated mainly into two different blocks. The first block is the set of papers in the field or related to the computer architecture [6], in which the feasibility and enhancements are studied from the point of view of architecture and network [7–9]. These works study and give response to questions such as which number of cores should share an antenna in a cluster, how should the clusters be organized, or which is the power consumption of the transceiver assuming a known path loss profile.

The second block is the set of papers related with EM propagation and more focused from the telecommunications field perspective, in which the feasibility and enhancements are studied from the point of view of EM and materials [10–25]. These works study and give response to questions such as how the materials affect to the path loss, which is the dominant propagation form inside the chip or package, or which is the power consumption due to the path loss profile and the antennas radiation efficiency.

Table 2.1 summarizes the related work on propagation analysis and channel characterization on WNoC. There have been studies on different frequency bands and considering different physical environments, this is, several combinations of layers with different materials. However, there has not been a unified study considering a realistic chip package, including components such as microbumps, ceramic substrate, solder balls, heat spreader or heatsink. Moreover, very few works have explored the impact of these components on the wireless communication metrics (e.g. channel capacity).

In short, this thesis attempts to give answers to the following questions related to the EM propagation within a computing package and the implications on the wireless communications design. In particular:

- How is a package (layers and their widths, dimensions and functionalities)? (Chapter 3)
- Which are the materials of the components and layers of the package? (Chapter 3)
- Which changes we can implement to the package (physical changes) in order to enhance Electromagnetic propagation? (Chapter 4)
<table>
<thead>
<tr>
<th>Citation</th>
<th>Year</th>
<th>Geometry model</th>
<th>Propagation model</th>
<th>Methodology</th>
<th>Upgrades</th>
<th>Enhancements</th>
<th>Antennas used</th>
<th>Frequency Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>[9]</td>
<td>2009</td>
<td>SiO2 and Substrate</td>
<td>Green function</td>
<td>Simulation</td>
<td>Bottom/Top dielectric guiding layer (AIN or Glass)</td>
<td>Enchanced waveguiding (-\rightarrow) monocomponent (surface wave) propagation</td>
<td>Dipole</td>
<td>0-120 GHz</td>
</tr>
<tr>
<td>[10]</td>
<td>2009</td>
<td>SiO2 and Substrate</td>
<td>-</td>
<td>Simulation</td>
<td>-</td>
<td>-</td>
<td>Dipole, loop, yagi</td>
<td>54-66 GHz</td>
</tr>
<tr>
<td>[14]</td>
<td>2017</td>
<td>SiO2 and Substrate</td>
<td>Multi-path</td>
<td>Analysis, simulation</td>
<td>Increase the resistivity of the Si substrate, elevate the height of antenna pairs</td>
<td>Improve path loss</td>
<td>Optical antenna</td>
<td>Optical</td>
</tr>
<tr>
<td>[15]</td>
<td>2013</td>
<td>SiO2 and Substrate</td>
<td>Friis, ray-tracing</td>
<td>Analysis, simulation</td>
<td>Ground plane between silicon substrate and undoped silicon layer</td>
<td>Improved transmission gain and radiation efficiency of silicon on-chip antenna</td>
<td>Dipole</td>
<td>10-100 GHz</td>
</tr>
<tr>
<td>[16]</td>
<td>2015</td>
<td>SiO2, Si and undoped Si bottom layer</td>
<td>Ray-tracing</td>
<td>Analysis, simulation</td>
<td>Bottom layer between substrate and metal chunk (ground)</td>
<td>Wider range and higher sensitivity</td>
<td>Dipole</td>
<td>54-66 GHz</td>
</tr>
<tr>
<td>[17]</td>
<td>2002</td>
<td>SiO2, Si and Glass/AlN bottom layer</td>
<td>Friis</td>
<td>Experimental</td>
<td>Load the chamber with absorbers</td>
<td>Decrease duration PDP -&gt; decrease the RMS delay spread value</td>
<td>Dipole</td>
<td>13-18 GHz</td>
</tr>
<tr>
<td>[18]</td>
<td>2005</td>
<td>SiO2, Si and BT-Resin bottom layer</td>
<td>-</td>
<td>Experimental</td>
<td>-</td>
<td>-</td>
<td>Dipole</td>
<td>13-18 GHz</td>
</tr>
<tr>
<td>[19]</td>
<td>2010</td>
<td>-</td>
<td>Multi-path: PDP and RMS-DS</td>
<td>Analysis, experimental</td>
<td>-</td>
<td>-</td>
<td>Dual-ridge Horn</td>
<td>1-11 GHz</td>
</tr>
<tr>
<td>[20]</td>
<td>2013</td>
<td>Analysis from other works</td>
<td>Path loss, two-ray model, CIR dispersion</td>
<td>Analysis, experimental</td>
<td>-</td>
<td>-</td>
<td>Dipole, monopole</td>
<td>1-750 Thz</td>
</tr>
<tr>
<td>[21]</td>
<td>2017</td>
<td>Conventional printed antenna</td>
<td>Friis, Simulation</td>
<td>Quarter wave monopoles</td>
<td>Improvements in channel losses and bandwidths</td>
<td>Planar dipole, monopole</td>
<td>130-170 GHz</td>
<td></td>
</tr>
<tr>
<td>[22]</td>
<td>2013</td>
<td>Non-wireless NoC</td>
<td>Friis, Experimental</td>
<td>Surface waves which propagate along a surface</td>
<td>Smaller wave decay, reduce the average internode distances, broadcast</td>
<td>-</td>
<td>22.5-35 GHz</td>
<td></td>
</tr>
<tr>
<td>[23]</td>
<td>2009</td>
<td>SiO2, Si and interposer, wire bond package</td>
<td>-</td>
<td>Simulation, experimental</td>
<td>Thinning Silicon thickness and optimizing interposer width</td>
<td>Transmission 5 parameters increased from -93 to -31 dB, tan-oh of the interposer not considered on simulations.</td>
<td>Dipole, horizontal</td>
<td>20 GHz</td>
</tr>
<tr>
<td>[24]</td>
<td>2014</td>
<td>Black box, Input power and output power at antenna ports</td>
<td>-</td>
<td>Simulation, experimental</td>
<td>QOQ modulation</td>
<td>Data rate of 16 Gbps at 60 GHz</td>
<td>-</td>
<td>30, 60 and 90 GHz</td>
</tr>
</tbody>
</table>

Table 2.1: Taxonomy of related work on propagation analysis and channel characterization on WNoC
• How can we theoretically model the electromagnetic propagation inside a chip? (Chapter 5)

• Which is the path loss between a group of 16 antennas depending on the distance? (Chapter 6)

• Which are the most adequate antennas for our case and why, which is the delay spread? (Chapter 6)

• Which is the maximum bitrate (capacity) that we can achieve? (Chapter 6)
Chapter 3

Model definition

3.1 Environment description

Conventional chip structure

Chips are composed of billions of CMOS transistors, whose structure can be represented by the Figure 3.1. Its functionality is based in the fact that the Source and the Drain terminals are either Open Circuit or short circuit depending on the voltage in the Gate terminal, following the two state transistors operation. The simplest model can be seen as a concatenation of millions of transistors placed one next to each other, forming in terms of materials, a Silicon Dioxide (SiO$_2$) layer in the upper level, and a Silicon Substrate layer in the lower one (see Figure 3.1). There may also be a metallic layer below the substrate, which could act as ground plane depending on the configuration. This model is generally used in the papers cited on the table whose model is SiO$_2$ and Substrate.

Particularities of our scenario

In WNoC, the transmitter/receiver antennas are expected to be very small in order to not add too much area overhead in the NoC. As our chip size is expected to be 22 mm per side, the length of the antennas will be in the order of mm or smaller. As the length of the antenna is inversely proportional to the operating central frequency, this frequency will be in the order of tenths or hundreds of Gigahertz, or even Terahertz. The high central frequency allows us to have a theoretically large absolute bandwidth, but it has new problems as strong path attenuation due to the high frequency of operation. The strong path attenuation disadvantage may be compensated by the fact that the path distance between

Figure 3.1: (a) Structure of a CMOS transistor and (b) resulting layered model.
transmitter and receiver will be very short, so the effect of the path attenuation may not be too critical as we will see. Another advantage of our scenario is that the antennas are static, which leads to not having presence of Doppler effect.

**Propagation channel**

As Silicon is a very lossy material, we could speculate that most of the signal would propagate through the Silicon Dioxide layer as the paths through the substrate will be highly attenuated. Nevertheless, the Silicon Dioxide layer is very thin compared to the wavelength, so this leads to a high attenuation of the direct path. To see which is the dominant path, we will have to take into account the potentially strong multipath caused by the path reflections on the border between SiO$_2$ and Substrate layers, and the diffracted signals which are then reflected at the ground metal chuck. In future sections, we will consider the possibility of adding metallic walls to the model around all the sides of the package which will keep the Electric field confined in a region which will increase significantly the multipath effect.

### 3.2 Small scale model construction

#### 3.2.1 Research of model layers and materials and their implication

We will use a flip-chip package with solder bumps and extra dielectric layers to enhance transmission as the initial chip geometry model for the characterization of the channel. The layers will be described from the top of the chip, to the bottom, following the schematic on Figure 3.2.

At the top, there is the heatsink, which is the only metallic structure above the Silicon layer, and it will have importance for our propagation model. Below the heatsink, there is the heat spreader, which initially will not be of our interest, and below them we have the first layer of the die: the Silicon layer, which is the layer where all the active components of the transistors are placed. Below the Silicon layer, we have the layer where all the active components of the transistors are interconnected. The connections are made using different horizontal metallic layers which are interconnected between them using vertical layers, and are also connected to the active components of the transistors. Between the metal layers, there is Silicon Dioxide. The bottom metal layers, which are further away from the Silicon, are much thicker than the upper ones. At the bottom, we have the flip-chip bumps, which are placed at the bottom edge of the die and are approximately cylindrical structures that connect the chip with the package. They are uniformly distributed across all the chips.
bottom area and they have a separation that oscillates between 10 m and 100 m. The lower layers of the package will be described below this section, without entering into too much detail.

Assumptions

We will model the heatsink as a uniform metal structure. In our case will be the layer that reflects the signals that traverse the Silicon layer. We will assume the Silicon layer is uniform, but given that it is a highly doped material, we will have to take into account the high losses of this material. Because the bottom metal layers are much thicker than the upper ones, we can approximate all this layer by two layers, one of Silicon Dioxide at the top (next to the Silicon layer) and one of Metal at the bottom. Working around 60GHz frequencies will lead to wavelengths in the order of mm (5 mm in vacuum). The separation between bumps is much smaller than the wavelength, so this will allow us to approximate the bumps layer as a uniform metallic structure.

Placement of the antenna

The placement of the antenna has been discussed. The first idea is to place the antenna between the interconnections metal layer and the bumps, but this would mean that all the propagation must go through a very thin dielectric layer between two metal layers and this is a very bad environment to radiate electromagnetic waves. Additionally, we would have capacitance effects, as a dielectric between two metal layers is a capacitor. Nevertheless, this case will be studied in further sections at several higher frequencies. As the first option was discarded, the only place which the antenna seems feasible to be placed is at the Silicon Dioxide layer, between the substrate and the interconnections metal layer. As the Silicon Dioxide layer is very thin, we expect that a great contribution of received power will come from the rays that diffract on the Silicon substrate and reflect on the heatsink, making it the dominant path.

3.2.2 Formal definition of all the layers

Figure 3.3 shows the schematic used in CST as a model for the simulations in small scale. Figure 3.4 shows the description of the layers in the small-scale model with their material and function.

Table 3.1 shows the dimensions of each layer of the small-scale model.
3.2.3 Field result templates with non-enclosed package cases

Figure 3.5 shows the field magnitude over the plane $Y=0$. In this figure we can also see that the field magnitude at the bumps region is null.

The representation in Figure 3.6 shows the field intensity along a straight line parallel to the $Z$ axis that traverse all the layers of the package and the die. As we can see, with the non-enclosed package case, the majority of the field intensity is kept at the Silicon and Silicon Dioxide layers, the field magnitude at the bumps region is null and outside the package, the field intensity is lower but it is still too high.

As the kind of package we are modelling is usually surrounded by metallic structures around all the sides (see Figure 3.7), the idea of adding metallic walls around all the package was considered. Also, the ceramic substrate has some copper layers at the top of it that
Table 3.1: Dimensions of each layer of the small-scale model.

<table>
<thead>
<tr>
<th>Name</th>
<th>Height</th>
<th>Radius (mm)</th>
<th>Side (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heatsink</td>
<td>0.5</td>
<td>-</td>
<td>6.6</td>
</tr>
<tr>
<td>Si substrate</td>
<td>0.489</td>
<td>-</td>
<td>2.2</td>
</tr>
<tr>
<td>SiO2 layer</td>
<td>0.011</td>
<td>-</td>
<td>2.2</td>
</tr>
<tr>
<td>Cu upper layer</td>
<td>0.002</td>
<td>-</td>
<td>2.2</td>
</tr>
<tr>
<td>Bumps layer &amp; epoxy coating</td>
<td>0.0875</td>
<td>0.025</td>
<td>2.2</td>
</tr>
<tr>
<td>Cu lower layer</td>
<td>0.008</td>
<td>-</td>
<td>2.2</td>
</tr>
<tr>
<td>Ceramic substrate</td>
<td>0.5</td>
<td>-</td>
<td>6.6</td>
</tr>
<tr>
<td>Solder Balls</td>
<td>0.32</td>
<td>0.225</td>
<td>6.6</td>
</tr>
<tr>
<td>PCB layer</td>
<td>0.5</td>
<td>-</td>
<td>6.6</td>
</tr>
</tbody>
</table>

Figure 3.6: Field intensity along a straight line parallel to the Z axis

Figure 3.7: Schematic of a flip-chip package

were included at the model and simplified by a single copper layer. The addition of this feature was expected to enhance the field magnitude inside the die as in this way the field would be kept inside the region between the heatsink and the ceramic substrate, and no power would be dissipated outside the die. The addition of this feature would also give a more accurate match between the reality and the model.
Figure 3.8: New small-scale model used at CST

Figure 3.9: Field magnitude over the plane $Y=11$ mm for the non-enclosed and the enclosed (with package walls) cases.

Figure 3.8 shows the new small-scale model used at CST.

3.2.4 Field result templates with enclosed package cases

Figure 3.9 show the field magnitude over the plane $Y=11$ mm for the non-enclosed and the enclosed (with package walls) cases.

Thin aluminum walls (10 $\mu$m) on 4 sides were added, so the propagation area is totally confined in the colored region.
In the previous sections the necessity of creating a small-scale model was exposed due to the computational problems that produce working with a model which is both big and complex (big amount of very small bumps). After demonstrating that all the field in the small-scale model will be confined in the region between the ceramic substrate and the heatsink, we can eliminate from our model all the elements which are situated outside this region as they will not have any impact in the results. In addition, as the propagation inside the bumps region is null, we can establish that the bumps region at the frequency of operation acts as a metallic conductor, so we can simplify all the small and complex structures of the bumps by a solid copper layer with the same dimensions as the whole bumps region.

### 3.3 Real scale model definition

As we will see, the electric field was confined inside a particular region and the model could be simplified: The heatsink was no longer a complex structure and was substituted by a simple and thick enough layer. Below the heatsink, the shape of the Silicon and Silicon Dioxide layers remained constant but with the new bigger dimensions. The bumps layer was substituted by a simple and uniform copper layer, and all the rest of the components below the bottom copper layer were removed. The schematic used in CST is displayed at Figure 3.10.

The dimensions of each layer with the real scale is shown in Table 3.2.

<table>
<thead>
<tr>
<th>Name</th>
<th>Height</th>
<th>Radius (mm)</th>
<th>Side (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Heatsink</td>
<td>0,5</td>
<td>-</td>
<td>33</td>
</tr>
<tr>
<td>Si substrate</td>
<td>0,489</td>
<td>-</td>
<td>22</td>
</tr>
<tr>
<td>SiO2 layer</td>
<td>0,011</td>
<td>-</td>
<td>22</td>
</tr>
<tr>
<td>Cu upper layer</td>
<td>0,002</td>
<td>-</td>
<td>22</td>
</tr>
<tr>
<td>Bumps layer &amp; epoxi coating</td>
<td>0,0875</td>
<td>0,025</td>
<td>22</td>
</tr>
<tr>
<td>Cu lower layer</td>
<td>0,008</td>
<td>-</td>
<td>22</td>
</tr>
<tr>
<td>Ceramic substrate</td>
<td>0,5</td>
<td>-</td>
<td>33</td>
</tr>
<tr>
<td>Solder Balls</td>
<td>0,32</td>
<td>0,225</td>
<td>33</td>
</tr>
<tr>
<td>PCB layer</td>
<td>0,5</td>
<td>-</td>
<td>33</td>
</tr>
</tbody>
</table>

Figure 3.10: Schematic used in CST for the real scale model

Table 3.2: Dimensions of each layer with the real scale
The total height of the die is 0.598 mm. The total height of the package is 2.418 mm. The side of the die is 22 mm, whereas the side of the package is 66 mm. The total volume of the die is 289.2 mm³. The total volume of the package is 10.53 cm³.

**Area overhead**

All the widths of the layers described above are based on the dimensions of the state-of-art chips. The only layers that will have different widths respect to an ordinary package without WNoC are the Silicon layer and the added AIN layer. In our final model, the Silicon layer which was assumed to have a width of 489 µm before the enhancements, will be substituted by a Silicon layer with a width of 100 µm and an additional AIN layer with a width of 850 µm. These additions will be explained in further sections. The extra height of the die and the package will be 461 µm. Therefore, the extra volume of the die will be 223.12 mm² (77.15% more) and the extra volume of the package will be 2.01 cm² (19.1% more).

**3.4 Simulation methodology**

The program used for the simulations in this thesis is CST Microwave Studio, a specialist tool for the 3D EM simulation of high frequency components that is seen by an increasing number of engineers from this field as an industry standard development tool.

CST Microwave Studio is a full wave simulator that uses the equations of Maxwell to evaluate the field distribution over a set of 3D geometric forms in a virtual space and to extract the S-Parameters between several ports that can be attached to an antenna.

In addition to these basic features, CST Microwave Studio has a lot of built-in tools for performing analysis, operations, representations and extraction of parameters from the results that were obtained from the solution of Maxwell's equations.

The S-Parameters were obtained for all the simulations performed, but were specially interesting in the simulations of a group of 16 antennas in which one of them was used as the excitation and the other ones as receivers. In these cases, the S-Parameters were crucial to determine the path loss, the optimization of the layers thicknesses in terms of power loss or to study the trade-off between using different kinds of antennas. To determine the channel response, the gain was obtained with CST using a specific tool to calculate gains from a radiation antenna. This tool was also useful to determine the radiation efficiency of an antenna. The electric field could also be represented, when CST was configured properly, over a line, a plane or even a volume, being able to modify the cross-sections to see the field distribution inside the geometric form. The electric field over a plane or line, the gain and S-Parameters were able to be exported in ascii format to be used later by other data analysis software as Matlab, used in a lot of occasions. The electric field representation and export was very useful to compare the analytical modelling with the simulation results.

The time-domain solver feature, together with all the tools that come with it, was very useful to determine multipath effect parameters as the delay spread, which is crucial to determine the coherence bandwidth, and with it, the capacity of the channel.
Chapter 4

Performance evaluation

4.1 Field result templates of the path loss profile

For the path loss profile study, an array of 16 ports that will be connected each one to an antenna was created and their elements were uniformly distributed over the Silicon Dioxide layer forming a rectangular mesh. For the interest of our study, the S-parameters of each pair of antennas were evaluated using port 1 as the excitation port, and leaving the other ones as passive receiver ports. Port 1 was selected as excitation because it is placed in a corner of the die and the results using this port as the excitation will be the worst-case ones, as the most separated pair of ports are the ones at the corners. After obtaining the S-Parameters, using Matlab we calculated for each antenna the worst S-Parameter from 55 to 65 GHz, which in most of the cases resulted in a line that was composed by several S-Parameters that were the worst case for a particular region of the spectrum instead of a single S-Parameter which is the worst case in all the span. This is because different nodes have notches at particular frequencies resulting from the destructive interference between waves coming from different paths. We consider three different antennas, and their pros and cons will be studied in the next section analyzing the mean and the response flatness of the worst S-Parameters.

4.1.1 Comparison of the performance between antennas

Square aperture antenna

At Figure 4.1(a), we can observe the field magnitude over the plane of the Silicon Dioxide layer. At Figure 4.1(b), we can see the S Parameters from the S2-1 to the S15-1 with the excitation at port 1. The mean of the minimum of the S-Parameters was -116.62 dB and its variance was 23.47.

Monopole antenna

At Figure 4.2(a), we can observe the field magnitude over the plane of the Silicon Dioxide layer. At Figure 4.2(b), we can see the S Parameters from the S2-1 to the S15-1 with the excitation at port 1. The mean of the minimum of the S-Parameters was -88.73 dB and its variance was 36.37.
Figure 4.1: (a) Field magnitude over the plane of the Silicon Dioxide layer and (b) S Parameters from the S2-1 to the S15-1 with the excitation at port 1.

Figure 4.2: (a) Field magnitude over the plane of the Silicon Dioxide layer and (b) S Parameters from the S2-1 to the S15-1 with the excitation at port 1.

Figure 4.3: (a) Field magnitude over the plane of the Silicon Dioxide layer and (b) S Parameters from the S2-1 to the S15-1 with the excitation at port 1.
Figure 4.4: Minimum of the S-Parameters with the three different kinds of antenna and their mean.

<table>
<thead>
<tr>
<th>Antenna type</th>
<th>Pros</th>
<th>Cons</th>
</tr>
</thead>
<tbody>
<tr>
<td>Square aperture antenna</td>
<td>-</td>
<td>High variance</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Lowest mean</td>
</tr>
<tr>
<td>Monopole</td>
<td>Highest mean</td>
<td>Highest variance</td>
</tr>
<tr>
<td>Patch antenna</td>
<td>Lowest variance</td>
<td>Lower mean than monopole</td>
</tr>
</tbody>
</table>

Table 4.1: Pros and cons of the three antennas studied.

**Patch antenna**

At Figure 4.3(a), we can observe the field magnitude over the plane of the Silicon Dioxide layer. At Figure 4.3(b), we can see the S Parameters from the S2-1 to the S15-1 with the excitation at port 1. The mean of the minimum of the S-Parameters was -102.77 dB and its variance was 13.36.

**Patch antenna**

Figure 4.4 shows the minimum of the S-Parameters with the three different kinds of antenna and their mean.

The Monopole antenna has the highest mean but has the highest variance. This is due to the non-optimal adaptation of the antenna. The mean of the Monopole, even that is higher than with the other kinds of the antenna, it is still very low (-88.73 dB) due to antenna inefficiency surrounding a big piece of Silicon, and needs to be raised to have acceptable path loss results. These trade-offs are summarized in Table 4.1. The techniques to increase the mean of the minimum of the S-Parameters with excitation at port 1 are purposed, explained, tested and optimized in the next section.

4.2 Enhancements of the path loss profile

4.2.1 Additional dielectric layer. Motivation of AIN.

The Silicon is a very lossy material in terms of electrical conductivity ($\tan\delta=0.25175$ at 60 GHz) and we saw with the previous simulations that the Silicon Dioxide layer is too thin to propagate electromagnetic waves through it. That causes that the direct ray travels along a surface wave between the Silicon Dioxide and the Silicon layer, as the attenuation coefficient for the direct ray corresponds to the $\tan\delta$ of the Silicon Bulk. In this scenario,
a good solution to enhance the propagation between the antennas inside the chip is to add an additional layer to our model made of a material with low electrical conductivity. In order to do not add extra area overhead and extra cost to the production of the chip, a good choice when choosing the extra layer is to use one of the layers that our chip has for a certain function, and take advantage of the conductivity properties of its material or replace it by another material which also does this function and has more advantageous conductivity properties. In our case, as its scenario is a flip-chip package, we will take advantage of the heat spreader layer which is between the Silicon bulk and the heatsink. This layer must be made of a material with very high thermal conductivity at the same time that it has to have a low thermal expansion coefficient. The thermal conductivity is the property of a material to conduct heat and the thermal expansion is the property of a material to change in shape, area and volume in response to a change of temperature.

In Figure 4.5 we can see a plot of the thermal conductivity vs the thermal expansion for a list of materials typically used for this application. As we need materials with high thermal Conductivity and low thermal expansion, the most interesting materials for this application are the Silicon Carbide, the Beryllium Oxide and the Aluminium Nitride. The best heat spreader of the three materials selected is the Silicon Carbide (SiO), which has a thermal conductivity over 350 W/mK, but it is not interesting for our application due to its high electrical conductivity (tanδ=0.003). The Beryllium Oxide(BeO), also known as Beryllia, has a high thermal conductivity of 330 W/mK, and a much lower electrical conductivity (tanδ=0.00039811 at 60 GHz). Although the Beryllium Oxide would be a very good option for our scenario, the Aluminium Nitride, which has a lower thermal conductivity of 285W/mK, is more interesting because it has a slightly lower electrical conductivity (tanδ=0.00029938 at 60 GHz) and in our application we have enough heat spreader properties with the AIN whereas the electrical conductivity of this layer is very important for reducing the path loss between antennas. The thickness of the AIN layer will have to be adjusted in order to find the thickness value that maximizes the minimum of the S-Parameters.
4.2.2 Reduction of the Silicon thickness. Motivation.

In [25], a minimum received power of -30 dBm is set as a reasonable received power to operate without problems. Therefore, we need to reduce the path loss to be able to achieve these levels of received power without having to transmit a lot of power. To this end, one can reduce the Silicon thickness. This way, we are reducing the path loss, as the length of the path that the rays pass through the Silicon layer, which is a very lossy material, is shorter. Doing that we are also improving the radiation efficiency of the antennas, as the fact of being surrounded by a lossy material affects the radiation efficiency of them. Nowadays, there are several new wafer thinning techniques for reducing the Silicon layer thickness which include mechanical grinding, chemical mechanical polishing (CMP), wet etching and atmospheric downstream plasma (ADP) dry chemical etching (DCE). Co-design of the antenna and propagation layers. The design of the ideal Silicon and AIN layers thicknesses was done performing parametric simulations with all the combinations for several Silicon and AIN layers thicknesses.

4.2.3 Co-design of the antenna and propagation layers.

The design of the ideal Silicon and AIN layers thicknesses was done performing parametric simulations with all the combinations for several Silicon and AIN layers thicknesses.

As the computation time with antennas other than the aperture raises due to the complexity added by the small edges of the antenna structure as monopoles or patches, the first simulation was performed using the aperture antennas. Simulating in the case of the aperture antenna, we could have an approximation of which is the region of interest we want to evaluate with the real antennas, which are more complex and would take too computation time for a broad evaluation. The Silicon thickness parameter was evaluated from 0.15 mm to 0.25 mm with a resolution of 0.05 mm. The AIN layer thickness parameter was evaluated from 0 to 0.85 with a resolution of 0.05 mm. The results are shown in Figure 4.6, in which we can see a tendency of improvement of the minimum of the S-Parameters as we reduce the Silicon thickness and we increase the AIN layer. Nevertheless, the optimal value is given with a Silicon thickness of 0.15 mm and an AIN thickness of 0.8 mm. The next
step was to perform a parametric simulation with the monopole antennas, which are the antennas that have given better results in terms of low power loss, adaptation and radiation efficiency. According to the previous results, the parametric simulation was performed at the region of interest, in which the mean of the minimum of the S-Parameters is higher.

The Silicon thickness parameter was evaluated again from 0.15 mm to 0.25 mm with a resolution of 0.05 mm. The AIN layer thickness parameter was evaluated only from 0.7 mm to 0.9 mm with a resolution of 0.05 mm. As in this case we only have 15 cases, the three axis representation it is not appropriate to reflect well which are the best cases.

Adaptation of the antennas.

This shift of the optimal frequency for adaptation was due to the different material on the layers that the monopole traverse: Silicon Dioxide, Silicon and AIN. Assuming that the monopole is resonant for the length $\lambda_0/(4 \sqrt{\varepsilon_{r,\text{eff}}}$, the effective dielectric permittivity was extracted, and the length of the monopole was computed for 60 GHz. $\lambda_0$ is the wavelength of the signal in the vacuum, and $\varepsilon_{r,\text{eff}}$ is the effective dielectric permittivity of the medium. As changing the length of the monopole could change all the S-Parameters enough to alter the optimal thicknesses of both Silicon and AIN layers, the parametric simulation to determine the optimal thickness for each of the two layers should be repeated. At the same time, when we find the new ideal pair of thicknesses, the frequency for the minimum S1-1 parameter could be shifted again, so in that case the antenna would no longer be adapted, meaning that we should modify again the length of the monopole. This process will be repeated until we approach enough to the solution. In figure 29, we can observe the S1-1 parameter using the monopole and the optimal Si and AIN thickness before adaptation and after all the adaptation process.

The parametric simulation to optimize the thicknesses was performed again for the new monopole length. In this simulation, the Silicon thickness was evaluated from 0.15 to 0.225 in steps of 0.025 mm, and the AIN thickness was evaluated from 0.7 to 0.9 mm in steps of 0.05 mm. The selection of the widths for the optimization was based on the previous results. In Figure 4.7, we can see that in this case we do not have a trade-off because the case in which the Silicon layer has a thickness of 0.15 mm and the AIN layer has a thickness of 0.85 is the best of all both in terms of mean and variance.

In Figure 4.8, the S-Parameters for the case 13 (Si=0.15, AIN=0.85) are shown. After the results, a final parametric simulation was needed to be performed with more precision.
which means higher resolution around the previous optimal result. The optimal thickness resulted to be 0.10 mm for the Silicon layer and 0.84 mm, for the AIN layer, as this case had the highest mean and the lowest variance. On this section, after having chosen the most efficient antenna and having adjusted its sizes looking for adaptation at the same time the thicknesses of the Silicon bulk layer and the Aluminum Nitride layer were also adjusted, we have achieved a reduction of a total loss from 76.67 dB in the best case of the aperture antenna to a total loss of only -34.3 dB, with the optimal thicknesses for the two layers using the adapted monopole.

4.2.3.1 Trade-off etching.

The fact that the antennas inside a chip are surrounded by Silicon, a very lossy material, makes the antenna less efficient in terms of power radiation. A possibility for enhancing the radiation of the antenna is to surround it by another material less lossy than the silicon by perforating the Silicon with a bigger diameter than the antenna, placing the antenna inside the hole and filling the space between the Silicon and the antenna with the new material. In our case, as we are using an AIN layer between the Silicon and the heatsink as a heat spreader and to enhance the propagation, the material selected to fill the etch will be the Aluminum Nitride.

In Figure 4.9, the structure of an etch inside a chip is shown. In this case, the diameter of the etch that has been used is 10 times the diameter of the monopole antenna. For the optimal case with the Silicon thickness of 0.1 mm and the AIN thickness of 0.84 mm found in the previous section, the possibility of using the etching technique in our model has been studied. For doing this, several simulations have been performed and the results have been processed with matlab. The minimum of the S-Parameters for each case and their mean has been calculated and plotted in the same figure. The results are shown in Figure 4.10.

The minimum of the S-Parameters has been plotted for three cases: without etching and with etches of diameter two times and 10 times bigger than the diameter of the monopole. As we can see, the difference between the cases it is almost 1.3 dB, which is very low for the complexity we add to the production process. Furthermore, this very low difference must
be due to the fact that now we have less amount of Silicon therefore we have less amount of material with high conductivity and that means we have less losses, but the radiation efficiency of the antennas has not increased.
Chapter 5

Analytical modeling

5.1 Construction of the path loss model

For the construction of an analytical model, the Ray tracing approximation was used, which consists on assuming the field in each point of the space comes from the sum of infinitely narrow rays that can arrive to that point by a direct ray, a reflected ray in a change of medium, a diffraction or scattering. The power does not come equally from all the contributions, which means that some of them will be the most important and the rest can be neglected for a simplification of the model although it is still a good approximation. All the simulations for the path loss model were performed with a single antenna placed in the middle of the die. The contributions which can be neglected depend on the environment in which we are working.

- Direct ray: This will be the most important component of our model because they will provide the majority of the power received.

- Reflected rays: As the antenna is placed in the Silicon Dioxide layer and the points are evaluated on this same layer, the reflections at the four walls which are the boundaries between the die and the vacuum between the die and the metallic box of the package, will be taken into account. Also, the rays reflected at the bottom of heatsink should be taken into account. For simplicity of the model, the reflected rays with two or more walls of the die, will not be taken into account, as their contribution is not as important as the single reflections.

- Diffracted rays: All the diffracted rays that come out from the die are very unlikely to enter again to the die as they have to be perpendicular enough to be able to transmit between the Silicon Dioxide and the vacuum, reflect in the package box, and transmit again between the vacuum and the Silicon Dioxide. Moreover, the few rays that are inside this boundary, will be highly attenuated by two diffractions and one reflection.

- Scattering: The scattering effect comes from rough surfaces such as the ocean surface and building facades. In our case, except for the bumps and the solder balls, all the model of our package has even surfaces with tetrahedral forms, and the bumps and the solder balls are not included in the volume in which the propagation takes place, so the scattering effect will not be considered for our theoretical model. As the important contributions that we will consider have been set, we can start defining the electric field in some point in the Silicon Dioxide layer of the die:
\[ E_{\text{SiO}_2} = E_{\text{direct}} + \sum_{\text{walls,heatsink}} E_{\text{reflected}} \quad (5.1.1) \]

As we are evaluating the electric field magnitude, Friis equation is not a good option for modeling the attenuation of each ray with the distance, because we do not have two antennas communicating, we only have a large number of rays radiated by an antenna placed in the center. For modeling the change of amplitude depending on the distance of each ray, we will model the amplitude in a distance \( d \) using the following equation:

\[
\frac{A_0}{A_d} = e^{\gamma d} \quad (5.1.2)
\]

Where \( \gamma \) is the propagation constant, and can be expressed as:

\[
\gamma = \alpha + j\beta \quad (5.1.3)
\]

Where \( \alpha \) is the attenuation constant, and \( \beta \) is the phase constant. The electric field magnitude at a given distance \( d \), can be decomposed into real and imaginary parts as:

\[
E_{\text{mag},d} = e^{-\alpha d} e^{-j\beta d} \quad (5.1.4)
\]

The attenuation constant can be expressed as:

\[
\alpha = \frac{\pi \sqrt{\varepsilon_r}}{\lambda} \tan(\delta) \quad (5.1.5)
\]

Where \( \tan(\delta) \) is the tangent of the delta of the electric conductivity, and in the case of \( \text{SiO}_2 \) is 0.0975 at 60 GHz and in the case of the Silicon is 0.25175 at 60 GHz. The electric field magnitude of the direct ray can hence be expressed as:

\[
E_{\text{direct}} = \exp\left\{ \frac{\pi \sqrt{\varepsilon_r,\text{SiO}_2}}{\lambda} \tan(\delta)_{\text{Si}} d_{\text{direct}} \right\} \exp\left\{ -\frac{2\pi}{\lambda_0} \sqrt{\varepsilon_r,\text{SiO}_2} d_{\text{direct}} \right\} \quad (5.1.6)
\]

Note that the \( \tan(\delta) \) is the one of the Silicon instead of the Silicon Dioxide one. This was changed because after observing the simulation results, the results matched with the model only with the Silicon \( \tan(\delta) \). This is due to the thinness of the Silicon Dioxide layer, which makes the propagation through the Silicon Dioxide practically like the Silicon one. The electric field magnitude of the reflected rays at the edges of the die can hence be expressed as:

\[
E_{\text{ref,wall},i} = R_i \exp\left\{ \frac{\pi \sqrt{\varepsilon_r,\text{SiO}_2}}{\lambda} \tan(\delta)_{\text{Si}} d_{\text{ref,wall},i} \right\} \exp\left\{ -\frac{2\pi}{\lambda_0} \sqrt{\varepsilon_r,\text{SiO}_2} d_{\text{ref,wall},i} \right\} \quad (5.1.7)
\]

Where \( R_i \) is the reflection coefficient at the wall \( i \), which can be W, E, S or N. The electric field magnitude of the reflected rays at the edges of the die can be expressed as:

\[
E_{\text{ref,heatsink}} = T_{\text{SiO}_2,\text{Si}} R_{Al} T_{\text{Si},\text{SiO}_2} \exp\left\{ \frac{\pi \sqrt{\varepsilon_r,\text{Si}}}{\lambda} \tan(\delta)_{\text{Si}} d_{\text{ref,heatsink}} \right\} \exp\left\{ -\frac{2\pi}{\lambda_0} \sqrt{\varepsilon_r,\text{Si}} d_{\text{ref,heatsink}} \right\} \quad (5.1.8)
\]

Where \( T_{\text{SiO}_2,\text{Si}} \) is the transmission coefficient for each incidence angle between the Silicon Dioxide and the Silicon layer, \( R_{Al} \) is the reflection coefficient of the aluminum heatsink,
Figure 5.1: Product of both transmission coefficients between Silicon layer and Silicon Dioxide layer and the reflection coefficient at the heatsink.

![Product of both transmission coefficients between Silicon layer and Silicon Dioxide layer and the reflection coefficient at the heatsink](image)

Figure 5.2: Total Electric field without radiation diagram of the antenna.

![Total Electric field without radiation diagram of the antenna](image)

and $T_{Si,SiO2}$ is the transmission coefficient for each incidence angle between the Silicon and the Silicon Dioxide layer. For the transmission and reflection coefficients, the following equation has been used:

$$T_{MediumA,B} = \frac{2\cos\theta_i}{\sqrt{\varepsilon_{r,B}}} + \frac{\cos\theta_t}{\sqrt{\varepsilon_{r,A}}}$$

$$R_{Al} = \frac{1}{\sqrt{\varepsilon_{r,Al}}} - \frac{1}{\sqrt{\varepsilon_{r,Sl}}}$$

Where $\theta_i$ is the incidence angle and $\theta_t$ is the transmitted angle. These transmission and reflection coefficients take into account that the transmission coefficient beyond the critical angle is zero and the reflection coefficient is 1, which means that for certain angles, the power is kept in the same medium.
Figure 5.3: Error between results and ray-tracing approximation

Figure 5.4: Comparison between the theoretical model and the simulation results in a 3-D view

**Matching with path loss results.**

In Figure 5.3, the error was computed using the following formula:

\[
\text{Error} = \text{abs}(E - \hat{E})
\]  

Where \( \hat{E} \) is the approximation of \( E \), the results obtained from the simulations. As we can see in the figure, the error is higher only in the edges of the die, and in the region near the antenna, where the propagation is ruled by near field laws, whereas in the majority of the die the model matches very well.

In Figure 5.4, we can observe the comparison between the theoretical model and the simulation results in a 3-D view, where the azimuth represents the field intensity and \( y \) and \( x \) axis represent the points of the plane.

In Figures 5.4 and 5.5, we can see the comparison between the Ray Tracing theoretical model and the simulation results. The plot is very similar both qualitatively and in terms of absolute numbers, except of the edges, where the effect of interference between non main rays is higher.
Figure 5.5: Comparison between the theoretical model and the simulation results in a 2-D view

Figure 5.6: E-field simulation results evaluated along the line X=0 mm and Z=0.095 mm

5.1.1 Near field region

In Figure 5.6, we can see the E field simulation results evaluated along the line X=0 mm and Z=0.095 mm. As we can see in the figure, there is a region which can be approximated by a line in dB scale. The slopes of the two lines (one for each side) are -5.28 dB/mm and -5.10 dB/mm. In the region near the antenna, the approximation does not fit as we are in the near field region:

$$\frac{\lambda_0}{\sqrt{\varepsilon_r}} \approx 1.3 \text{mm}$$  \hspace{1cm} (5.1.12)

In the region between -1.3 and 1.3 mm, near field laws dominate the propagation and will be studied above. Also, in the edges of the die, the distortion due to reflections in the side of the die are stronger and creates peaks and valleys of field intensity due to constructive and destructive interference.

In the region between -1.3 and 1.3, which corresponds to the near field region, the fitting curve used is the following, according to [26]:

$$P_{RX} \sim |E|^2 \sim \frac{1}{(kd)^2} + \frac{1}{(kd)^4} + \frac{1}{(kd)^6}$$  \hspace{1cm} (5.1.13)

This formula means that the power in the near field region is inversely proportional to the distance elevated at 2, 4 and 6. In figure 3, each of the fitting curves are superposed over the results and are only visible in their valid region. Also, the region inside the antenna limits was not considered [-0.15 ; 0.15].
In Figure 5.7, the equations explained above for the near region have been applied for the region inside the limits $[-1.3 -0.15] \cup [0.15 1.3]$ mm, which corresponds to the near field region outside the antenna limits.
Chapter 6

Wireless channel characteritzation

6.1 Channel frequency response

In this section, the channel response was computed for a span of 10 GHz, taking 60 GHz as the central frequency, and using the port 1 as the source excitation. The antennas used and the modifications of the model such as Silicon and AIN layer thicknesses were the optimal ones according to the conclusions taken at the previous sections. With these assumptions, the resulting frequency response is a set of 16 frequency responses, one for each pair of antennas, using the antenna corresponding to port 1 as the excitation one, and ports 2 to 16 as the receiver ones. The modulus of the frequency response for a pair of antennas can be obtained from the S-parameters and the gain of both transmitter and receiver antennas. Their relationship is shown in the following equation:

\[ G_t G_r |H(f)|^2 = \frac{|S_{21}|}{(1 - |S_{11}|^2) \cdot (1 - |S_{22}|^2)} \]  

(6.1.1)

Where S21 is the power that receives port 2 from the power radiated at port 1, S11 and S22 is the power that returns to port 1 and port 2 respectively with the excitations at port 1 and 2, respectively. Gt and Gr are both transmitter and receiver antennas gain and H(F) is the channel frequency response. As all the 16 antennas used in the package are identical monopoles, both transmitter and receiver gains are identical, and were computed performing a separate simulation with a single transmitter monopole at the center of the package, and removing the package walls to be able to capture the gain with the corresponding CST tool. The gain of the antenna was averaged along the \( \phi \) axis for \( \theta = 90^\circ \). This was done because the gain that will see an eventual receiver monopole from a transmitter one that is located next to it will receive the corresponding power according to the radiation pattern of the antenna in the horizontal direction (\( \theta = 90^\circ \)), and the average was done for simplification reasons because the monopole can be considered an omnidirectional antenna in the direction orthogonal to azimuth. The results of the gain are shown in Figure 6.1.

Finally, the modulus of the channel responses with excitation at port 1 were computed using the S-Parameter results, the gain results and equation 1. The results are shown in Figure 6.2.
6.2 Path loss

Path loss exponent from channel response.

In wireless communications, path loss can be represented by the path loss exponent, whose value is around 2 for free space propagation, but can be up to 4 for relatively lossy environments, and is below 2 in the environments which act as a waveguide. Path loss is usually expressed in dB, and can be represented by the following formula:

\[ L_{dB} = 10n \cdot \log_{10}(d) + C \quad (6.2.1) \]

For calculating the path loss exponent from the channel response, several simulations with different excitations were performed in order to have a better representation of the channel response at the whole package, not only when the excitation was at Port 1. As the package has two axis of symmetry, performing simulations at the 16 ports was not required. Simulations with excitations at ports 1, 2, 5 and 6 were performed to calculate the channel response for each pair of antennas for each excitation. The rest of the channel responses for the excitations at the rest of the ports were deduced from these 4. The mean of the channel response for each pair of the antennas was computed for each of the excitations and was
In Figure 6.4, the mean of the channel response for each pair of the antennas was scattered with different shapes and colors for each port of excitation.

In Figure 6.5, a linear regression fitting in a log scale for the distance was performed and plotted over the samples, producing a line with a slope of 8.14 dB/mm.

In this case, the path loss could be expressed as:

$$L_{dB} = 10 \cdot 0.814 \cdot \log_{10}(d) + 8.55$$  \hspace{1cm} (6.2.2)

As in the previous figure there were 2 outliers that were clearly separated from the rest of them, they were not considered useful for the calculation of a realistic path loss exponent,
so they were removed for the calculation of the linear fitting. The results of the two lines are shown at Figure 6.6.

The slope of the fitting line was this time 9.32 dB/mm. Thus, the path loss in this case can be expressed by the formula:

\[ L_{dB} = 10 \cdot 0.932 \cdot \log_{10}(d) + 7.6 \]  \hspace{1cm} (6.2.3)

This means that our path loss exponent is 0.9, which corresponds to an environment where the waveguide effect is the dominant in the propagation model.

### 6.3 Multipath analysis

Our model of the package is very rich in metal structures, such as the heatsink and the package edges, which are made of aluminum, or the bumps, which are made out of copper
and tin. These metal structures produce a big level of reflections due to the high reflectivity of their materials, and the signal will mainly attenuate only in the dielectric materials.

The fact that we have a confined region where all the propagation takes place, which is between the package walls, the heatsink and the copper layer of the ceramic substrate, makes all the signals radiated inside this region attenuate slower, thereby increasing the multipath. This effect is similar to the one that is produced in a reverberation chamber, which are confined chambers with a minimum absorption of electromagnetic energy. A special group of objects that introduce multipath is the bumps, which are conical small metallic structures which spread the rays that inflict to them in a lot of different directions.

In Figure 6.7, the plot represents the E-field distribution at the plane Z=0.095, which corresponds to the one where the antennas are placed. The antennas used are patch antennas and their time-domain response has been captured for a delta excitation at the time t=0.26 ns.

As we can see in the figure above, the direct rays (black lines) are not the only important contribution to the signal, and even for some points of the die, they are not the first components to arrive. The red lines represent the diffracted rays that come from outside the die and manage to reflect along the space between the package walls (edges of the package) and the edges of the die.

**Power delay profile and delay spread**

In telecommunications, a good measure of the multipath richness of a channel is the delay spread. It can be interpreted as the difference between the time of arrival of the earliest significant multipath component and the time of arrival of the latest multipath component. The most common metric of the delay spread is the root mean square delay spread (rms), and can be expressed by the following equation:

\[
\tau_{RMS} = \sqrt{\frac{\int_{0}^{\infty} (\tau - \bar{\tau})^2 PDP(\tau)d\tau}{\int_{0}^{\infty} PDP(\tau)d\tau}}
\]

(6.3.1)
Where PDP is the Power Delay Profile of the channel, and \( \tau \) is the mean delay of the channel, which can be computed as:

\[
\tau = \frac{\int_0^\infty \tau PDP(\tau) d\tau}{\int_0^\infty PDP(\tau) d\tau}
\] (6.3.2)

In our case we studied the delay spread of the channels between each pair of antennas when the excitation is at port 1, to have the worst scenario (highest delay spread). For computing each delay spread, a time domain simulation was performed with the case of the aperture antenna, another with the patch antennas and another one with the monopoles. The power delay profile of the port 2 is shown at Figure 6.8 for the case of the aperture antennas, patch and monopoles.

The delay spreads were plotted over distance and over the package top view and colored depending on the magnitude of this parameter.

**Aperture:** The highest delay spread in the aperture antenna, shown at Figure 6.9 occurs at the edges of the die, due to the richness of multipath in the receiver antenna at these areas.

**Patch:** The highest delay spread in the patch antenna, shown at Figure 6.10, occurs near to the excitation antenna, due to the importance of the ringing signals that stay at the big structure of the patch antenna, coming out in regular intervals after the main ray.

**Monopole:** The highest delay spread in the monopole antenna, shown at Figure 6.11, occurs far from the excitation antenna, but not in the edges, because a high delay spread happens when the direct ray and the multipath components have similar magnitude and one of them does not dominate among the others. In the edges of the die, the multipath components coming from outside the die dominate over the direct rays which are highly attenuated by the silicon and other lossy materials.

The maximum delay spread, in our study, is the important data because it gives us the minimum coherence bandwidth. The maximum delay spreads are:

- Aperture: 0.1127 ns
- Patch: 1.332 ns
- Monopole: 0.1227 ns

Seeing the results, we can conclude that the Patch antenna is not a good option in terms of trying to minimize multipath, as its structure keeps the rays inside before they come out for a long time after the main ray. The results with the aperture antenna are slightly better than with the monopole because it does not have a big metal structure which could keep signals inside before they come out after the main ray, but as the results in terms of channel frequency response are much better, we consider that the monopole antenna is the most appropriate for our model.

An alternative to the delay spread as a tool to study the difference of time between the arrival of the firsts and the last contributions of power to the receiver antenna is presenting in a normalized graph the cumulative sum of the power received at each port in function of the time, which is the same as the cumulative sum of the S-Parameters in function of the time.

The lines that correspond to a pair of ports with a high delay spread will have a steeper slope in the representation. This is shown in Figure 6.12.
Coherence Bandwidth

With the maximum Delay Spread computed for each case, we can easily calculate the maximum Coherence Bandwidth, which is a statistical measurement of the range of frequencies over which the channel can be considered flat, or in other words, the maximum bandwidth in which two frequencies have correlated amplitude fading. The coherence bandwidth, $B_c$, is given approximately by the expression:

$$B_c = \frac{1}{\tau_{RMS}} \quad (6.3.3)$$

The minimum coherence bandwidths are:

- Aperture: 8.873 GHz
- Patch: 0.751 GHz
Channel Capacity

The maximum rate at which information can be transmitted over a communications channel of a specified bandwidth in the presence of noise can be obtained by the Shannon-Hartley theorem. This maximum rate is known as capacity, and can be obtained by:

\[ C = B \cdot \log_2(1 + \frac{S}{N}) \]  

(6.3.4)

The capacity is the theoretical upper bound of the data rate that can be communicated at an arbitrary low error rate using an average signal power S and an additive white gaussian noise of power N. As the frequency of operation is 60 GHz, neither the shot noise or the interferences introduced by the clock will not be significant, so the noise will be basically composed of thermal noise. The thermal noise can be computed as:
\[ N = B \cdot k \cdot T \]  \hspace{1cm} (6.3.5)

Where \( T \) is the temperature in Kelvin, \( B \) is the bandwidth of the noise, which equals to the bandwidth of the signal, and \( k \) is the Boltzmann constant. With the monopoles case, the coherence bandwidth obtained was 8.150 GHz. The temperature of the processor varies depending on the model, but we will use the maximum average temperature that the typical producers provide. Its the case of the AMD Athlon or the AMD Sempron, which can reach the temperature of 95°C (368.15°K). Hence, the Noise power is:

\[ 8.150GHz \cdot 1,3807 \cdot 10^{23} J/K \cdot 368.15K = 4.1425 \cdot 10^{-11}[W] \]  \hspace{1cm} (6.3.6)

In [25], the power consumption of the transmitter and receiver transceivers was studied by simulations and checked by experimental results, and for their study they assumed a
transmitter power in the ports of the antenna of -0.5 dBm, and they expected a received
signal in the ports of the receiver antenna of -30 dBm, to ensure a low BER. The power that
we assume it is provided by the transmitter transceiver is around 0.8913 mW (-0.5 dBm).
After the enhancements, the mean minimum of the S-Parameters was -34.3 dB. Hence, the
Signal power is:

\[
S = 10^{-\frac{30+0.5}{10}} \cdot 10^{-\frac{34.3}{10}} \text{ [W]} \quad (6.3.7)
\]

Hence, the Capacity is:

\[
8.150GHz \log_2(1 + \frac{10^{-\frac{30+0.5}{10}} \cdot 10^{-\frac{34.3}{10}}}{4.1425 \cdot 10^{-11}}) = 105.66Gb/s \quad (6.3.8)
\]

The received power in the ports of the receiver antenna for the worst case is -34.8 dBm,
just 4.8 dB lower than the one assumed at the paper mentioned above. We assume this low
difference of power will be tolerable and compatible with the model used in the paper.

**Reducing Multipath Effects**

As the SNR is almost 40 dB, the possibility of reducing the multipath in order to increase
the coherence bandwidth has been studied for the case of the monopoles. The two solutions
include a reduction of the SNR. In the first case, the aluminum walls at the sides of the
packages were removed. The results of Delay spread are shown in the following figure:

The maximum of the Delay Spread is at both S8-1 and S14-1, and has a nominal value
of 0.09421 ns. This means that the coherence bandwidth is in this case 10.61 GHz. The
mean of the minimum S-parameter is -38 dB. Hence, the Capacity is:

\[
10.61GHz \log_2(1 + \frac{10^{-\frac{30+0.5}{10}} \cdot 10^{-\frac{38}{10}}}{5.3929 \cdot 10^{-11}}) = 120.48Gb/s \quad (6.3.9)
\]

In the second case, the aluminum walls at the sides of the packages were changed of
material to rubber, which is a very absorbent material. The results of Delay spread are
shown in the following figure:
The maximum of the Delay Spread is this time at S11-1, and has a nominal value of 0.09225 ns. This means that the coherence bandwidth is in this case 10.84 GHz. The mean of the minimum S-parameter is -39.1 dB. Hence, the Capacity is:

\[
10.84GHz \cdot \log_2(1 + \frac{10^{-(-30+0.5)}}{5.5098 \cdot 10^{-11}}) = 118.80 \text{Gb/s} \tag{6.3.10}
\]

In the cases of using a patch antenna and an aperture antenna without enhancements the corresponding capacities would be, respectively, 7.33 Gbps and 0.604 Gbps
Chapter 7

Conclusions

It is necessary for the research in the art of WNoC to study more thoroughly the characterization of the wireless channel inside a package, particularly in our case of a flip-chip package.

With advanced EM simulation programs as the one used in this work, called CST microwave studio, we could create both simple and complex models of the package with parallelepipeds forming several layers of uniform materials. As the field is confined inside the lateral walls of the package, we could simplify all the elements of the model that are outside a certain region of interest.

After performing simulations with the model created, we could observe that the monopole antenna is the one of the three antennas studied (aperture, patch and monopole) that gives better results in terms of mean of the minimum of the S-Parameters. We demonstrated that the Aluminum Nitride material could be used as the heat spreader of the package taking advantage of its qualities as a thermal conductor and as an electrical insulator. The enhancements in terms of attenuation obtained modifying the thicknesses of both AIN and Silicon layers and choosing the proper and adapted antenna could increase the mean of the minimum of the S-Parameters from -76.67 dB to -34.3 dB. The possibility of using etching in the region of Silicon next to the antennas was discarded after observing that the impact of adding this feature in the S-Parameters was very small.

Performing simulations and monitoring the field across the package at frequencies from 60 GHz to 1 THz it was found that the EM propagation inside the bumps region was impossible at 60 GHz but feasible at higher frequencies like 1 THz.

Parallel to the work performing simulations with CST, a channel theoretical model has been built to have a theoretical modeling of the electrical field distribution over the package, to be able to extent the results to other situations with this tool. It also gives credibility to the results of the simulation and facilitates the understanding of them. The near field region has been modeled with equations about near field propagation from [26]. Both theoretical models fit very well with the simulation results.

After performing the last simulations, it has been revealed that the path loss exponent is 0.932, very small compared with 2, that corresponds at free space. The effect of multipath has been demonstrated that it is very important and in terms of delay spread, the aperture antenna is the one that gives better results but very close to the monopole antenna.

Finally, the channel capacity of the model described above is 105.66 Gbps with a mean of the minimum of the S-Parameters of -34.3 dB. It was observed that removing the lateral metallic package walls from the model, the delay spread was reduced so the capacity
increased to 120.48 Gbps, even that the mean of the minimum of the S-Parameters was reduced to -38 dB.
Bibliography


