Computer Architecture Department
Progress and Results 1996

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This is the second time the Department of Computer Architecture publishes this annuary. It describes the main activities of this Department along the last five years.

The purpose of this book is to explain what is the Department, with special emphasis on research activities in which the people of this Department is engaged.

This booklet begins with an overall description of the Department, the University in which it is set and the organization which serves to establish links between the Department and the industrial world. It continues with a brief biography of the people in the Department. After that, the research lines followed by the different groups of the Department are presented, together with the most relevant publications. Later on the graduate program supported by the Department is described, followed by a brief presentation of the undergraduate courses presently offered by this Department to the University. Finally, a description of the Research Centers hosted by the Department. A list of the available technical reports of the Department closes this annuary.

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Chapter 1

Introduction

Some general information about the Computer Architecture Department (DAC) is provided in this chapter, together with its framework, the Polytechnic University of Catalonia (UPC).

1.1 The Polytechnic University of Catalonia

The Polythecnic University of Catalonia (UPC) is a public institution at the service of the society whose objective is to offer a general education in technical, artistic and humanistic subjects. UPC aims to offer a high standard in teaching, responding to changes in the professions and adopting a multidirectional approach. It also maintains a high level of excellence in research and a high quality of life on the Campus.

The UPC was created in 1971 to teach and do research on science and engineering. It is located in Catalonia. The UPC has, at present, 38 Departments, 9 Schools and Faculties, 7 Technical Colleges, 6 Associate Schools and 6 Research Institutes.

The centers maintain curricula for undergraduate studies, the Schools and Faculties leading to 10 semester degree and the remaining leading to 6 semester diploma. The courses are focussed on eight areas: Architecture, Sciences, Civil Engineering, Industrial Engineering, Computer Sciences, Telecommunications, Nautical Studies and Photography. In these areas the UPC offers 13 degrees and 30 diplomas.

The UPC offers 52 graduate programs on seven areas: Architecture, Mathematics and Physics, Civil Engineering, Industrial Engineering, Electronics and Telecommunications, Computer Sciences and Business. The graduate programs are conducted by the Departments, and they are closely related to their respective research lines.

The centers of the UPC are spread all over Barcelona area. In the academic year 95–96, the UPC had 36985 non–graduate students, 1246 graduate students, 2173 teaching staff and 1055 administrative / service staff.

The address of the UPC is:

Universitat Politècnica de Catalunya[1]
Av. Dr. Gregorio Marañón, 42
08028 Barcelona (Spain)
Phone: (+34 3) 401 62 00
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1.2 The Computer Architecture Department

The Computer Architecture Department (DAC), is in charge of the teaching of courses on computer structure and organization, computer architecture, operating systems, computer networks, computer evaluation and VLSI design. The DAC is involved in the curricula of four centers in the UPC, details can be seen in the chapter "Undergraduate Programs".

The DAC maintain, at present, four separate research lines. Details can be found in the chapter "Research". In relation to these four research lines, the DAC offers one Graduate Program.

The legislative body of the DAC is the Council ("Consell"), where all the members of the DAC are represented, accordingly to an elective system; this body delegates the everyday tasks in a smaller steering committee, the "Junta", whose members are also elected. Some specific tasks are associated to a number of "adhoc" committees of the DAC. Two relevant examples are the "Comissió Docent", which deals with the evaluation of the academic quality of the DAC members, and the "Comissió d'Investigació", created to guarantee the coordination and quality of the research lines in the DAC.

The Department officers, at this moment, are the following people:

- **Chair**: Prof. Juan J. Navarro
- **Vice Chair of Organization**: Dr. Agustín Fernández
- **Vice Chairs of Undergraduate Affairs**:
  - Dr. Jaime Delgado (Coordinator and FIB)

[1] http://www.upc.es/

  - Dr. Juan C. Cruellas (ETSETB)
  - Prof. Manel Medina (EUPBL)
  - Mr. Sergio Sánchez (EUPVG)
  - Dr. Montse Peiron (Academic Laboratories)

- **Vice Chair of Graduate Affairs**: Dr. Jordi Cortadella
- **Administrative Officer**: Ms. Carme Peñas
- **System Manager**: Ms. Rosa Castro

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[2] http://www.ac.upc.es/

Chapter 2

The People

In this chapter we present the list of members of the Department during the academic year 1996–97.

This list of members is divided in several groups. The first three ones, Academic Staff, includes all the professors which have obtained tenure, either as Professors (Catedràtics d'Universitat), as Associate Professors (Professors Titulars d'Universitat), or Assistant Professors (Professors Titulars d'Escola Universitaria). In Spain, the tenure is obtained through a personal examination. The next one is for the Full Time Adjuncts (Professors Associats a Temps Complet), which are either professors which are working towards their doctoral dissertation, and at the same time having a teaching responsibility in the department. The next, is the last one including in the Academic Staff. It includes the Full Time Adjuncts (Professors Associats a Temps Parcial), or professors which work somewhere else, usually in the industry, and teach some specific subject, usually related to their experience with the industry world. The Research Fellows includes the supported people which are working toward their Doctorate degree, but do not have any teaching responsibilities within the department. The administrative staff are the people depending exclusively from the department, which do most of the paperwork job. For each person, the year written at the right, refers to the time s/he started to work at the department. Some people have their own WWW home page, addresses always are "http://www.ac.upc.es/homes/EMAIL".

2.1 Professors

- **Casals Torres, Olga**, 1983. (olga@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1983). Phd in Telecommunication Engineering, UPC, (1986).

- **Labarta Mancho, Jesús**, 1981. (jesus@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1981). Phd in Telecommunication Engineering, UPC, (1983).

- **Llabería Griñó, José M.**, 1981. (llaberia@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1980). MS degree in Computer Science, UPC, (1981). Phd in Computer Science, UPC, (1983).

- **Medina Llinàs, Manel**, 1974. (medina@ac.upc.es)
  MS degree in Telecommunication Engineering, Universidad Politécnica de Madrid, (1974). Phd in Telecommunication Engineering, UPC, (1981).

- **Navarro Guerrero, Juan J.**, 1982. (juanjo@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1982). Phd in Telecommunication Engineering, UPC, (1986).

- **Valero Cortés, Mateo**, 1974. (mateo@ac.upc.es)
  MS degree in Telecommunication Engineering, Universidad Politécnica de Madrid, (1974). Phd in Telecommunication Engineering, UPC, (1980).

2.2 Associate professors

- **Ayguadé Parra, Eduard**, 1986. (eduard@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1986). Phd in Computer Science, UPC, (1989).

- **Cortadella Fortuny, Jordi**, 1985. (jordic@ac.upc.es)
  MS degree in Computer Science, UPC, (1985). Phd in Computer Science, UPC, (1987).

- **Cruellas Ibarz, Juan Carlos**, 1985. (cruellas@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1983). Phd in Telecommunication Engineering, UPC, (1989).

- **Delgado Mercé, Jaime**, 1983. (jaime@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1983). Phd in Telecommunication Engineering, UPC, (1987).

- **Domingo Pascual, Jordi**, 1982. (jordid@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1982). Phd in Telecommunication Engineering, UPC, (1987).

- **Fernández Jiménez, Agustín**, 1988. (agustin@ac.upc.es)
  MS degree in Computer Science, UPC, (1988). Phd in Computer Science, UPC, (1992).

- **González Colas, Antonio**, 1986. (antonio@ac.upc.es)
  MS degree in Computer Science, UPC, (1986). Phd in Computer Science, UPC, (1989).

- **Herrada Lillo, Enrique**, 1974. (herrada@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1974). Phd in Telecommunication Engineering, UPC, (1983).

- **Navarro Mas, José I.**, 1985. (nacho@ac.upc.es)
  MS degree in Computer Science, UPC, (1985). Phd in Computer Science, UPC, (1991).

- **Navarro Moldes, Leandro**, 1988. (leandro@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1988). Phd in Telecommunication Engineering, UPC, (1992).

- **Olivé Duran, Angel**, 1983. (angel@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1983). Phd in Computer Science, UPC, (1991).

- **Solé Pareta, Josep**, 1984. (pareta@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1984). Phd in Computer Science, UPC, (1991).

- **Valero García, Miguel**, 1986. (miguel@ac.upc.es)
  MS degree in Computer Science, UPC, (1986). Phd in Computer Science, UPC, (1989).

2.3 Assistants

- **Badia Sala, Rosa M.**, 1989. (rosab@ac.upc.es)
  MS degree in Computer Science, UPC, (1989). Phd in Computer Science, UPC, (1994).

- **Barrado Muxí, Cristina**, 1989. (cristina@ac.upc.es)
  MS degree in Computer Science, UPC, (1989).

- **Bofill Soliguer, Pau**, 1986. (pau@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1983).

- **Cela Espín, José M.**, 1990. (cela@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1989). Phd in Telecommunication Engineering, UPC, (1996).

- **Doreste Blanco, Luis**, 1987. (luis@ac.upc.es)
  MS degree in Computer Science, UPC, (1986).

- **Gallego Fernández, Isabel**, 1979. (isabel@ac.upc.es)
  MS degree in Industrial Engineering, UPC, (1979).

- **Gil Gómez, Marisa**, 1988. (marisa@ac.upc.es)
  MS degree in Computer Science, UPC, (1988). Phd in Computer Science, UPC, (1994).

- **Jordán Fernández, Francisco**, 1988. (jordan@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1988). Phd in Telecommunication Engineering, UPC, (1995).

- **Larriba Pey, Josep Ll.**, 1989. (larri@ac.upc.es)
  MS degree in Computer Science, UPC, (1988). Phd in Computer Science, UPC, (1995).

- **Masip Bruin, Xavier**, 1989. (xmasip@ac.upc.es)
  BS degree in Telecommunication Engineering, UPC, (1989).

- **Royo Vallés, Dolors**, 1989. (dolors@ac.upc.es)
  MS degree in Computer Science, UPC, (1989).

- **Sánchez López, Sergio**, 1989. (sergio@ac.upc.es)
  BS degree in Telecommunication Engineering, UPC, (1989).

- **Torres Viñals, Jordi**, 1988. (torres@ac.upc.es)
  MS degree in Computer Science, UPC, (1988). Phd in Computer Science, UPC, (1993).

- **Tubella Murgadas, Jordi**, 1987. (jordit@ac.upc.es)
  MS degree in Computer Science, UPC, (1986). Phd in Computer Science, UPC, (1996).

2.4 Full Time Adjuncts

- **Acebrón Antón, José J.**, 1992. (acebron@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1992).

- **Artiaga Amouroux, Ernest**, 1994. (ernest@ac.upc.es)
  MS degree in Computer Science, UPC, (1994).

- **Barceló Ordinas, José M.**, 1991. (joseb@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1991).

- **Cerdà Alabern, Llorenç**, 1993. (llorenc@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1993).

- **Corral González, Anna del**, 1990. (anna@ac.upc.es)
  MS degree in Computer Science, UPC, (1990).

- **Cortés Roselló, Toni**, 1992. (toni@ac.upc.es)
  MS degree in Computer Science, UPC, (1992).

- **Díaz de Cerio Ripalda, Luis Manuel**, 1993. (ldiaz@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1993).

- **Elias Vila, Eduard**, 1990. (eduarde@ac.upc.es)
  MS degree in Computer Science, UPC, (1990).

- **Espasa Sans, Roger**, 1992. (roger@ac.upc.es)
  MS degree in Computer Science, UPC, (1992).

- **García Almiñana, Jordi**, 1991. (jordig@ac.upc.es)
  MS degree in Computer Science, UPC, (1991).

- **Girona Turell, Sergi**, 1993. (sergi@ac.upc.es)
  MS degree in Computer Science, UPC, (1993).

- **Herrero Zaragoza, Josep R.**, 1993. (josepr@ac.upc.es)
  MS degree in Computer Science, UPC, (1993).

- **Iñigo Griera, Jordi**, 1990. (jordii@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1990).

- **Jiménez Castells, Marta**, 1992. (marta@ac.upc.es)
  MS degree in Computer Science, UPC, (1992).

- **Juan Hormigo, Antonio**, 1992. (antonioj@ac.upc.es)
  MS degree in Computer Science, UPC, (1992).

- **Llosa Espuny, Josep**, 1990. (josepll@ac.upc.es)
  MS degree in Computer Science, UPC, (1990). Phd in Computer Science, UPC, (1996).

- **López Alvarez, David**, 1991. (david@ac.upc.es)
  MS degree in Computer Science, UPC, (1991).

- **Marín Tordera, Eva**, 1996. (eva@ac.upc.es)
  MS degree in Physics, Universitat de Barcelona, (1993).

- **Martorell Bofill, Xavier**, 1991. (xavim@ac.upc.es)
  MS degree in Computer Science, UPC, (1991).

- **Morancho Llena, Enric**, 1993. (enricm@ac.upc.es)
  MS degree in Computer Science, UPC, (1993).

- **Moreno Bilbao, Susana**, 1993. (susana@ac.upc.es)
  MS degree in Computer Science, UPC, (1993).

- **Parcerisa Bundo, Joan Manuel**, 1993. (jmanel@ac.upc.es)
  MS degree in Computer Science, UPC, (1993).

- **Pastor Llorens, Enric**, 1991. (enric@ac.upc.es)
  MS degree in Computer Science, UPC, (1991). Phd in Computer Science, UPC, (1996).

- **Peig Olivé, Enric**, 1993. (enricp@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1993).

- **Peiron Guàrdia, Montse**, 1990. (montse@ac.upc.es)
  MS degree in Computer Science, UPC, (1990). Phd in Computer Science, UPC, (1996).

- **Perramon Tornil, Xavier**, 1989. (xavierp@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1989).

- **Polo Cantero, José**, 1994. (jpolo@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1994).

- **Roig Mansilla, Oriol**, 1991. (oriol@ac.upc.es)
  MS degree in Computer Science, UPC, (1991).

- **Sánchez Carracedo, Fermín**, 1987. (fermin@ac.upc.es)
  MS degree in Computer Science, UPC, (1987). Phd in Computer Science, UPC, (1996).

- **Vila Martí, Frederic**, 1990. (frederic@ac.upc.es)
  MS degree in Electronic Engineering, Universitat de Barcelona, (1995).

2.5 Part Time Adjuncts

- **Calzón Cañas, Susana**, 1994. (susanac@ac.upc.es)
  MS degree in Computer Science, UPC, (1994).

- **Cosials Ruiz, Carlos**, 1992. (carlos@ac.upc.es)
  MS degree in Computer Science, UPC, (1989).

- **Fernández Barta, Montserrat**, 1992. (montsef@ac.upc.es)
  MS degree in Computer Science, UPC, (1989).

- **Marquès Puig, Joan Manel**, 1992. (marques@ac.upc.es)
  MS degree in Computer Science, UPC, (1991).

- **Martí Escalé, Ramon**, 1992. (ramon@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1990).

- **Pesado Collazos, M. Asunción**, 1995. (asun@ac.upc.es)
  MS degree in Computer Science, UPC, (1991).

- **Pons Jansana, Josep**, 1992. (josepp@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1986).

- **Santos Boada, Germán**, 1986. (german@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1986). Phd in Telecommunication Engineering, UPC, (1993).

- **Solé Clotet, Josep**, 1979.
  MS degree in Computer Science, UPC, (1979).

- **Toribio González, Angel**, 1990. (angelt@ac.upc.es)
  MS degree in Computer Science, UPC, (1988).

2.6 Administrative and Services Staff

- **Buch Tarrats, Jordi**, 1994. (jbuch@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1994). Qualified Technic (esCERT).

- **Cáceres López, Francisco J.**, 1995.
  Head Porter.

- **Calvet Gómez, Mercè**, 1993. (mcalvet@ac.upc.es)
  Assistant Administrative.

- **Castro Cabrera, Rosa M.**, 1991. (rosa@ac.upc.es)
  MS degree in Computer Science, UPC, (1991). System Manager.

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  Assistant Administrative (CEPBA).

- **Escobar Casanova, Joan**, 1990. (joane@ac.upc.es)
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  Assistant Administrative.

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  MS degree in Computer Science, UPC, (1990). System Manager (CEPBA).
- **Luna Mayans, Juani**, 1992. (juani@ac.upc.es)
  Assistant Administrative.
- **Mora Antolino, Víctor**, 1994. (victor@ac.upc.es)
  Assistant System Manager.
- **Peñas Zapata, Carme**, 1996. (carme@ac.upc.es)
  Administrative officer.
- **Pérez Rubio, Robert**, 1994. (robert@ac.upc.es)
  Assistant Administrative.
- **Riu Valentí, Oriol**, 1993. (uri@ac.upc.es)
  MS degree in Computer Science, UPC, (1994). System Manager (CEPBA).
- **Rodríguez Garrido, José A.**, 1995. (josear@ac.upc.es)
  Assistant System Manager.

2.7 Research Fellows

- **Alfonso Sánchez, José Miguel**, 1996. (josem@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1995).
- **Becerra Fontanal, Yolanda**, 1995. (yolandab@ac.upc.es)
  MS degree in Computer Science, UPC, (1994).
- **Cerdán Cartagena, Fernando**, 1996. (fernando@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1994).
- **Cornetta, Gianluca**, 1995. (cornetta@ac.upc.es)
  MS degree in Electronic Engineering, Politecnico di Torino (Italy), (1995).
- **Corbalán González, Julita**, 1996. (juli@ac.upc.es)
  MS degree in Computer Science, UPC, (1996).
- **Fontdecava Baig, Enric**, 1996. (enricf@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1994).
- **González González, José**, 1996. (joseg@ac.upc.es)
  MS degree in Computer Science, UPC, (1995).
- **González Tallada, Marc**. (marc@ac.upc.es)
  MS degree in Computer Science, UPC, (1996).
- **Grande Ayán, M. Luz**, 1994. (luz@ac.upc.es)
  MS degree in Computer Science, UPC, (1994).
- **Gregoris de la Fuente, Luis**, 1995. (luisg@ac.upc.es)
  MS degree in Computer Science, UPC, (1995).
- **Musoll Cinca, Enric**, 1994. (enricmc@ac.upc.es)
  MS degree in Computer Science, UPC, (1993). Phd in Computer Science, UPC, (1996).
- **Ortega García. Maite**, 1994. (maite@ac.upc.es)
  BS degree in Computer Science, UPC, (1994).

- **Peña Basurto, Marco A.**, 1995. (marcoa@ac.upc.es)
  MS degree in Computer Science, UPC, (1993).

- **Pérez Payeras, Andrés**, 1993. (andresp@ac.upc.es)
  MS degree in Telecommunication Engineering, UPC, (1993).

- **Puga Socarras, Carmen**, 1994. (carmen@ac.upc.es)
  MS degree in Electronic Engineering, Instituto Superior Politécnico José A. Echevarría (Cuba), (1985).

- **Reig Galilea, Fermín Javier**, 1992. (ferminj@ac.upc.es)
  MS degree in Computer Science, UPC, (1993).

- **Rodríguez Mula, Gerard**, 1995. (gerard@ac.upc.es)
  MS degree in Computer Science, UPC, (1994).

- **Rubia García, Montserrat**, 1996. (montser@ac.upc.es)
  MS degree in Computer Science, UPC, (1996).

- **Sánchez Navarro, Jesús**, 1996. (fran@ac.upc.es)
  MS degree in Computer Science, UPC, (1995).

- **Sarmiento Meneses, Mildred**, 1991. (mildred@ac.upc.es)
  MS degree in Systems Engineering, Escuela Colombiana de Ingeniería Julio Garavito (Colombia), (1990).

- **Serra Hurtado, Arturo**, 1995. (artur@ac.upc.es)
  Llicenciat en Filosofia i Lletres, (1977). Doctor en Antropologia Cultural, (1992).

- **Serra Monner, Albert**, 1996. (alberts@ac.upc.es)
  MS degree in Computer Science, UPC, (1994).

- **Vila Sallent, Joan**, 1993. (joanv@ac.upc.es)
  MS degree in Computer Science, UPC, (1992).

- **Villa Vargas, Luis A.**, 1994. (luisv@ac.upc.es)
  MS degree in Electronic Engineering, Instituto Politécnico Nacional (México), (1991).

Chapter 3

Research Fields

This chapter describes the main research activities in this Department. The information is organized along the four research lines presently pursued: "High Performance Computing"; "Design and Performance Evaluation of Broadband Integrated Communication Systems"; "Distributed Systems Architecture"; and "VLSI Systems Design". For each research group, we present a brief description of the most important working topics, including the best papers of each topic. The chapter is closing with the papers published in our Department since 1992.

3.1 Introduction

At the UPC, the research activities are organizated through the research lines. They are groups of people with common interest in a technical or scientific area. In this chapter, we present the current four research lines bellowing to the Computer Architecture Department:

- High Performance Computing
- Design and Performance Evaluation of Broadband Integrated Communication Systems
- Distributed Systems Architecture
- VLSI Systems Design

For each line, we present a brief description, the most important topics of each one, and for each topic the most relevant papers are shown. Also, the grants, basic research projects and R+D projects of the last 5 years are presented.

To finish this chapter, we present an exhaustive list of all the papers published from 1992 to 1996 in the Computer Architecture Department.

3.2 High Performance Computing Group

Our research group has been working in Architectures and Programming Tools for Supercomputers during the last years. The topics dealt with by the group are:

- Processor architecture
- Memory Management and Organization
- Instruction–Level Parallelism
- Parallelization, Data Distribution and Loop Transformations
- Algorithms and Architectures for Linear Algebra and Sparse Matrix computations
- Microkernel Technology Support to Parallel Applications
- Operating Systems for Parallel Machines
- Systematic mapping of algorithms to hardware
- Execution of Applications based on the Declarative Programming Paradigm

3.2.1 Research Subfields

Processor architecture

Branch instructions. Branch instructions impose a heavy limit to the exploitation of the instruction-level parallelism in pipelined processors. We have proposed a mechanism for the effective execution of branch instructions. This mechanism consists of executing branch instructions in parallel with the rest of the instructions, therefore branch instructions require no additional time.

- Antonio González. Design and Evaluation of an Instruction Cache for Reducing the Cost of Branches. *Performance Evaluation*, vol. 20, no. 1–3, pp. 83–96, May 1994.
- Antonio González. A Survey of Branch Techniques in Pipelined Processors. *Microprocessing and Microprogramming*, vol. 36, no. 5, pp. 243–257, September 1993.
- Antonio González and José M. Llabería. Reducing Branch Delay to Zero in Pipelined Processors. *IEEE Transactions on Computers*, vol. 42, no. 3, pp. 363–371, March 1993.

- Antonio González and José M. Llabería. Instruction Fetch Unit for Parallel Execution of Branch Instruction. In *Proccedings of the 3rd ACM International Conference on Supercomputing (ICS'89)*, pp. 417–426, Creta (Greece), June 1989.

- Antonio González, José M. Llabería, and Jordi Cortadella. A Mechanism for Reducing the Cost of Branches in RISC Architectures. *Microprocessing and Microprogramming*, vol. 24, no. 1–5, pp. 565–572, August 1988.

- Antonio González, José M. Llabería, and Jordi Cortadella. Zero–Delay Cost Branches in RISC Architectures. In *Proceedings of the IASTED International Symposium on Applied Informatics*, pp. 24–27, Grindelwald (Suiza), February 1988.

Vector Processors. Our research on vector architectures has focused on the memorry pipeline utilization problem. We started by developing a set ot tracing and simulation tools able to accurately extract performance data out of vectorized programs. This data clearly showed that the latency tolerance properties of vector architectures is not as good as expected. Therefore, our research focused on three different techniques aimed at improving vector performance:

- decoupling

- out–of–order execution and register renaming

- multithreading

The first two are targeted at improving single application performance while the third is targeted at a throughput improvement. We have looked at decoupled vector architectures and have shown that they can greatly improve performance and that tolerate main memory latency much better than a traditional vector architecture. We have also looked at out–of–order execution and register renaming for vector machines. Again, the performance advantage was substantial and the technique did also allow for toleration of large memory latencies. Moreover, register renaming allowed us to introduce precise exceptions in a vector machine, which, in turn, allows for the easy implementation of virtual memory. The mutlithreaded technique executes several independent vector programs on a machine having four sets of vector registers and sharing all other functional units. The performance of this type of architecture is also much better than a traditional vector machine and the technique is able to almost saturate the mmemory port.

- Roger Espasa and Mateo Valero. Multithreaded Vector Architectures. In *Proceedings of the Third International Symposium on High Performance Computer Architecture (HPCA'97)*, San Antonio, TX (USA), February 1997.

- Roger Espasa and Mateo Valero. Decoupled Vector Architectures. In *Proceedings of the Second International Symposium on High Performance Computer Architecture (HPCA'96)*, pp. 281–290, San José, CA (USA), February 1996.

Memory Management and Organization

Within this area we can distinguish several points. First, an out-of-order access method to vector elements has been proposed, designed and evaluated for vector uniprocessor systems. This method allows to perform the accesses with the minimum achievable latency for a number of families of strides greater than that achieved by the use of the conventional in-order access method. This mechanism can be used together with any storage scheme, such as interleaving, skewing or linear transformations. Also, a method that allows to achieve conflict-free access for the case of accessing vectors with power-of-two strides has been developed.

- Mateo Valero, Tomás Lang, José M. Llabería, Montse Peiron, Juan J. Navarro, and Eduard Ayguadé. Conflict–Free Strides for Vectors in Matched Memories. *Parallel Processing Letters*, vol. 1, no. 2, pp. 95–102, December 1992.

- Mateo Valero, Tomás Lang, José M. Llabería, Montse Peiron, Eduard Ayguadé, and Juan J. Navarro. Increasing the Number of Strides for Conflict–Free Vector Access. In *Proceedings of the 19th International Symposium on Computer Architecture (ISCA'92)*, pp. 372–381, Gold Coast (Australia), May 1992. Published on Computer Architecture News.

- Mateo Valero, Tomás Lang, and Eduard Ayguadé. Conflict–Free Access of Vectors with Power–of–Two Strides. In *Proccedings of the 6th ACM International Conference on Supercomputing (ICS'92)*, pp. 149–156, Washington D.C. (USA), July 1992.

- Mateo Valero, Montse Peiron, and Eduard Ayguadé. Access to Vectors in Multi–module Memories. In *Euromicro Workshop on Parallel and Distributed Processing*, pp. 228–236, Málaga (Spain), January 1994.

- Mateo Valero, Tomás Lang, Montse Peiron, and Eduard Ayguadé. Conflict–Free Access for Streams in Multimodule Memories. *IEEE Transactions on Computers*, vol. 44, no. 5, pp. 634–646, May 1995.

The out-of-order access method has been extended to the case of vector multiprocessor systems. Two operating modes have been considered. The first one assumes that all the processors in the system work together running a parallel application, and that they are synchronized to perform the accesses to different strips of a common data structure.

- Mateo Valero, Montse Peiron, and Eduard Ayguadé. Access to Streams in Multiprocessor Systems. In *Euromicro Workshop on Parallel and Distributed Processing*, pp. 310–316, Gran Canaria (Spain), January 1993.

- Montse Peiron, Mateo Valero, Eduard Ayguadé, and Tomás Lang. Conflict–Free Access to Streams in Multiprocessor Systems. In *19th Euromicro Conference*, pp. 119–130, Barcelona (Spain), September 1993. Published on Microprocessing and Microprogramming.

- Montse Peiron, Mateo Valero, Eduard Ayguadé, and Tomás Lang. Synchronized Access to Streams in Multiprocessors. *IEEE Technical Committee on Computer Architecture Newsletter*, pp. 37–41, 1993.

- Montse Peiron, Mateo Valero, and Eduard Ayguadé. Synchronized Access to Streams in SIMD Vector Multiprocessor. In *Proccedings of the 8th ACM International Conference on Supercomputing (ICS'94)*, pp. 23–32, Manchester (United Kingdom), July 1994.

On the other hand, the case of non-synchronized processors has been considered. In this case a global arbitration of the accesses to the memory system by the different processors is proposed to allow a minimum-latency access for vectors with strides belonging to the families which appear most frequently in real programs.

- Mateo Valero, Montse Peiron, and Eduard Ayguadé. Memory Access synchronization in Vector Multiprocessors. In *Joint International Conference on Vector and Parallel Processing (CONPAR'94 – VAPP VI)*, pp. 414–425, Linz (Austria), September 1994. Lecture Notes in Computer Science #854.

- Anna M. del Corral and José M. Llabería. Hardware Support to Reduce Conflicts between Vector Streams. In *2nd International Workshop on Massive Parallelism: hardware, Software and Applications*, pp. 90–104, Capri (Italy), October 1994.

- Anna M. del Corral and José M. Llabería. Out–of–Order Access to Vector Elements in order to Reduce Conflicts in Vector Processors. In *6th IEEE Symposium on Parallel and Distributed Processing (SPDP'94)*, pp. 126–134, Dallas (USA), October 1994.

- Mateo Valero, Eduard Ayguadé, and Montse Peiron. Network synchronization and Out–of–Order Access to Vectors. *Parallel Processing Letters*, vol. 4, no. 4, pp. 405–415, December 1994.

- Montse Peiron, Mateo Valero, Eduard Ayguadé, and Tomás Lang. Vector Multiprocessors with Arbitrated Memory Access. In *Proceedings of the 22nd International Symposium on Computer Architecture (ISCA'95)*, pp. 243–252, Sta. Margherita Ligure (Italy), June 1995. Published on Computer Architecture News.

- Anna M. del Corral and José M. Llabería. Access Order to Avoid Inter–Vector–Conflicts in Complex Memory Systems. In *9th International Parallel Processing Symposium (IPPS'95)*, pp. 404–410, Santa Barbara (USA), April 1995.

- Anna M. del Corral and José M. Llabería. Avoidig the Use of Buffers in Skewed Memory Systems for Vector Processors. In *International Conference on High Performance Computing (HiPC'95)*, pp. 105–110, New Delhi (India), December 1995.

- Anna M. del Corral and José M. Llabería. Reducing Inter–Vector–Conflicts in Complex Memory Systems. In *Proccedings of the 10th ACM International Conference on Supercomputing (ICS'96)*, pp. 382–389, Philadelphia (USA), May 1996.

- Anna M. del Corral and José M. Llabería. Increasing the Effective Memory Bandwidth in Multivector Processors. In *22nd Euromicro Conference*, pp. 38–45, Prague (Czech Republic), September 1996.

Finally, the design of new cache organizations and management policies to improve the cache performance is being studied, focussing specially in applications that use vector data.

- Toni Juan, Tomás Lang, and Juan J. Navarro. The Difference–bit Cache. In *Proceedings of the 23rd International Symposium on Computer Architecture (ISCA'96)*, pp. 114–121, Philadelphia (USA), May 1996.

- Antonio González, Carles Aliagas, and Mateo Valero. A Data Cache with Multiple Caching Strategies Tuned to Different Types of Locality. In *Proccedings of the 9th ACM International Conference on Supercomputing (ICS'95)*, pp. 338–347, Barcelona (Spain), July 1995.

Although cache–coherent shared–memory multiprocessors are sometimes used to run commercial workloads, little work has been done to characterize how well they support such applications. In particular, we do not have many insights on the demands of commercial workloads on the memory subsystem of such machines. We analyze the memory access patterns of several queries that are representative of Decision Support Systems (DSS) databases.

- Pedro Trancoso, Josep–L. Larriba–Pey, Zheng Zhang, and Josep Torrellas. The Memory Performance of DSS Commercial Workloads in Shared–Memory Multiprocessors. In *Proceedings of the Third International Symposium on High Performance Computer Architecture (HPCA'97)*, San Antonio, TX (USA), January 1997.

Instruction-Level Parallelism

Instruction-Level Parallelism is a topic that heavily relates architecture organization and compilation techniques. Related with this topic we are working in different areas:

ICTINEO: A compiler for ILP research. We are working on the implementation of a research tool to support our research on topics related with Instruction Level Parallelism. The tool, named ICTINEO is implemented on top of Polaris (from CSRD, University of Illinois at Urbana- Champaign). The key feature of ICTINEO is its high-level internal representation that allows us to do both high and low-level transformations and optimizations in a unified way. A description of the internal representation can be found in:

- Eduard Ayguadé, Cristina Barrado, Antonio González, Jesús Labarta, David López, Josep Llosa, Susana Moreno, David Padua, Fermín J. Reig, and Mateo Valero. Ictineo: A Tool for Research on ILP. In *Supercomputing'96*, Pittsburgh (USA), November 1996. Research Exhibit: "The Polaris Compiler: Use in Research and Education".

- Eduard Ayguadé, Cristina Barrado, Jesús Labarta, Josep Llosa, David López, Susana Moreno, David Padua, Enric Riera, and Mateo Valero. ICTÍNEO: Una Herramienta para la Investigación en Paralelismo a Nivel de Instrucciones. In *VI Jornadas de Paralelismo*, pp. 53–61, Barcelona (Spain), July 1995.

- Eduard Ayguadé, Cristina Barrado, Jesús Labarta, David López, Susana Moreno, David Padua, and Mateo Valero. A Uniform Representation for High–level and Instruction–Level Transformation. Technical Report UPC–CEPBA–95–01, European Center for Parallelism of Barcelona (UPC), 1995. Also published as UPC–DAC–95–02.

Register Requirements and Software Pipelining. Software pipelining is a loop scheduling technique that extracts parallelism from loops by overlapping the execution of several consecutive iterations. Agressive scheduling techniques such are software pipelining tend to increase the register requirements. We have evaluated the register requirements of software pipelined loops, and the effects on performance of the latency and number of functional units. As a result we have proposed novel software pipelining techniques that try to obtain schedules with minimum register requirements while producing near-optimal schedules in terms of throughput:

- Josep Llosa, Antonio González, Eduard Ayguadé, and Mateo Valero. Swing Modulo Scheduling: A Lifetim–Sensitive Approach. In *IFIP WG10.3 Working Conference on Parallel Architectures and Compilation Techniques (PACT'96)*, pp. 80–86, Boston (USA), October 1996.

- José González and Antonio González. Identifying Contributing Factors to ILP. In *22nd Euromicro Conference*, Prague (Czech Republic), September 1996.

- Josep Llosa, Mateo Valero, Eduard Ayguadé, and Antonio González. Hypernode Reduction Modulo Scheduling. In *28th Annual IEEE/ACM International Symposium on Microarchitecture (Micro–28)*, pp. 350–360, Ann Arbor, Michigan (USA), November 1995.

- Josep Llosa, Mateo Valero, and Eduard Ayguadé. Bidirectional Scheduling to Minimize Register Requirements. In *5th Workshop on Compilers for Parallel Computers*, pp. 534–554, Málaga (Spain), June 1995.

- Josep Llosa. Heuristics for Register Constrained Software Pipelining. Technical Report UPC–DAC–95–34, Departament Arquitectura de Computadors (UPC), 1995. Also published as UPC–CEPBA–95–23.

- Josep Llosa, Mateo Valero, Eduard Ayguadé, and Jesús Labarta. Register Requirements of Pipelined Loops and their Effect on Performance. In *2nd International Workshop on Massive Parallelism: hardware, Software and Applications*, pp. 173–189, Capri (Italy), October 1994.

Register file organizations. Despite of the efforts for producing schedules with minimum register requirements, the continuous grow on the instruction level parallelism that can be exploited in existing processors claims for a high number of available registers in future designs. Unfortunately having a high number of registers, as well as a high number of access ports to them has its drawbacks on the area required to implement them, and their access time. We have proposed several register file organizations in order to have a high number of registers, with a fast access time, and requiring less area than an equivalent multiported register file.

- Josep Llosa, Mateo Valero, and Eduard Ayguadé. Non–Consistent Dual Register Files to Reduce Register Pressure. In *Proceedings of the First International Symposium on High Performance Computer Architecture (HPCA'95)*, pp. 22–31, Raleigh, North Carolina (USA), January 1995.

- Josep Llosa, Mateo Valero, José A.B. Fortes, and Eduard Ayguadé. Using Sacks to Organize Registers in VLIW Machines. In *Joint International Conference on Vector and Parallel Processing (CONPAR'94 – VAPP VI)*, pp. 628–639, Linz (Austria), September 1994. Lecture Notes in Computer Science #854.

PhD Thesis on ILP.

- Josep Llosa. *Reducing the impact of register pressure on software pipelined loops.* PhD thesis, Universitat Politècnica de Catalunya (UPC), February 1996. Advisors Mateo Valero and Eduard Ayguadé.

This thesis deals with the high register requirements of software pipelined loops and their effects on performance. The work proposes several heuristics to perform register-constrained software pipelining. In order to reduce the performance penalty caused by register constraints, it proposes a new software pipelining technique that produces near-optimal schedules with low register requirements. Finally it proposes several register file organizations with the goal of having a large number of registers without degrading the access time and the area required to implement them.

Parallelization, Data Distribution and Loop Transformations

In this area, the group first focused on the exploitation of fine-grain parallelism in loops with tight recurrences for both shared and distributed-memory multiprocessor systems. The static estimation of loop performance metrics and the implementation of our proposals (Parafrase-2 and Alliant FX- 8) have also been tackled. The most relevant publications are the following:

- Cristina Barrado, Jesús Labarta, Eduard Ayguadé, and Mateo Valero. Generation a Periodic Pattern for VLIW. In *5th Workshop on Compilers for Parallel Computers*, pp. 485–502, Málaga (Spain), June 1995.

- Cristina Barrado, Jesús Labarta, Eduard Ayguadé, and Mateo Valero. Automatic Generation of Loop Scheduling for VLIW. In *IFIP WG10.3 Working Conference on Parallel Architectures and Compilation Techniques (PACT'95)*, pp. 306–309, Limassol (Cyprus), June 1995.

- Cristina Barrado, Jesús Labarta, and Patricia Borensztejn. Implementation of GTS. In *Proceedings of Parallel Architectures and Languages Europe (PARLE'94)*, pp. 565–576, Athens (Grece), June 1994. Lecture Notes in Computer Science #817.

- Cristina Barrado, Jesús Labarta, and Eduard Ayguadé. An Efficient Scheduling of DOACROSS Loops. In *Proceedings of Parallel and Distributed Computing and Systems*, pp. 303–307, Washington DC (USA), October 1994.

- Patricia Borensztejn, Jesús Labarta, and Cristina Barrado. Measures of Parallelism at Compile Time. In *Euromicro Workshop on Parallel and Distributed Processing*, pp. 253–258, Gran Canaria (Spain), January 1993.

- Jesús Labarta, Eduard Ayguadé, Jordi Torres, Mateo Valero, and José M. Llabería. *Balanced Loop Partitioning Using GTS*, chapter 19, pp. 298–312. Languages and Compilers for Parallel Computing, Lecture Notes in Computer Science #589. Springer–Verlag, 1992.

- Eduard Ayguadé, Jesús Labarta, Jordi Torres, José M. Llabería, and Mateo Valero. *Parallelism Evaluation and Partitioning of Nested Loops for Shared Memory Multiprocessors*, chapter 11, pp. 220–242. Advances in Languages and Compilers for Parallel Computing, Research Monographs in Parallel and Distributed Computing. Pitman/MIT Publishers, 1991.

- Eduard Ayguadé, Jesús Labarta, Jordi Torres, José M. Llabería, and Mateo Valero. Nested–Loop Partitioning for Shared–Memory Multiprocessor Systems. In *2nd Workshop on Compilers for Parallel Computers*, pp. 378–385, Paris (France), December 1990.

More recently, the group focused on the automatic data distribution and loop parallelization for both distributed and coherent cache-based shared memory multiprocessor systems (like Convex Exemplar or SGI Power Challenge). The analysis is done based on an estimation of the trade-offs between data movement and reduction of execution time due to parallel execution. DDT (Data Distribution Tool, on top of ParaScope) is the result of this research and generates directives either from the HPF, PFA from Silicon or Exemplar from Convex programming models. The most relevant publications are the following:

- Jordi Garcia, Eduard Ayguadé, and Jesús Labarta. Using a 0–1 Integer Programming Model for Automatic Static Data Distribution. *Parallel Processing Letters*, vol. 6, no. 1, pp. 159–171, 1996.

- Eduard Ayguadé, Jordi Garcia, Merce Girones, M. Luz Grande, and Jesús Labarta. A Research Tool for Automatic Data Distribution in HPF. *Scientific Programming*, vol. 6, no. 1, pp. 73–95, 1997. Special Issue on Implementations of HPF.

- Eduard Ayguadé, Jordi Garcia, M. Luz Grande, and Jesús Labarta. Data Distribution and Loop Parallelization for Shared–memory Multiprocessors. In *9th International Workshop on Programming Languages and Compilers for Parallel Computing*, San José, CA (USA), August 1996.

- Jordi Garcia, Eduard Ayguadé, and Jesús Labarta. A Framework for Automatic Dynamic Data Mapping. In *8th IEEE Symposium on Parallel and Distributed Processing (SPDP'96)*, pp. 92–99, New Orleans, Luisiana (USA), October 1996.

- Eduard Ayguadé, Jesús Labarta, Jordi Garcia, Merce Girones, and Mateo Valero. Analyzing Reference Patterns in Automatic Data Distribution Tools. *International Journal of Parallel Programming*, vol. 23, no. 6, pp. 515–535, December 1995.

- Jordi Garcia, Eduard Ayguadé, and Jesús Labarta. A Novel Approach towards Automatic Data Distribution. In *Supercomputing'95*, San Diego (USA), December 1995. Also presented at Workshop on Automatic Data Layout and Performance Prediction, Rice University, April 1995.

- Eduard Ayguadé, Jordi Garcia, Merce Girones, M. Luz Grande, and Jesús Labarta. Data Redistribution in an Automatic Data Distribution Tool. In *8th International Workshop on Programming Languages and Compilers for Parallel Computing*, pp. 271–287, Columbus, Ohio (USA), August 1995. Lecture Notes in Computer Science #1033.

- Eduard Ayguadé, Jordi Garcia, Merce Girones, Jesús Labarta, Jordi Torres, and Mateo Valero. Detecting and Using Affinity in an Automatic Data Distribution Tool. In *7th International Workshop on Programming Languages and Compilers for Parallel Computing*, pp. 61–75, Ithaca, NY (USA), August 1994. Lecture Notes in Computer Science #892.

- Eduard Ayguadé, Jesús Labarta, Jordi Garcia, Merce Girones, and Mateo Valero. Detecting Affinity for Automatic Data Distribution. In *2nd International Workshop on Massive Parallelism: hardware, Software and Applications*, pp. 32–46, Capri (Italy), October 1994.

- Eduard Ayguadé, Jesús Labarta, Jordi Garcia, Merce Girones, and Mateo Valero. A Study of Data Sets and Affinity in the Perfect Club. In *4th Workshop on Compilers for Parallel Computers*, Delft (The Netherlands), December 1994.

We have also proposed a methodology based on linear loop transformations to systematically transform sequential loops in order to enable their parallelization. The methodology is targeted towards distributed memory multicomputers starting from the sequential program.

- Agustín Fernández, José M. Llabería, and Miguel Valero–García. Loop Transformation Using Non–unimodular Matrices. *IEEE Transactions on Parallel and Distributed Systems*, vol. 6, no. 8, pp. 832–840, August 1995.

- Agustín Fernández, José M. Llabería, Juan J. Navarro, and Miguel Valero–García. Transformation of Systolic Algorithms for Interleaving Partitions. In *Application Specific Array Processors (ASAP'91)*, pp. 56–71, Platja d'Aro (Spain), September 1991.

- Agustín Fernández, José M. Llabería, Juan J. Navarro, and Miguel Valero–García. Interleaving Partitions of Systolic Algorithms for Programming Distributed Memory Multiprocessors. In *The 2nd European Distributed Memory Computing Conference EDMCC2*, pp. 90–99, Munich (Germany), April 1991. Lecture Notes in Computer Science #487.

The use of different linear loop transformations oriented towards the exploitation of parallelism for shared memory multiprocessors has also been subject of research. Either the use of an alignment component or a different unimodular transformation for each statement in the loop body have been the main contributions of this work, published in the following papers:

- Eduard Ayguadé, Peter Knijnenburg, and Jordi Torres. Multi–Transformations: Definition and Usefulness. In *XV International Conference of the Chilean Computer Science Society*, pp. 37–47, Arica (Chile), November 1995.

- Jordi Torres, Eduard Ayguadé, Jesús Labarta, and Mateo Valero. Loop Parallelization: Revisiting Framework of Linear Loop Transformations. In *Proceedings of the Parallel and Distributed Processing Symposium*, pp. 420–427, Braga (Portugal), January 1996. Also in 5th Workshop on Compilers for Parallel Computers, Málaga (Spain), June 1995.

- Eduard Ayguadé and Jordi Torres. Partitioning the Statement per Iteration Space Using Non–singular Matrices. In *Proccedings of the 7th ACM International Conference on Supercomputing (ICS'93)*, pp. 407–415, Tokyo (Japan), July 1993.

- Jordi Torres, Eduard Ayguadé, Jesús Labarta, and Mateo Valero. ALIGN and DISTRIBUTE–Based Linear Loop Transformations. In *6th International Workshop on Programming Languages and Compilers for Parallel Computing*, pp. 321–339, Portland, OR (USA), August 1993. Lecture Notes in Computer Science #768.

Also we are working on a new unified method for simultaneously tiling the register and cache levels of the memory hierarchy. We will focus on the code transformation phase of tiling. Our algorithm uses strip-mining and loop interchange on all memory hierarchy levels to determine the tiles as usual, and, afterwards, and due to the special characteristics of the register level, we apply index set splitting, fully unrolling and unnecessary load/store elimination. We propose a technique to perform the loop interchange in non-convex iteration spaces that computes the loop bounds exactly and we also present an order in which to perform index set splitting that guaranties that each loop in the nest will be processed only once and also avoids code explosion.

The performance of the memory hierarchy obtained with our method is substantially higher than the performance obtained by commercial preprocessors capable of restructuring code to exploit the memory hierarchy. The main contributions of this work are published in the following papers:

- Marta Jiménez, José M. Llabería, Agustín Fernández, and Enric Morancho. A Unified Transformation Technique for Multilevel Blocking. In *2nd International Euro–Par Conference (Euro–Par'96)*, pp. 402–405, Lyon (France), August 1996. Lecture Notes in Computer Science #1123.

- Marta Jiménez, José M. Llabería, Agustín Fernández, and Enric Morancho. Multilevel Blocking in Complex Iteration Spaces. In *VII Jornadas de Paralelismo*, pp. 229–244, Santiago de Compostela (Spain), September 1996.

- Marta Jiménez, José M. Llabería, Agustín Fernández, and Enric Morancho. A Unified Transformation Technique for Multilevel Blocking. Technical Report UPC–DAC–95–51, Departament Arquitectura de Computadors (UPC), 1995.

Algorithms and Architectures for Linear Algebra and Sparse Matrix computations

We are working in multilevel block algorithms applied to dense and general sparse matrices. First of all, it has been studied, proposed, developed and evaluated multilevel block algorithms. The main goal of multilevel block algorithms is to optimize the locality exploitation of data in linear algebra operations. The target architectures of multilevel block algorithms are those with several levels in the memory hierarchy. The different forms of the algorithms have been classified and we have proved that one of them, that we call MOB, is optimal in performance and can be easily designed. The performance improvements obtained with the MOB algorithms are outstanding.

In the design of the multilevel block algorithms, in addition to the conflicts that appear in cache lines, we consider TLB misses and page faults. The evaluation of MOB algorithms is done theoretically on a memory hierarchy model and is validated with trace-driven simulations and experimental measurements on two new computers that use high performance microprocessors.

- Juan J. Navarro, Elena García, and Josep R. Herrero. Data Prefetching and Multilevel Blocking for Linear Algebra Operations. In *Proccedings of the 10th ACM International Conference on Supercomputing (ICS'96)*, pp. 109–116, Philadelphia (USA), May 1996.

- Juan J. Navarro, Elena García, Josep–L. Larriba–Pey, and Toni Juan. Block Algorithms for Sparse Matrix Computations on High Performance Workstations. In *Proccedings of the 10th ACM International Conference on Supercomputing (ICS'96)*, pp. 301–308, Philadelphia (USA), May 1996.

- Juan J. Navarro, Toni Juan, and Tomás Lang. MOB Forms: A Class of Multilevel Block Algorithms for Dense Linear Algebra Operations. In *Proccedings of the 8th ACM International Conference on Supercomputing (ICS'94)*, pp. 325–334, Manchester (United Kingdom), July 1994.

- Juan J. Navarro, Toni Juan, Mateo Valero, José M. Llabería, and Tomás Lang. Multilevel Orthogonal Blocking for Dense Linear Algebra Computations. *IEEE Technical Committee on Computer Architecture Newsletter*, pp. 10–14, 1993.

For the case of sparse linear systems, parallel algorithms have been implemented.

- José M. Cela, Jesús Labarta, and Juan J. Navarro. Performance on Distributed Memory Multicomputers of Domain Decomposition Solvers. In *7th SIAM Conference on Parallel Processing for Scientific Computing*, pp. 391–392, San Francisco (USA), February 1995.

- José M. Cela, Albert Pujolar, and Juan J. Navarro. Standard PDEs Solvers vs. Domain Decomposition Solvers on Vector Multiprocessors. In *Proceedings of the IASTED International Symposium on Applied Informatics*, pp. 230–235, Annecy (France), May 1993.

The basic approach of this piece of work is to extract the coarse grain parallelism that those applications have. In order to do so, domain decomposition techniques have been used and a message passing programming model on a distributed memory multicomputer have been assumed. All this work is related to project ESPRIT-6753 (IDENTIFY) in collaboration with the British Rutherford Appleton Laboratory and the French company Bertin et Cie. In particular, the developed software can be applied to Fluid Dynamics problems. The role of our research group in the project was to implement the linear solvers for the project. Some of the methods developed are: i) Element by element methods, ii) Iterative methods on the global matrix, iii) Iterative methods on the Schur Complement matrix. In addition, we have also implemented the corresponding software for the assembly of the matrices which is necessary for methods (ii) and (iii). This latter software allows the assembly both from a finite volume discretization and from a finite element discretization.

With the objective of improving the efficiency of the parallel solvers, different reordering algorithms have been included in the code. Those algorithms have the aim of reducing the band and increment the parallelism. Some of those algorithms process elements within submatrices and others process submatrices within the global matrix.

Within the field of sparse linear systems, one can find banded linear systems. This type of problems appears in the discretization of partial differential equations. The size of the band can vary from one only subdiagonal (bidiagonal matrices) to tens of diagonals. The work developed has focussed on three different parts. In a first part, algorithms have been studied for narrow banded systems (bidiagonal and tridiagonal). Those methods have been studied for their execution on vector processors in:

- Josep–L. Larriba–Pey, Juan J. Navarro, Angel Jorba, and Oriol Roig. Review of general and Toeplitz Bidiagonal Solvers. *Parallel Computing*, vol. 22, no. 8, pp. 1091–1125, 1996.

- Josep–L. Larriba–Pey, Juan J. Navarro, Angel Jorba, and Oriol Roig. A generalized vision of some parallel bidiagonal systems solvers. In *Proccedings of the 8th ACM International Conference on Supercomputing (ICS'94)*, pp. 404–411, Manchester (United Kingdom), July 1994.

In the second part, the methods studied above have been analyzed for strictly diagonal dominant systems of equations. New methods have been proposed for the solution of those systems. The study has a mathematical component to prove the accuracy of the methods and an architectural component to study the methods on specialized architectures:

- Josep–L. Larriba–Pey, Angel Jorba, and Juan J. Navarro. A generalized criterion for the early termination of R–Cyclic Reduction and Divide and Conquer for recurrences. In *7th SIAM Conference on Parallel Processing for Scientific Computing*, pp. 448–453, San Francisco (USA), February 1995.

- Josep–L. Larriba–Pey, Angel Jorba, and Juan J. Navarro. A Parallel Tridiagonal Solver for Vector Uniprocessors. In *6th SIAM Conference on Parallel Processing for Scientific Computing*, pp. 590–597, Norfolk, VA (USA), March 1993.

- Josep–L. Larriba–Pey, Angel Jorba, and Juan J. Navarro. Overlapped Partitions versus Tricyclic Reduction: Races on the C–3400. In *Convex User Group Worlwide Conference*, pp. 150–155, Richardson, TX (USA), March 1993.

- Josep–L. Larriba–Pey, Angel Jorba, and Juan J. Navarro. Spike Algorithm with savings for strictly diagonal dominant tridiagonal systems. *Microprocessing and Microprogramming*, vol. 39, pp. 125–128, October 1993.

Finally, a study of the algorithms for different applications has been carried out:

- Josep–L. Larriba–Pey, Juan J. Navarro, and Angel Jorba. Vector and parallel interpolation by Natural Cubic Splines and B–Splines. In *Proceedings of the Parallel and Distributed Processing Symposium*, pp. 385–392, Braga (Portugal), January 1996.

- Josep–L. Larriba–Pey, M. Mascagni, Angel Jorba, and Juan J. Navarro. An Analysis of the Parallel Computation of Arbitrarily Branched Cable Neuron Models. In *7th SIAM Conference on Parallel Processing for Scientific Computing*, pp. 373–378, San Francisco (USA), February 1995.

Microkernel Technology Support to Parallel Applications

Our topics of research are user-level libraries and microkernels on shared memory multiprocessor architectures. The goal is the promotion of the cooperation between user-level and kernel-level resource schedulers to fit the needs of parallel applications. Mach 3.0 and Cthreads are our departure platform.

More specifically, we look for cooperation between kernel and user levels through processor and physical memory partitioning, affinity and memory conscious scheduling, event notifications to user level: upcalls, scheduler activations, user-level servers (policies) and kernel tunable scheduling mechanisms by processor sets and memory sets.

We are involved in the development of a new parallel execution environment implemented directly on top of the microkernel abstractions composed by servers (loader, pager, parallel i/o server and measurement server) and libraries (user threads and upcalls management). The goal consists in execute parallel applications by use of kernel extensions that enable new functionalities based on physical processors and memory space partitioning techniques, without compromising system reliability.

We have implemented user-level scheduling policies and mechanisms: hints, handoff, user level efficient context switch, priorities, locks with priorities or hints, non blocking and preemptive ready queues management and support to scheduling activations from kernel upcalls.

The validation of our designs is done through porting and evaluating the performance of parallel applications (like those in the SPLASH suite or based on the PARMACS macros) to run on standard Mach 3.0 and our environment.

- Marisa Gil, Toni Cortés, Angel Toribio, and José I. Navarro. Towards User–Level Parallelism with Minimal Kernel Support on Mach. In *Workshop On Microkernel Technology for Distributed Systems, OSF*, Grenoble (France), June 1993.

- Marisa Gil, Xavier Martorell, and José I. Navarro. The Enhancement of a User–level Thread Package Scheduling on Multiprocessors. In *2nd International Conference on Software for Multiprocessors and Supercomputers, Theory, Practique and Experience*, pp. 390–398, Moscow (Russia), September 1994.

- Marisa Gil, Xavier Martorell, and José I. Navarro. The eXc Model: Scheduler–Activations on Mach 3.0. In *7th IAESTED/ISMM International Conference on Parallel and Distributed Computing Systems*, pp. 5–10, Washington D.C. (USA), October 1995.

Operating Systems for Parallel Machines

Within this topic, we have worked in several areas. First, we have designed and implemented PAROS a micro-kernel operating syststem for distributed memory multiprocessors. Second, we are also working on processor scheduling policies aimed for message passing applications focussing on a temporal sharing of coarse and fine grain communications. The application of these can be done both in massively parallel and workstation networks. Finally, we are working on a parallel/distributed file system with a cooperative cache aimed for parallel machines or networks of workstations.

We have also developped a set of analisys and visualization tools which ease the study of the above topics. All these tools are part of the DiP project.

PAROS

- Cristina Pujol, Jesús Labarta, Luis Gregoris, and Sergi Girona. Paros Kernel Free Distribution v1.2 User Manual. Technical Report UPC–CEPBA–94–07, European Center for Parallelism of Barcelona (UPC), 1994. Also published as UPC–DAC–94–12.

- Jesús Labarta, Judit Giménez, Cristina Pujol, and Teodor Jové. Multiprogramming parallel applications on the Paros operating system kernel. In *Euromicro Workshop on Parallel and Distributed Processing*, pp. 474–480, Gran Canaria (Spain), January 1993.

- Jesús Labarta, Cristina Pujol, Teodor Jové, and José I. Navarro. Paros: Operating System Kernel for Distributed Memory Multiprocessors. In *Parallel Computing and Transputer Applications (PACTA'92)*, pp. 673–682, Barcelona (Spain), September 1992.

Processor Scheduling

- Jesús Labarta, Sergi Girona, and Toni Cortés. Analyzing scheduling policies using Dimemas. In *Environments and Tools For Parallel Scientific Computing III (ETPSC III)*, Faverges de la Tour (France), August 1996.

- Sergi Girona, Toni Cortés, Jesús Labarta, Vincent Pillet, Andrés Pérez, and Elena García. Resource Management Policies, 1994. Deliverable OPS4A of the project "Basic research APPARC".

Parallel/Distributed File Systems

- Toni Cortés, Sergi Girona, and Jesús Labarta. PACA: A Cooperative File System Cache for Parallel Machines. In *2nd International Euro–Par Conference (Euro–Par'96)*, pp. 477–486, Lyon (France), August 1996. Lecture Notes in Computer Science #1123.

- Toni Cortés, Sergi Girona, and Jesús Labarta. PACA: a Cooperative File System Cache. In *VII Jornadas de Paralelismo*, pp. 245–258, Santiago de Compostela (Spain), September 1996.

Analisys and Visualization Tools

- Jesús Labarta, Sergi Girona, Vincent Pillet, Toni Cortés, and Luis Gregoris. DiP: A Parallel Program Development Environment. In *2nd International Euro–Par Conference (Euro–Par'96)*, pp. 665–674, Lyon (France), August 1996. Lecture Notes in Computer Science #1124.

- Jesús Labarta, Sergi Girona, Vincent Pillet, Toni Cortés, and José M. Cela. Un entorno para el desarrollo de programas paralelos. In *VI Jornadas de Paralelismo*, pp. 77–84, Barcelona (Spain), July 1995.

- Vincent Pillet, Jesús Labarta, Toni Cortés, and Sergi Girona. PARAVER: PARAllel Visualization and Events Representation. In *The 18th Technical Meeting of WoTUG*, pp. 17–31, Amsterdam (The Netherlands), April 1995.

We are also working in the interaction between the operating system and the compiler. The compiler can provide the operating system with information (obtained from an static analysis of the code) that is not offered by the user and can not be obtained at run-time by the operating system. This information may be useful to effectively exploit both parallelism in an application and multiprogrammed execution in tightly-coupled systems.

- Xavier Martorell, Jesús Labarta, José I. Navarro, and Eduard Ayguadé. A Library Implementation of the Nano–Threads Programming Model. In *2nd International Euro–Par Conference (Euro–Par'96)*, pp. 644–649, Lyon (France), August 1996. Lecture Notes in Computer Science #1124.

Systematic mapping of algorithms to hardware

We have proposed a systematic method for mapping systolic algorithms to hardware. This method covers several topics: partitioning, data input / output, efficiently use of Process Elements. An important topic is code generation. The starting point is the sequential code. All used transformations modify code and finally we obtain the parallel code of every Process Element of the Systolic Processor.

- Miguel Valero–García, Juan J. Navarro, José M. Llabería, Mateo Valero, and Tomás Lang. *Mapping QR Decomposition of Bounded Matrix on a 1D Systolic Array*, pp. 25–38. Elsevier Publishers, 1992.

- Alvaro Suárez, José M. Llabería, and Agustín Fernández. Scheduling Partitionings in Systolic Algorithms. In *Application Specific Array Processors (ASAP'92)*, pp. 619–633, Berkeley (USA), August 1992.

- Alvaro Suárez. *Ordenación de la ejecución de particiones en algoritmos sistólicos*. PhD thesis, Universitat Politècnica de Catalunya (UPC), November 1993. Advisor José M. Llabería.

- Miguel Valero–García, Juan J. Navarro, José M. Llabería, and Mateo Valero. Implementation of Systolic Algorithms Using Pipelined Functional Units. In *Application Specific Array Processors (ASAP'90)*, pp. 272–283, Princeton, NJ (USA), September 1990.

In the other hand, one method to execute efficiently parallel algorithms with hypercube communication topology (i.e. FFT algorithms, All-to-All personalized communications, Jacobi methods for singular value decomposition and eigenvalue computation) on torus multicomputers has been developed. It was proposed and evaluated a new embedding of hypercubes on torus multicomputers. It was shown that this embedding is optimal for rings in terms of execution time. In addition, some new techniques to reduce the communication costs in hypercube algorithms have been studied.

- Luis Díaz de Cerio, Miguel Valero–García, and Antonio González. Overlapping Communication and Computation in Hypercubes. In *2nd International Euro–Par Conference (Euro–Par'96)*, pp. 253–257, Lyon (France), August 1996. Lecture Notes in Computer Science #1123.

- Antonio González, Miguel Valero–García, and Luis Díaz de Cerio. Executing Algorithms with Hypercube Topology on Torus Multicomputers. *IEEE Transactions on Parallel and Distributed Systems*, vol. 6, no. 8, pp. 803–814, August 1995.

- Luis Díaz de Cerio, Miguel Valero–García, and Antonio González. A Study of the Communication Cost of the FFT on Torus Multicomputers. In *1st IEEE International Conference on Algorithms and Architectures for Parallel Processing*, pp. 131–139, Brisbane (Australia), April 1995.

- Luis Díaz de Cerio, Miguel Valero–García, and Antonio González. Efficient FFT on Torus Multicomputers: A Performance Study. In *2nd Austrian–Hungarian Workshop on Transputer Applications*, pp. 233–242, Budapest (Hungary), September 1994.

- Miguel Valero–García and Antonio González. FFT on Massively Parallel Processors. In *COST 229 Workshop on Massively Parallel Computing*, pp. 1–9, Madeira (Portugal), April 1993.

- Antonio González and Miguel Valero–García. The Xor Embedding: An Embedding of Hypercubes onto Rings and Toruses. In *Application Specific Array Processors (ASAP'93)*, pp. 15–28, Venecia (Italy), October 1993.

Execution of Applications based on the Declarative Programming Paradigm

Definition of a novel execution model for Prolog programs, called Multipath, that combines a depth and a breadth traversal of the search tree related to programs. The main idea consists of the possibility to traverse simultaneously more than one path of the search tree, which reduces the number of control and data instructions that would be executed in the standard execution model of Prolog. This execution model is well suited for non-deterministic programs.

Multipath can be implemented on several architectural models: from sequential environments (SISD) to parallel architectures (MIMD, SPMD) exploiting data parallelism.

- Jordi Tubella and Antonio González. Exploiting Path Parallelism in Logic Programming. In *Euromicro Workshop on Parallel and Distributed Processing*, pp. 164–173, San Remo (Italy), January 1995.

- Jordi Tubella and Antonio González. A Partial Breadth–First Execution Model for Prolog. In *6th IEEE International Conference on Tools with Artificial Intelligence TAI'94*, pp. 129–137, New Orleans (USA), November 1994.

- Antonio González and Jordi Tubella. The Multipath Parallel Execution Model for Prolog. In *1st International Conference on Parallel Symbolic Computation PASCO'94*, pp. 164–173, Linz (Austria), September 1994.

- Jordi Tubella and Antonio González. Combining Depth–First and Breadth–First Search in Prolog Execution. In *Joint Conference on Declarative Programming GULP–PRODE'94*, pp. 452–453, Peñíscola (Spain), September 1994.

- Jordi Tubella and Antonio González. MEM: A New Execution Model for Prolog. *Microprocessing and Microprogramming*, vol. 39, no. 2–5, pp. 83–86, November 1993.

- Jordi Tubella and Antonio González. Measuring Scheduling Policies in Pure Or–Parallel Program. In *2nd Conference on Declarative Programming PRODE'93*, pp. 57–71, Blanes (Spain), September 1993.

- Antonio González, Jordi Tubella, and Carles Aliagas. An Evaluation Tool for the EDS Parallel Logic Programming System. In *European Workshop on Parallel Computing EWPC'92*, pp. 566–569, Sitges (Spain), March 1992.

- Jordi Tubella and Antonio González. Design and Evaluation of a Two–Level Hierarchical Multiprocessor for Logic Programming. In *Proceedings of the IASTED International Symposium on Applied Informatics*, pp. 45–48, Innsbruck (Austria), February 1992.

3.2.2 R+D Projects and Agreements

- **Effective Integration of Fine-Grain Parallelism Exploitation and Multiprogramming**
  Project length: October, 1996 – September, 1999.
  Funding body: CEC/ESPRIT P21907.
  Budget Funding: 107.7 M. ptas.
  Holder: Mateo Valero.
  Partners: Consiglio Nazionale Ricerche (CNR), PALLAS-Gesellschaft Fur Parallele Anwendungen und Systeme, University of Patras.

- **Parallel Computing and Modelling for Industrial Problems**
  Project length: July, 1996 – June, 1999.
  Funding body: CEC/INCO CONTRACT 950845.

Budget Funding: 9.6 M. ptas.
Holder: Mateo Valero.
Partners: Laboratoire d'Informatique du Parallelisme (LIP), Universidad de Chile-DIM, INRIA-Rocquencourt: Promath Project Team, Universidad de la República (IMERL), MATRA CAP Systems S.A. (MCS), UITESA, Eléctrica Pehuenche, S.A., Centro de Investigación Minera y Metalúrgica (CIMM), Administración de Usinas y Transmisiones Eléctricas (UTE).

- **Short and Lomgterm Optimization of Electricity Generation and Trading**
  Project length: December, 1996 – May, 1999.
  Funding body: CEC/ESPRIT 22695.
  Budget Funding: 14.5 M. ptas.
  Holder: Mateo Valero.

- **Parmat-Efficient Handling of Large Matrices on High Parallel Computer Systems With the Permas Code**
  Funding body: CEC/ESPRIT CONTRACT 22740.
  Budget Funding: 32.7 M. ptas.
  Holder: Mateo Valero.

- **Access to Large Scale Facilities Activity of the Training amd Movility of Researchers**
  Project length: January, 1996 – December, 1998.
  Funding body: CEC/TMR ERBFMGECT95-0062.
  Budget Funding: 96.0 M. ptas.
  Holder: Mateo Valero.

- **PCI-II Parallel Computing Iniciative**
  Project length: April, 1996 – May, 1998.
  Funding body: CEC/ESPRIT 21037.
  Budget Funding: 48.8 M. ptas.
  Holder: Mateo Valero.

- **Parallelisation of the Chirp Scaling Algorithm Sar Processor**
  Project length: April, 1996 – September, 1997.
  Funding body: CEC/ESPRIT 21037.
  Budget Funding: 1.6 M. ptas.
  Holder: Mateo Valero.

- **Stampar Development of a Proposal Sftware for Enhanced Design of Sheet Stamping Dies**
  Project length: April, 1996 – September, 1997.
  Funding body: CEC/ESPRIT 21037.
  Budget Funding: 5.6 M. ptas.
  Holder: Mateo Valero.

- **Development and Parallelization of Reactive Transport Codes of Use in Environment Management Strategies**
  Project length: April, 1996 – September, 1997.
  Funding body: CEC/ESPRIT 21037.
  Budget Funding: 8.0 M. ptas.
  Holder: Mateo Valero.

- **Parallelization of a Glass Manufacturing Modelling Code**
  Project length: April, 1996 – September, 1997.
  Funding body: CEC/ESPRIT 21037.
  Budget Funding: 3.0 M. ptas.
  Holder: Mateo Valero.

- **Promenvir-High Performance Computer-Based Probabilistic Mechanical Design Environment**
  Project length: January, 1996 – December, 1997.
  Funding body: CEC/ESPRIT P20189.
  Budget Funding: 23.0 M. ptas.
  Holder: Mateo Valero.
  Partners: Construcciones Aeronáuticas S.A., Centro de Estudios e Investigaciones Técnicas de Guipúzcoa (CEIT), Universitat Stuttgart (RUS), Italdesign Spa, IKO Software Service, The University of Southampton, The Parallel Application Centre (PAC), Blue Engineering Srl.

- **Contract ERBCHGECT92-0009**
  Project length: April, 1993 – August, 1997.
  Funding body: CEC/CAPITAL HUMÀ I MOBILITAT.
  Budget Funding: 8.4 M. ptas.
  Holder: Mateo Valero.

- **Access to Supercomputing Facilities for European Researchers (Human Capital and Mobility, EEC).**
  Project length: April, 1993 – August, 1997.
  Funding body: CEC/CAPITAL HUMÀ I MOBILITAT CT92-0009.
  Budget Funding: 39.8 M. ptas.
  Holder: Mateo Valero.
  Partners: CESCA, CEPBA.

- **Parallel Computing Iniciative**
  Project length: June, 1994 – August, 1996.
  Funding body: CEC/ESPRIT 9602.
  Budget Funding: 26.3 M. ptas.
  Holder: Mateo Valero.
  Partners: IBERDROLA, UITESA, Universidad Politécnica de Valencia, Métodos Cuantitativos, GONFIESA, CESCA, TECNATOM, Universidad de Málaga, AMES, Ayuntamiento de Barcelona, NEOSYSTEMS, Hespedia de Alimentación, AZTI, Tecnologia y Gestión de la Información (TGI), Universidad Politécnica de Madrid.

- **Ships Software Supercomputer Highly Parallel System**
  Project length: July, 1994 – December, 1995.
  Funding body: CEC/ESPRIT P9601.
  Budget Funding: 68.9 M. ptas.
  Holder: Mateo Valero.
  Partners: ACRI, ACSET, ARTT, BAE SRC, CHAM, GENIAS, IBD, INTERA, MSC GMBH, PARTEX, DAC (UPC Associated).

- **PERMPAR dins el Marc Europort1**
  Project length: January, 1994 – December, 1995.
  Funding body: CEC/ESPRIT EP8421.
  Budget Funding: 12.7 M. ptas.
  Holder: Mateo Valero.
  Partners: CEPBA (UPC Associated), CESCA, GMD, INTES, Bureau Veritas, IRCN.

- **Gran Instal.lació en el Programa Dem la C.E.E. Capital Humà i Mobilitat**
  Project length: April, 1993 – March, 1995.
  Funding body: FUNDACIÓ CATALANA PER A LA RECERCA.
  Budget Funding: 7.8 M. ptas.
  Holder: Mateo Valero.

- **Contract 7417 Ca. 2 Advanced Computer Training and Technology Transfer**
  Project length: July, 1992 – May, 1995.
  Funding body: CEC/COMETT.
  Budget Funding: 8.4 M. ptas.
  Holder: Mateo Valero.

- **Supercomputer Highly Parallel System**
  Department contribution: Evaluation of a set of linear algebra and FFT algorithms when executed on a single processor and when executed on the multiprocessor systems designed in the project.
  Project length: June, 1992 – May, 1995.
  Funding body: CEC/ESPRIT P6253.
  Budget Funding: 61.1 M. ptas.
  Holder: Mateo Valero.
  Partners: Advanced Computer Research Institute (ACRI) (coordinator), Advanced Computer & Software Eng. Tech. (ACSET), Sekas Gmbh, Foundation of Research & Technology-Hellas (FORTH), Phoenix Vlsi, University of Edinburgh, University of Manchester, DAC (UPC, associated).

- **Performance Critical Application of Parallel Architectures**
  Department contribution: Proposal of techniques for the efficient access to multimodule memories and memory hierarchy. Proposal of compilation techniques to optimize program locality.
  Project length: July, 1992 – July, 1995.
  Funding body: CEC/ESPRIT 6634.
  Budget Funding: 22.3 M. ptas.
  Holder: Mateo Valero.
  Partners: Rijks Universiteit te Leiden (coordinator), UNI-C, KFA-Kernforschungsanlage Juelich Gmbh, University of Manchester, DAC (UPC, associated), University of Patras, Queen's Univesity Belfast.

- **Suport al Centre Europeu de Paral.lelisme de Barcelona**
  Department contribution: Teaching and collaboration on the vectorization and parallelization of sequential algorithms.
  Project length: May, 1991 – May, 1995.
  Funding body: CONVEX Supercomputer SAE (Ibérica).
  Budget Funding: 12.0 M. ptas.
  Holder: José M. Llabería.
  Partners: UPC, CONVEX Supercomputers SAE.

- **Investigació sobre Computació**
  Department contribution: Algorithm characterization and performance evaluation.
  Project length: May, 1991 – May, 1995.
  Funding body: CONVEX SUPERCOMPUTER SAE (IBÉRICA.
  Budget Funding: 12.0 M. ptas.
  Holder: Mateo Valero.
  Partners: UPC, CONVEX Supercomputers SAE.

- **Interactive Desing Using a Network of Transputer in Fluids**
  Department contribution: Design and implementation of efficient parallel algorithms to solve systems of equations that use big sparse matrices.
  Project length: May, 1992 – October, 1994.
  Funding body: CEC/ESPRIT P6753.
  Budget Funding: 51.0 M. ptas.
  Holder: Mateo Valero.

Partners: Bertin & Compagnie S.A. (coordinator), Industrias de Optica S.A. (INDO), Serc-Rutherford Appleton Laboratory Nir (RAL), DAC (UPC, associated), Parsys Ltd., Bayerische Motorenwerke AG (BMW).

- **Automatic Data Distribution for the Convex MPP**
  Department contribution: Characterization of real programs in terms of access to dimensional data structures. Implementation and evaluation of data alignment and distribution techniques for massively parallel compilers.
  Project length: 1991 – 1994.
  Funding body: CONVEX Computer Corporation (USA) and CONVEX Supercomputers SAE..
  Holder: Mateo Valero.
  Partners: UPC.

- **Automatic Data Distribution**
  Department contribution: Implement the Li & Chen partitioning method and communication free method on Parascope Evaluate the efficiency of results. Propose improvements.
  Project length: 1991 – 1994.
  Funding body: Convex Computer Corp., Convex Supercomputer SAE.
  Holder: Jesús Labarta and Eduard Ayguadé.
  Partners: Convex Computer Corp., Convex Supercomputer SAE, UPC.

3.2.3 Grants

- **Computación Paralela para el Modelado de Problemas Industriales** (1996–1999) (CICYT TIC–1630/96).
  Budget Funding: 2.0 M. ptas.
  Holder: Eduard Ayguadé.

- **Entorno de Diseño Mecánico Probabilístico Basado en Computaciones de Altas Prestaciones** (1996–1998) (CICYT TIC–1980/96).
  Budget Funding: 1.5 M. ptas.
  Holder: José M. Cela.

- **High Performance Computing** (1995–1998) (CICYT TIF–429/95).
  Budget Funding: 100.6 M. ptas.
  Holder: Mateo Valero.

- **Equipo de Conexión Remota y Gestión de Espacio en Disco** (1996–1997) (CICYT IN–209/96).
  Budget Funding: 10.0 M. ptas.
  Holder: Juan J. Navarro.

- **Grup Recerca Qualitat95** (1995–1997) (CIRIT GRQ–402/95).
  Budget Funding: 5.0 M. ptas.
  Holder: Mateo Valero.

- **Cooperación entre el Microkernel y las Aplicaciones para Explotar el Paralelismo en Sistemas Multiprocesadores** (1994–1997) (CICYT TIC–439/94).
  Budget Funding: 4.9 M. ptas.
  Holder: José I. Navarro.

- **Colaboración en la Financiación de las Actividades del CEPBA** (1996) (CIRIT).
  Budget Funding: 10.0 M. ptas.
  Holder: Mateo Valero.

- **Infraestructura de Recerca 95** (1995–1996) (CIRIT IN–95)).
  Budget Funding: 25.0 M. ptas.
  Holder: Mateo Valero.

- **Sistema Computador Masivamente Paralelo** (1994–1995) (CICYT IN–543/94).
  Budget Funding: 145.0 M. ptas.
  Holder: Mateo Valero.

- **Sistemas Operativos para Computadores Masivamente Paralelos** (1994–1995) (CICYT TIC–537/94).
  Budget Funding: 1.5 M. ptas.
  Holder: Jesús Labarta.

- **Infraestructura de Recerca 94** (1994–1995) (CIRIT IN–94).
  Budget Funding: 3.0 M. ptas.
  Holder: Juan J. Navarro.

- **Architecture and Compilers for Supercomputers** (1992–1995) (CICYT TIC–880/92).
  Budget Funding: 76.0 M. ptas.
  Holder: Mateo Valero.

- **IDENTIFITY Diseño Interactivo Mediante la Utilizazión de una Red de transputers en Fluidos** (1993–1994) (CICYT TIF–1057/93).
  Budget Funding: 8.9 M. ptas.
  Holder: Juan J. Navarro.

- **SHIPS Sistemas Paralelos de Supercomputación** (1993–1994) (CICYT TIC–1056/93).
  Budget Funding: 7.0 M. ptas.
  Holder: José M. Llabería.

- **Actualización Computadores CEPBA** (1993–1994) (CICYT TIC–1452/93).
  Budget Funding: 34.0 M. ptas.
  Holder: Mateo Valero.

- **Grups de Recerca de Qualitat–Computaciones Paralelas** (1992–1993) (CIRIT QUA–3003/93).
  Budget Funding: 8.0 M. ptas.
  Holder: Mateo Valero.

3.3 Design and Performance Evaluation of Broadband Integrated Communication Systems

Some of the topics covered by this research line are: Broadband Integrated Communication Networks: protocols, reference connection, signalling, operation and maintenance functions. Asynchronous Transfer Mode, Source traffic modelization for the new services (CBR, VBR). ATM switching: basic switching elements, multistage interconnection networks, analytic models. Performance of multiplexing and switching elements. Traffic Control and Network Resource Management for ATM BISDN: policing functions, connection admission control, priorities, cell spacing, cell delay variation, congestion control, Broadband access facilities: topologies, medium access protocols. ATM local area networks. Internetworking units: high speed networking, MAN, LAN, WAN, ATM internetworking.

This research field is organized in two research groups:

- Integrated Broadband Communication Systems and Applications (LR 33040610-01). Research team: Jordi Domingo–Pascual, Josep Solé–Pareta, German Santos, Teodor Jové, Josep L. Marzo, Ramon Fabregat, Joan Vila–Sallent, Sergio Sánchez and Xavier Masip.
- Traffic Management in ATM Networks (LR 33040610-02). Research team: Olga Casals, Jorge García, Josep M. Barceló and Fernando Cerdan.

3.3.1 Research Topics

Internetworking, and MAC protocols

- David Andrés, Joan Vila–Sallent, Jordi Domingo–Pascual, and Josep Solé–Pareta. Performance of Interconnecting FDDI Networks through ATM when Managing Video. In *5th International Conference on High Performance Networking (HPN'94)*, pp. 341–355, Grenoble (France), July 1994.
- X. Masdeu, Josep Solé–Pareta, and Jordi Domingo–Pascual. Comparison of DQDB +/- and DQDB IEEE 802.6 Protocols. In *Broadband Services, Systems and Networks*, pp. 1–12, Brighton (UK), November 1993.
- Josep Solé–Pareta, German Santos, and F. Noguera. Supporting Distance Learning Applications on Top of Current Public. In *11th International Symposium on Subscriber Loops Services*, pp. 68–74, Melbourne (Australia), February 1996.
- A. Espuña, L. Puigjaner, and German Santos. Adding Intermediate Storage to Noncontinuous Processes. In *Com-Chem'90*, pp. 145–152, Hague (The Netherlands), May 1990.

Traffic characterization in ATM Networks

- Joan Vila–Sallent, Josep Solé–Pareta, and Jordi Domingo–Pascual. Monitorization of Multiplexed ATM Video Sequences. In *5th International Workshop on Packet Video*, pp. 71–79, Berlin (Germany), March 1993.
- Josep Solé–Pareta and Jordi Domingo–Pascual. Burstiness Characterization of ATM Cell Streams. *Computer Networks and ISDN Systems*, vol. 11, no. 26, pp. 1351–1366, August 1994.
- Josep Solé–Pareta, Jordi Domingo–Pascual, and Jorge García. Modelling the Bursty Characteristics of ATM Cells Streams. In *1st International Conference on Integrated Broadband Services, Systems and Networks*, pp. 329–334, London (UK), September 1990.
- Josep Solé–Pareta, Jorge García, and Jordi Domingo–Pascual. Traffic Burstiness Influence on ATM Switching Behavior. In *4th International Conference on Data Communication Systems and their Applications*, pp. 133–148, Barcelona (Spain), June 1990.

Bandwidth Allocation in ATM Networks

- Ramon Fabregat, Josep L. Marzo, Josep Solé–Pareta, and Jordi Domingo–Pascual. CAC controlled services sharing a link with connectionless data services in an ATM network: a performance evaluation study. In *2nd International Conference on Integrated Broadband Services, Systems and Networks*, Brighton (UK), November 1993.

- Ramon Fabregat, Josep Solé–Pareta, Josep L. Marzo, and Jordi Domingo–Pascual. Bandwidth Allocation Based on Real Time Calculations Using Convolution. In *IEEE Global Telecommunications Conference & Exhibition*, pp. 788–793, (USA), December 1994.

- Josep L. Marzo, Ramon Fabregat, Jordi Domingo–Pascual, and Josep Solé–Pareta. Fast Calculation of the CAC Convolution Algorithm Using the Multinomial Distribution Function. In *10th UK Teletraffic Symposium on Performance Engineering in Telecommunications Networks*, pp. 23–26, London (UK), April 1993.

ATM switching and Fast Packet Switching

- Jordi Domingo–Pascual and Josep R. Freixenet. Arbitration Mechanisms for Non Uniform Traffic in Packet Swiyching Multiprocessor Interconnection Networks. In *ISMM International Conference on Mini and Microcomputers and their Applications*, pp. 112–115, Montreal (Canada), May 1990.

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Routing in ATM Networks

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- Joan Vila–Sallent and Josep Solé–Pareta. High Performance Distributed Computing over ATM Networks: A Survey of Strategies. In *2nd International Conference on Massively Parallel Computing Systems (MPCS'96)*, May 1996.

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- Josep Solé–Pareta and Joan Vila–Sallent. Network–Based Parallel Computing over ATM Using Improved SSCOP Protocol. *Computer Communications*, November 1996. Special issue on Recent Advances in Networking Technology, to appear.

Medium Access Control (MAX) Protocol

A MAC protocol used to concentrate ATM user traffic in a Passive Optical Network (PON) with a tree structure has been proposed implemented and evaluated (with analytical and simulation models and also through experiments) within the European research program RACE project R2024. The PON is used as access network in various european ATM National hosts.

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- Chris Blondia, Olga Casals, Jorge García, T. Toniatti, and L. Verri. Performance of Shared Medium Access Protocols for ATM Traffic Concentration. *European Transactions on Telecommunication and Related Technologies*, vol. 5, no. 2, pp. 219–226, March 1994.

- Fernando Cerdan, Olga Casals, Josep M. Barceló, and Jorge García. Protocolo de Control de Acceso al Medio para una Red de Acceso ATM. In *Cuartas Jornadas de I+D en Telecomunicaciones*, pp. 257–265, Madrid (Spain), November 1994.

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- Jorge García Olga Casals, and Chris Blondia. A Cell Based MAC Protocol with Traffic Shaping and a Global FIFO Strategy. In *RACE Open Workshop on Broadband Access.*, pp. 1–4, Nijmegen (The Netherlands), June 1993.

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The different space priority mechanisms proposed in ATM networks are evaluated with an analytical model, assuming bursty input traffic.

- Jorge García and Olga Casals. Priorities in ATM Networks. In *Advanced Research Workshop on Architecture and Performance Issues of High–Capacity Local and Metropolitan Networks*, pp. 1–15, Sofia–Antipolis (France), June 1990.

- Jorge García and Olga Casals. Performance Evaluation of Source Dependent Congestion Control Procedures in ATM. In *Singapore International Conference on Networks (SICON'91)*, pp. 178–182, Singapore (Malaysia), September 1991.

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- Jorge García and Olga Casals. Stochastic Models of Space Priority Mechanisms with Markovian Arrival Processes. *Annals of Operations Research*, no. 35, pp. 271–296, January 1992.

ATM Traffic Models

Characterization of ATM traffic using analytical models.

- Chris Blondia and Olga Casals. Traffic Profiles in ATM Networks. In *1st International ATM Traffic Expert Symposium*, pp. 1–21, Basilea (Switzerland), April 1995.
- Olga Casals. A Review of Voice, Data and Video Traffic Models for ATM. *European Transactions on Telecommunication and Related Technologies*, vol. 5, no. 2, pp. 139–154, March 1994.
- Chris Blondia and Olga Casals. Traffic Profiles in ATM Networks. In *Telecommunication Systems*, pp. 49–69, 1996.

Analysis of a statistical multiplexer

Performance evaluation of an ATM multiplexer with VBR sources using an analytical model.

- Chris Blondia and Olga Casals. Cell Loss Probabilities in a Statistical Multiplexer in an ATM Network. In *Messung, Modellierung und Bewertung Von Rechensystemen*, pp. 121–136, Munich (Germany), September 1991.
- Chris Blondia and Olga Casals. Statistical Multiplexing of VBR Sources in an ATM Network: A Matrix–Analytic Approach. In *Performance Aspects of ATM Networks*, Leidschendam, October 1991.
- Chris Blondia and Olga Casals. Performance Analysis of Statistical Multiplexing of VBR Sources. In *IEEE Infocom'92*, pp. 828–838, Florence (Italy), May 1992.
- Chris Blondia and Olga Casals. Statistical Multiplexing of VBR Sources: A Matrix–Analytic Approach. *Performance Evaluation*, vol. 1, no. 16, pp. 5–20, October 1992.

Cell Delay Variation (CDV) Analysis

Analytical model to evaluate the CDV introduced by statistical multiplexing in ATM networks.

- Jorge García and Olga Casals. Approximate Analysis of Statistical Multiplexing of VBR and Periodic Sources. In *IV International Meeting of Statistics in the Basque Country*, San Sebastian (Spain), August 1992.
- Jorge García and Olga Casals. Asymptotic Analysis of Statistical Multiplexing of Variable Bit Rate and Constant Bit Rate Sources. In *Modelling and Performance Evaluation of ATM Technology*, Martinique (France), January 1993.
- Jorge García and Olga Casals. A Discrete Time Queueing Model to Evaluate the Cell Delay Variation in an ATM Queueing Network. *Performance Evaluation*, vol. 21, no. 1, pp. 3–22, October 1994.

Worst Case Traffic (WCT) Sources

Models for the evaluation of WCT sources multiplexing.

- Jorge García, Josep M. Barceló, and Olga Casals. An Exact Model for the Multiplexing of Worst Case Traffic Sources. In *Conference on Performance of Computer Networks*, pp. 3–17, Istambul (Turkey), January 1996.
- Josep M. Barceló, Jorge García, and Olga Casals. Comparison of Models for the Multiplexing of Worst Case Traffic Sources. In *Premier Colloque sur la Gestion du Traffic*, pp. 41–48, Paris (France), December 1995.

Experiments on an ATM testbed

Description of the experiments performed with the ATM tesbed located in Basel (Switzerland) and discussion of the results obtained.

- Josep M. Barceló, Olga Casals, L. Jaussi, V. Nellas, and N. Mitrou. Results of Experiments on Resource Management Performed by Exploit WP 3.5 on the Exploit Testbed. In *ATM Hot Topics on Traffic and Performance*, pp. 1–10, Milan (Italy), June 1995.

- N. Mitrou, V. Nellas, A. Martínez, L. Jaussi, and Josep M. Barceló. First Results and Analysis of Traffic Experiments Performed by Exploit WP3.2 on the ETB. In *14th Exploit Traffic Workshop*, pp. 1–9, Basilea (Switzerland), September 1995.

- L. Jaussi, Josep M. Barceló, S. Louis, and Olga Casals. Experimental Evaluation of CDV Impact on ATM Resource Management. *European Transactions on Telecommunication and Related Technologies*, vol. 7, no. 5, September 1996.

ABT service

Performance evaluation of the Fast Reservation Protocol designed for ABT.

- Llorenç Cerdà, Jorge García, and Olga Casals. A Study of the Fairness of the Fast Reservation Protocol. In *3rd Workshop on Performance Modelling and Evaluation of ATM Networks*, pp. 1–11, Ilkley (United Kingdom), July 1995.

Policing function for ABR service category

Improvements and performance study of the Dynamic Generic Cell Rate Algorithm (DGCRA) proposed for ABR.

- Llorenç Cerdà, Jorge García, and Olga Casals. A Study of the Fairness of the Fast Reservation Protocol. In *3rd Workshop on Performance Modelling and Evaluation of ATM Networks*, pp. 1–11, Ilkley (United Kingdom), July 1995.

- Llorenç Cerdà and Olga Casals. Improvements and Performance Study of the Conformance Definition for the ABR Service in ATM Networks. In *ITC Specialists Seminar on Control in Communications*, pp. 323–334, (Sweden), 1996.

ABR Flow Control

Performance analysis of the ABR congestion control mechanism.

- Chris Blondia and Olga Casals. Analysis of Explicit Rate Congestion Control in ATM Networks. In *Australian Telecommunication Networks & Applications Conference*, Melbourne (Australia), December 1996.

- Chris Blondia and Olga Casals. Throughput Analysis of the Explicit Rate Congestion Control Mechanism in ATM Networks. In *ITC Specialists Seminar on Control in Communications*, pp. 89–101, (Sweden), 1996.

3.3.2 R+D Projects and Agreements

- **Multimedia Information Window for National Hosts (InfoWin AC113)**
  Project Objetive: The strategic goal is the creation of the ACTS Information Window, that allows the ACTS projects to see the world surrounding them, and, at the same time, provides to the world a view of all aspects of the work in ACTS. Projects within the ACTS Program will "see and be seen" by a world–wide community of peer researchers and developers as

well as prospective users of the service which are the subject of the projects' works. The INFOWIN mechanisms will also be used for ACTS internal information exchange.
Department contribution: WP1 (1mm): Regional Representative functions. Gather information from ACTS Program managers, projects and from the Global Communications world. WP3 (4mm): Promotion of the InfoWin products, understanding user needs, monitoring local/regional activities and production of News Clips.
Project length: March, 1996 – February, 1999.
Funding body: EU (ACTS). Subcontracted by Telefónica Investigación y Desarrollo.
Holder: Jordi Domingo–Pascual.
Partners: University of Stuttgart (D), Analysys Ltd. (UK), DeTeBerkom GmbH (D), CP2i (F), CSELT (I), NCSR Demokritos (GR), Telefónica Investigación y Desarrollo (E), Burger Breedband Net vzw (B), Bureau for International Research and Technology Cooperation (A), INRIA (F), KTH (S), Landsmidstvdin (ICE), uni C (DK), Telenor Research (N), The Open University (UK), Femuniversitaet Hagen Gesamthochshule (D), IENM (A), Fraunhofer IGD (D), Intracom Hellenic Telecommunications Electronics Ind. (GR), Ascom Tech Ltd. (CH).

- **Platform for Engineering Research and Trials**
  Project length: October, 1995 – May, 1997.
  Funding body: CEC/ACTS AC094.
  Budget Funding: 16.9 M. ptas.
  Holder: Olga Casals.

- **Broadband Acces Facilities**
  Department contribution: Bandwidth management: Connection Acceptance Control, Usage Parameter Control, Medium Access Control Protocol, Performance Evaluation of the protocol, Specification of experiments on the demonstrator.
  Project length: January, 1992 – June, 1995.
  Funding body: CEC/RACE 2024.
  Budget Funding: 32.4 M. ptas.
  Holder: Olga Casals.
  Partners: AT&T Network Systems Nederland B.V., ASCOM TECH AG., Telefónica de España, Deutsche Bundespost Telekom Forschungsinstitut, Dowty Communications Limited, Maz Mikroelektric Anwenkungszentrum Hamburg Gmgh, Italtel Societa Italiana Telecomunicazioni S.P.A., Queen Mary and Westfield College, National Technical Univesity of Athens, Centro Studi e Laboratori Telecomunicazioni S.P.A., The University of Stuttgart, UPC, Universiteit Van Nijmegen, Technische Universitat Hamburg - Harburg, Koninklijke Ptt Nederland N.V..

- **Exploitation of an ATM Technology Test-Bed for Broadband Experiments and Applications**
  Department contribution: Specify and perform experiments on network resource management.
  Project length: January, 1992 – December, 1995.
  Funding body: CEC/RACE 2061.
  Budget Funding: 31.1 M. ptas.
  Holder: Olga Casals.
  Partners: Association Swiss Ptt/Ascom Tech, Ascom Tech Ltd., Bell Telephone Mfg Co., Standard Elektrik Lorenz Ag-Sel Alcatel, Alcatel Standard Eléctrica, S.A., Alcatel Telecom Norway AS, British Telecommunications Plc., Centro de Estudios de Telecommunicacoes, DBP Telekom Forschungsinstitut, Inst Engenharia de Sist. de Computadores, Jydsk Telfon, Kjobenhavns Telefon Aktieselskab, Mikroelektronik Anwendungszentrum Gmbh, Nokia Corporation, Norwegian Telecom Research, National Technical University of Athens, Laboratoires d'Electronique Philips, Philips Kommunikations Industrie AG, Queen Mary & Westfield College, Koninklijke Ptt Nederland Nv Ptt Research, Regie des Telegraphes et des

Telephones, Telefónica de España S.A., Universiteit Gent, University of Nijmegen, UPC, University of Stuttgart.

- **Network Termination Type 1 at 622 Mbps**
  Department contribution: Functional specification of the equipment according with international standards for Broadband ISDN, ATM and SDH. Definition of the test equipment procedures and test integration in the PLANBA network.
  Project length: July, 1992 – July, 1994.
  Funding body: TIDSA PLANBA-C1751: TR1-622.
  Budget Funding: M. ptas.
  Holder: Jordi Domingo–Pascual.
  Partners: Telefónica Investigación y Desarrollo S.A. (TIDSA).

- **Realización de un Trabajo de Investigación y Desarrollo para el Proyecto TR1.**
  Project length: July, 1992 – December, 1994.
  Funding body: SITRE PLANBA–C 1926.
  Holder: Jordi Domingo–Pascual.

3.3.3 Grants

- **Plataforma ATM para la Investigación y la Realización de Pruebas EXPERT** (1996–1999) (CICYT TIC–2024/96).
  Budget Funding: 4.4 M. ptas.
  Holder: Olga Casals.

- **Diseño y Evaluación de Redes de Banda Ancha** (1994–1997) (CICYT TIC–1512/94).
  Budget Funding: 2.8 M. ptas.
  Holder: Olga Casals.

- **Supervisió de Qualitat dels Serveis Telemàtics Proveïts per a la Xarxa Acadèmica de Banda Ampla en l'Accés de la UPC** (1996–1997) (CICYT TEL–2509/96).
  Budget Funding: 10.5 M. ptas.
  Holder: Josep Solé–Pareta.

- **Servicios de Banda Ancha Especializados y de Formación del Centro de Comunicaciones** (1996–1997) (CICYT TEL–1961/96).
  Budget Funding: 16.3 M. ptas.
  Holder: Jordi Domingo–Pascual.

- **Infraestructura de Recerca 94. Laboratori de proves d'equips i de comunicacions en banda ampla** (1994–1995) (CICYT IN–667/94).
  Budget Funding: 10.0 M. ptas.
  Holder: Jordi Domingo–Pascual.

- **Adquisición de una Réplica del Equipo After (Adaptador Flexible de Terminales)** (1995–1996) (CICYT TIC–1405/95).
  Budget Funding: 7.1 M. ptas.
  Holder: Josep Solé–Pareta.

- **Grup Recerca Qualitat95** (1995–1996) (CIRIT GRQ–464/95).
  Budget Funding: 5.0 M. ptas.
  Holder: Olga Casals.

- **Planba–Comunicaciones integradas de Banda Ancha** (1992–1996) (CICYT TIC–1289/92).
  Budget Funding: 7.7 M. ptas.
  Holder: Jordi Domingo–Pascual.

- **ABR (Available Bit Rate) and Local Area Networks with ATM Technology** (1995–1998) (CICYT TIC–982/95).
  Budget Funding: 9.2 M. ptas.
  Holder: Olga Casals.

- **Grup Recerca Qualitat93–Disseny i Avaluació de sistemes integrats en banda ampla** (1992–1993) (CIRIT GRQ–3008/93).
  Budget Funding: 6.5 M. ptas.
  Holder: Olga Casals.

3.4 Distributed Systems Architecture

The general goal of this research field is the study of the interconnection methods for distributed applications. This interconnection is confronted from the point of view of the application, i.e. like a set of services that are necessary to design in order to facilitate the correct operation of the application. These services are conceived starting from a general architecture, that is particularized into concrete solutions for each case, according to the requirements of the application's users.

In summary we could say that in this research line all aspects relative to the distributed systems and their applications are studied, focusing on Telematic Applications.

The covered topics by the internal and external projects in which we are participating, or in which we have been involved, are:

- Distributed applications and systems
- Internet security
- Electronic Commerce Applications: EDIFACT, Brokerage Services, Secure Transactions, etc.
- Open Documents Architecture (ODA) and Open Document Interchange Format (ODIF)
- Open Systems (Internet, ISO/OSI): WWW engines, Java
- Electronic Certificates and Certification Authorities (X.509)
- Computer Supported Cooperative Group (CSCW) and Groupware
- Specification and implementation of protocols for distributed architectures
- International standards development (ISO, EWOS, AENOR, IFIP)
- Document Communication (Joint Synchronous Edity, Sequential Document Production, etc.)
- Multimedia publishing applications

3.4.1 Research Subfields

Group Communication

Study how distributed systems could give support to collaborative work carried out by a potentially large number of people, computers networking together, forming a potentially large and widespread community, many times a region of Internet. In other words, the interfaces between components of a distributed system and people are our target topic.

Collaborative services and telematic applications for specific areas of application (education, research, cooperation networks, civic networks) have been studied, designed and validated in a multidisciplinary approach with contributions from education and social sciences as well as computing and networking.

Large scale cooperative networks are subject of particular interest. Services and mechanisms for scaling up and enabling the evolution of a global networking infrastructure such as:

- Federation of autonomous heterogeneous and distributed sources of information,
- Notification and coordination for people, resources or services,
- Optimizing the access to information by distribution and replication,
- Architectures for large scale distributed networks of services and people,
- Services and applications for particular communities.

Pilots in several application areas have been set up: in education with the I*earn educational network, Pangea on cooperation networks, Aleph on large scale networks, Bcnet on civic networks, Intermed on regional networks, Epitelio on social integration networks, among others.

Several workshops and conferences are organized and promoted such as Inet–Cat, Inter–Med, etc. to discuss and disseminate the results of our research with other research groups and the society.

Basic research has been partially funded mainly by several CICYT (ES), COST 14 (EC), and ESPRIT Basic Research (EC) actions.

Applied research has developed in the framework of the above and other projects such as CACTUS (EC), EPITELIO (EC), MSC (EC), among others.

Researchers: Leandro Navarro (Leader), Miquel Colomer, Joan M. Marqués, Claudio E. Righetti, Gerard Rodríguez, María Clara Rozo, Mildred Sarmiento, Artur Serra and Josep Turró.

Distributed Systems Security

Specification and development of Electronic Commerce Applications based on EDIFACT. Development of EDIFACT security messages and others.

Study of the security control mechanisms in Internet, computer networks and distributed systems in general.

The group holds the Spanish CERT (Computer Emergency Response Team) to coordinate the Internet security incidents.

Security policies choices have been analyzed, and specific security policies for security targets have been defined. Security products are tested and evaluated.

Tools for secure authentication and certification have been developed and an infrastructure for public key certification (Certification Authority, CA) has been set up in coordination with other CA in Europe.

A version of the secure transport layer has also been implemented, according to the ISO 10736 specification: Transport Layer Security Protocol.

Now, we are working to introduce security in WWW, Electronic Commerce and EDI applications (Electronic Data Interchange), using electronic signatures and certification authorities (CA).

Researchers: Manel Medina (Leader), Jordi Buch, Oscar Ciurana, Juan C. Cruellas, Isabel Gallego, Jordi Iñigo, Francisco Jordán, Enric Peig, Xavier Perramon and Montse Rubia.

Secure Infrastructures: Authentication and certification

This topic includes works on secure infrastructures based on authentication and certification. In the listed papers, it is discussed and formalized solutions to the problem of authentication in multi–entity based environments using key distribution centers as the basis for authenticating such entities. On the other hand, it is also presented and formalized general certification architectures in order to provide a global authentication system based on certification.

- Francisco Jordán and Manel Medina. Improving the Security Infrastructure without Exteding the X.509 Base–Certificate. In *6th Joint European Networking Conference*, pp. 313.3–313.7, Tel Aviv (Israel), May 1995.

- Francisco Jordán, Manel Medina, Juan C. Cruellas, and Isabel Gallego. A Step Ahead in the Directory Authentication Framework. In *IFIP International Working Conference in Upper Layer Protocols, Architectures and Applications (ULPAA'94)*, pp. 89–106, Barcelona (Spain), June 1994.

- Francisco Jordán and Manel Medina. Secure Multicast Communications using a Key Distribution Center. In *Information Networks and Data Communication International Conference (INDC'94)*, pp. 367–380, Funchal, Madeira Island (Portugal), May 1994.

- Francisco Jordán and Manel Medina. A Complete Secure Transport Service in the Internet. In *Internet Society Symposium on Network and Distributed System Security*, pp. 67–76, San Diego (USA), February 1994.

- Francisco Jordán. *Infraestructura de Seguridad en Aplicaciones y Sistemas Distribuidos.* PhD thesis, Universitat Politècnica de Catalunya (UPC), October 1995. Advisor Manel Medina.

EDI Security

Activities on this topic focus in security services provision in UN/EDIFACT messages. A member of the groupo is also an active mnember of the UN/EDIFACT Security Joint Working Group (SJWG). This group is in charge of the standardisation of UN/EDIFACT structures and messages to implant security services in UN/EDIFACT systems. Relevant aspects of EDI security are public key infrastructure in EDIFACT, certification, Interactive EDI security, etc. Our most important contributions are:

- Juan C. Cruellas. Attribute Certificates and Certificate Extensions, 1995. SJWG internal working document.

- Juan C. Cruellas and Isabel Gallego. Delegation Protocols in Distributed Systems, 1995. SJWG internal working document.

- Juan C. Cruellas and Montse Rubia. Examples of the use of AUTACK message, 1996. Annex of the EDIFACT CD-9735 part 6 to be proposed as ISO CD.

- Juan C. Cruellas and Montse Rubia. EDI Security Structures and X.500 Use, 1996. Contribution to documents on guidance to use of X.500 directories by EDI users. EWOS/EG.

Interoperability

The existence of several proposals for public key infraestructures raise the need for studies on interoperability. Interest of the group for this topic has resulted in the activities developed in DEDICA project, devoted to facilitate interoperability between X.509 and UN/EDIFACT public key infrastructures. Among other the following items are of interest:

- Certificates. Semantical and syntactical studies have been carried out in X.509 and UN/EDIFACT certificates in order to determine the contained information in each one. Rules to produce a certificate of one type from a certificate of the other type with similar semantic information have been produced.

- Certificates revocation management in X.509 and UN/EDIFACT world.

- Security policies specification.

Our most important contributions are:

- Fritz Bauspieß, Juan C. Cruellas, and Montse Rubia. Directory based EDI Certificate Access and Management. In *Digitale Signaturen*, Darmstadt (Germany), September 1996.

- Montse Rubia, Juan C. Cruellas, Manel Medina, and Isabel Gallego. Naming conversion rules specification, 1996. Deliverable of DEDICA project.

- Montse Rubia, Juan C. Cruellas, Manel Medina, and Isabel Gallego. Final Specifications of Certificates Conversion Rules, 1996. Deliverable of DEDICA project.

Multimedia Document Architectures and Distribution

This research line is devoted to different topics around multimedia applications, focusing on the architecture of the multimedia information (mainly multimedia documents) and on applications allowing the distribution, remote handling and management of multimedia information. Co–operative document handling is also considered. These distributed applications are based on many different network environments, like those provided by OSI and Internet. How to apply multimedia document characteristics to the network is another topic.

Two different types of activities are being made:

- Standardization work: The group is actively working on the specification of different International Standards through participation in and contribution to ISO/IEC JTC1/SC18, ITU–T SG8, EWOS EG SMMI and ETSI TE2 (some of these Committees are currently under re–organization). The developed standards include ISO/IEC 8613 (ODA; Open Document Architecture), ISO/IEC ISP 15121 (AODs, Interactive Document Manipulation profiles), ISO/IEC ISP 12069 (ADFs, Document Filing and Retrieval profiles), ITU-T T.190 (Co–operative Document Handling – Framework and basic services), etc.

- Research and Development projects: The group has participated or is participating in several European R&D projects, mainly in the ESPRIT and ACTS programs, developing telematic applications in the field of distributed multimedia systems.

The work being done can be classified in the following sub–lines:

- Multimedia document architectures: It includes the development of specifications and software for the representation of multimedia documents for its interchange in open environments.

- Distributed multimedia applications: It includes the development of specifications and software for distributed multimedia applications, such as remote document manipulation, document filing and retrieval, joint synchronous editing, sequential document production, etc.

- Electronic mail applications: It includes the development of electronic mail extensions (such as message storage and intelligent mailboxes) and electronic mail based applications (like automatic document translation).

- Others: Some members of the group are also working on other related fields.

Researchers: Jaime Delgado(Leader), José J. Acebrón, Juan C. Cruellas, Francisco Jordán, Ramon Martí, José M. Martínez, Ramon Mercé, Antonio Paradell, Xavier Perramon, José Polo.

Mutimedia Document Architectures

It includes the development of specifications and software for the representation of multimedia documents for its interchange in open environments. The main results of our work are:

- Standardization work. The second version of the ISO/IEC 8613 (ODA: Open Document Architecture) standar was published in 1994. Our group edited two of the different parts of the standar, and actively contributed to the work of corresponding ISO/IEC working group (ISO/IEC JTC1/SC18/WG3, working in collaboration wtrih ITU–T SG8).

  In addition, two new parts of the ODA Satandard/Recommendation, published in 1995 and 1996, Abstract Interface for the Manipulation of ODA Documents, and Identification of Document Fragments, were edited by team members.

  An ETG (EWOS Technical Guide) on how to include Application Specific Information, like STEP or EDIFACT, into ODA documents was developed under the ledearship of our team. It was approved and published in 1995.

  Also effort was put on the development of an ETG on Specifications for the Definitions of Layout Consistency in ODA documents.

- Research and Development Projects. The ESPRIT FODATEC project (Feasibility demonstration of ODA for TEChnical documents) is an example of R&D work in this field.

The most relevant papers in this topic are:

- José J. Acebrón and Jaime Delgado. Handling and Interchange of Structured Multimedia Documents Containing Application Specific Information. In *6th Joint European Networking Conference*, pp. 1–8, Tel Aviv (Israel), May 1995.
- Jaime Delgado and Xavier Perramon. ODA Converters and Document Application Profiles. In *Message Handling Systems and Application Layer Communications Protocols*, pp. 329–342. North–Holland, 1991.
- Jaime Delgado, José J. Acebrón, Ramon Martí, and Xavier Perramon. Contribution to the Topic Generic Abstract Interface for the Manipulation of Documents, March 1996. EWOS/EG/SMMI 96/085.
- José J. Acebrón and Jaime Delgado. A Modular Design for the Next Generation of ODA Profiles, December 1994. EWOS/EG/SMMI 95/005.
- José J. Acebrón and Jaime Delgado. Including ASI into ODA documents: Extensions required in FOD026, January 1994. EWOS/EG/ODA 94/014.

Distributed Mutimedia Applications

It includes the development of specifications and software for distributed multimedia applications, such as remote document manipulation, document filing and retrieval, joint synchronous editing sequential document production, etc. The main results of our work are:

- Standardization work. Active participation (being also editors) in the development of the profiles for Interactive Document Manipulation, AOD profiles (ISO/IEC ISP 15121), including the original idea, the taxonomy of profiles, and the profiles themselves.

  Similar situation with respect to the profiles for Document Filing and Retrieval, ADF profiles (ISO/IEC ISP 12069). Both set of profiles were developed through participation in EWOS.

  Specification, in collaboration with ETSI TE2, and for ITU-T SG8, of the Recommendation T-190 on Cooperative Document Handling Framework and basic services.

  Participation in the development of an EWOS ETG on Multimedia Medical Data Interchange.

- Research and Development Projects. The work being done in the ACTS MULTIMEDIATOR project (Multimedia Publishing Brokerage Service), leaded by one member of the team, is a good example of distributed multimedia applications.

The most relevant papers in this topic are:

- Jaime Delgado and José J. Acebrón. Design of Multimedia Document Communication Services over Multipoint Protocols. In *Protocols for Multimedia Systems*, pp. 63–80, October 1996.
- José J. Acebrón and Jaime Delgado. Interchange of Multimedia Documents Containing External Information. In *International Networking Conference (INET'95)*, pp. 25–33, Honolulu (USA), June 1995.
- José J. Acebrón and Jaime Delgado. Design of a Distributed Document System based on ODA: DODS. In *IFIP International Working Conference in Upper Layer Protocols, Architectures and Applications (ULPAA'94)*, pp. 209–219, Barcelona (Spain), June 1994.
- Jaime Delgado. Clarification of ADF2 Profiles, May 1994. EWOS/EG/ODA 94/098.
- Jaime Delgado and José J. Acebrón. Proposals for profiling ITU–T T.120 Recommendations, March 1996. EWOS/EG/SMMI 96/070.

Electronic Mail Applications

It includes the development of electronic mail extensions (such as message storage and intelligent mailboxes) and electronic mail bsed applications (like automatic document translation).

The main results of the work in this sub–line come from some ESPRIT projects like TWB–II (Translator's Workbench II), TWD abd CACTUS (CARLOS ("Communication Architecture for Layered Open Systems") Addition for Clustered Terminal User Agents).

The most relevant papers in this topic are:

- Jaime Delgado and Manel Medina. Group Communication Mailbox Server Accessible through a Standard Mailbox Client. In *Message Handling Systems and Application Layer Communications Protocols*, pp. 177–189. North–Holland, 1991.

- Jaime Delgado, Francisco Jordán, and Manel Medina. X.400 Access to Machine Translation Systems. In *Message Handling Systems and Application Layer Communications Protocols*, pp. 317–327. North–Holland, 1991.

- Jaime Delgado and Manel Medina. Use of the Abstract Service Definition Convention for Distributed Information Processing Systems Specification. In *Message Handling Systems and Distributed Applications*, pp. 217–231. North–Holland, 1989.

- Jaime Delgado, Manel Medina, Francisco Jordán, and Leandro Navarro. A User Interface for Distributed Applications. In *ESPRIT'88 Putting the Technology to Use*, pp. 1699–1710. North–Holland, 1988.

- Jaime Delgado, Manel Medina, B. Butscher, and M. Tschichholz. Storage Agents in Message Handling Systems. In *Office Systems: Methods and Tools*, pp. 97–113. North–Holland, 1987.

3.4.2 R+D Projects and Agreements

- **Directory Based Edi Certificate Access and Management (DEDICA)**
  Department contribution: UPC is in charge of the technical management of the project. It is also strongly involved in the specification and development phase of the project.
  Project length: April, 1996 – March, 1998.
  Funding body: CEC/TELEMATICS TE2005.
  Budget Funding: 16.0 M. ptas.
  Holder: Manel Medina.
  Partners: Teleport Paris, Alcatel Business, Eritel, Finsiel Consulenze e Applicazioni Informatiche, INTRASOFT, SSE.

- **Multi–Site Computing (MSC)**
  Project length: September, 1996 – March, 1998.
  Funding body: CEC/ESPRIT 22508.
  Budget Funding: 51.1 M. ptas.
  Holder: Leandro Navarro.
  Partners: Espais Telematics, S.L..

- **Epitelio Network-Excluded People Integration by the Use of Telematic Innovative Opportunities (EPITELIO–NETWORK)**
  Project length: January, 1996 – July, 1997.
  Funding body: CEC/TELEMATICS UR1009.
  Budget Funding: 10.7 M. ptas.
  Holder: Leandro Navarro.
  Partners: IEPALA, GREEN NET Educational Trust, ECTF, SODEPAZ, EUSKALNET, PFD, Manchester Metropolitan University, Trans European Rural Network (TERN), PANGEA, ENAIP, UPC.

- **Interworking Public Key Infraestructure por Europe (ICE–TEL)**
  Project length: January, 1996 – December, 1997.
  Funding body: CEC/TELEMATICS C1005.
  Budget Funding: 10.5 M. ptas.
  Holder: Manel Medina.
  Partners: GMD, COST, UNI-C, FCCN, FCR, Institute of Cibernetics, INESC, INTRASOFT, IC, IJS, POLITO, SSE, Technischen Universitaett Graz, UNINETT, University College London, SALFORD.

- **Multimedia Publishing Brokerage Service (MULTIMEDIATOR)**
  Department contribution: Implementation of the distributed service DFR (Document Filing and Retrieval). Contribution to standardization and to the general architecture.
  Project length: September, 1995 – August, 1997.
  Funding body: CEC ACTS AC096.
  Budget Funding: 22.0 M. ptas.
  Holder: Jaime Delgado.
  Partners: LOGIC CONTROL, SARITEL, BINTEC, MEDIA TRANSFER, DIACOMA, ARTS VIDEO, FCR, A PTT, TID, CSELT, MARI, COSI, DAC (UPC).

- **EDI Trusted Thirds**
  Project length: July, 1994 – July, 1995.
  Funding body: CEC/TEDIS 56621.
  Budget Funding: 11.0 M. ptas.
  Holder: Manel Medina.
  Partners: Bull, Expercom, Cryptomathic, Philips, R3 Security, Siemens Nixdorf, DAC (UPC Coordinator).

- **Computational Mechanisms of Interaction in Cooperative Work**
  Department contribution: We participe in three chief areas: 1.- The representation of the organization context, the study of boundaries and the interconnection of organizations. 2.- The notations and description techniques to represent the basic mechanisms of interaction that drive group activities. 3.- The object infrastructure and services supporting group interactions, laying on standarization work by ODP and OMG.
  Project length: September, 1992 – August, 1995.
  Funding body: CEC/ESPRIT 6225.
  Budget Funding: 22.5 M. ptas.
  Holder: Leandro Navarro.
  Partners: University of Amsterdam, GMD, University of Lancaster, University of Manchester, University of Milan, University of Nottingham, National Laboratory of RISOE and SICS.

- **Security Administration and Manegement in EDI**
  Project length: January, 1994 – December, 1994.
  Funding body: CEC/TEDIS 56533.
  Budget Funding: 3.0 M. ptas.
  Holder: Manel Medina.
  Partners: DAC (UPC Associated), Cryptomathic, Philips, R3 Security.

- **Password Value Project**
  Department contribution: Selected as the pilot site for Spain.
  Project length: September, 1993 – November, 1994.
  Funding body: CEC – VALUE Program.
  Holder: Francisco Jordán.
  Partners: GMD, INRIA, UCL.

- **Translator's Workbench**
  Department contribution: In TWB we developed a remote access to a machine translation system using X.400, several ODA converters for different word processors, and an access module to a remote terminological database. Our work in TWB-II is related to the distribution and networking of translation tools developed in the project. Furthermore, new ODA converters (for WordPerfect word processor) are being developed.
  Project length: April, 1992 – September, 1994.
  Funding body: CEC/ESPRIT P6005.
  Budget Funding: 17.9 M. ptas.
  Holder: Jaime Delgado.
  Partners: TA-Triumph-Adler Olivetti (coordinator), Cap Debis Systemhaus Ksp Gmbh, SNI, Siemens-Nixdord Information Systeme Ag, Siemens-Nixdord Sistemas de Información S.A., L-Cube Information Systems, S.A., University of Surrey, UPC.

- **Towards Secure OSI (COST–225)**
  Department contribution: Several documents containing, among others, the specification of a certification infraestructure for Europe, a secure transport protocol mechanism for multi-entity communications, implementation of TLSP (Transport Layer Secure Protocol).
  Project length: July, 1991 – August, 1994.
  Funding body: CEC COST 225.
  Holder: Manel Medina and Francisco Jordán.
  Partners: Representation of EU Countries.

- **Diversos Serveis dins del Marc del Projecte de la Xarxa Telemàtica Educativa de Catalunya (XTEC)**
  Project length: September, 1993 – December, 1993.
  Funding body: PROGRA. INFORMATI. EDUC. (GTAT).
  Budget Funding: 7.6 M. ptas.
  Holder: Leandro Navarro.

- **Cosine P8 Pilot Project**
  Department contribution: Selected as the pilot site for Spain.
  Project length: October, 1992 – June, 1993.
  Funding body: CEC – RARE – COSINE.
  Holder: Francisco Jordán.
  Partners: Baltimore Technologies (coordinator), UPC, Trinity College Dublin, GMD Darmstadt.

- **Feasibility Demonstration of Oda Technical Documents**
  Department contribution: Development of tools for handling documents based on the ODA (Open Document Architecture) standard (ISO 8613), including converters between FrameMaker word processor and ODA. Development of communication tools, including remote access to ODA documents based on X.400 and interactive communication. Contribution to ODA standardization in ISO and EWOS.
  Project length: January, 1991 – December, 1993.
  Funding body: CEC/ESPRIT EP5402.
  Budget Funding: 22.1 M. ptas.
  Holder: Jaime Delgado.
  Partners: Bureau Van Dijk (coordinator), Caption and UPC.

3.4.3 Grants

- **Interworking Public Key Certification Infrastructure for Europe (ICE–TEL)** (1996–1998) (CICYT TEL–1626/96).
  Budget Funding: 4.6 M. ptas.
  Holder: Manel Medina.

- **Intercambio Electrónico Seguro de Documentos Multimedia** (1995–1998) (CICYT TIC–903/95).
  Budget Funding: 18.8 M. ptas.
  Holder: Manel Medina.

- **Preparación Propuesta "Applied Telematics MICE"** (1995–1996) (CICYT TIC–1364/95).
  Budget Funding: 0.3 M. ptas.
  Holder: Manel Medina.

- **Directory based EDI Certificate Access and Management (DEDICA)** (1996–1997) (CICYT TEL–1644/96).
  Budget Funding: 5.8 M. ptas.
  Holder: Manel Medina.

- **Grup Recerca Qualitat95** (1995–1997) (CIRIT GRC–296/95)).
  Budget Funding: 1.5 M. ptas.
  Holder: Manel Medina.

- **Gestión y Administración de la Seguridad en Edi** (1995–1996) (CICYT TIC–1503/94).
  Budget Funding: 2.0 M. ptas.
  Holder: Manel Medina.

- **COMIC** (1993–1996) (CICYT TIC–1486/92).
  Budget Funding: 3.8 M. ptas.
  Holder: Leandro Navarro.

- **FODATEC (Demostración de Viabilidad de Oda para Documentos Técnicos)** (1993–1996) (CICYT TIC–1487/92).
  Budget Funding: 8.0 M. ptas.
  Holder: Jaime Delgado.

3.5 VLSI Systems Design

The research activities carried out in this area cover different aspects of the design, synthesis, verification and test of VLSI systems. A special emphasis is devoted to using formal methods to develop CAD tools for these tasks.

The current efforts are focused to the following topics: asynchronous circuits, low power design, high-level synthesis and models of concurrency.

3.5.1 Research Subfields

Synthesis, Formal Verification, and Test of Asynchronous Systems

During these last few years, asynchronous circuits have gained interest due to their promising advantages, such as local synchronization, elimination of the clock skew problem, faster and less power-consuming circuits, and high degree of modularity. However, the concurrent nature of asynchronous circuits makes them difficult to design because all transitions must be taken into account and hazards (voltage glitches) avoided. In addition, their usually complex structure also increases the difficulty of circuit verification and test.

Synthesis

Circuit synthesis can be divided into *high level* and *logic* synthesis. The former is devoted to obtaining a circuit description by mapping high level objects, e.g. operations and variables, into register transfer components, e.g. functional, storage and interconnection units. Given a low level behavioral description of a circuit, the latter obtains a set of equations that must be mapped onto a set of library gates. This mapping onto library gates, called *technology mapping*, must be carefully done regarding that certain properties still hold when the above equations are build by joining several smaller functions. Logic synthesis can be attacked from either a *state-based* or a *structural* point of view. State-based approaches may obtain more compact results, but are limited to small circuits, unless symbolic techniques are used. Structural methods may obtain sub-optimal solutions, but are able to synthesize much larger circuits.

Formal Verification

Formal verification consists in determining whether or not a circuit satisfies its specification. The specification can be some formalism that clearly and unambiguously describes the circuit behavior, whereas the circuit description usually characterizes the circuit at a lower level, e.g. a netlist of gates. Formal verification must assure that in any reachable circuit state the specification is not violated. Asynchronous circuits may have a huge number of reachable states, thus the problem of formal verification has been faced by using symbolic encoding and manipulation techniques. In addition, by using hierarchical approaches verification can be made even more efficiently.

Test

Test of asynchronous circuits is still a very open field. Most studies have been directed to theoretical results proving that they are *self-checking* in normal mode operation, whereas only few approaches are able to provide a set of test patterns. At the moment our group is working on novel Automatic Test Pattern Generation algorithms that will allow testing asynchronous circuits in commercial testing environments.

- Jordi Cortadella and Rosa M. Badia. An asynchronous architecture model for behavioral synthesis. In *Proc. European Conference on Design Automation (EDAC)*, pp. 307–311, Brussels, March 1992.

- Jordi Cortadella, Rosa M. Badia, Enric Pastor, and Abelardo Pardo. Achilles: A High-Level Synthesis System for Asynchronous Circuits. In *Handouts of the 6th. ACM/IEEE International Workshop on High-Level Synthesis*, pp. 87–94, Dana Point Resort, USA, November 1992.

- Rosa M. Badia and Jordi Cortadella. High-Level Synthesis of Asynchronous Systems: Scheduling and Process Synchronization. In *Proc. European Conference on Design Automation (EDAC)*, pp. 70–74, Paris, February 1993.

- Rosa M. Badia and Jordi Cortadella. GLASS: a Graph-theoretical Approach for Global Binding. *International Conference on Mini and Microcomputers and their Applications*, vol. 38, no. 1-5, pp. 775–782, September 1993.

- Enric Pastor and Jordi Cortadella. An Efficient Unique State Coding Algorithm for Signal Transition Graphs. In *Proc. of the IEEE International Conference on Computer Design*, pp. 174–177, Cambridge, USA, October 1993.

- Enric Pastor and Jordi Cortadella. Polynomial Algorithms for the Synthesis of Hazard-free Circuits from Signal Transition Graphs. In *Proc. of the IEEE/ACM International Conference on Computer Aided Design*, pp. 250–254, Santa Clara, USA, November 1993. IEEE Computer Society Press.

- Jordi Cortadella, Alexandre Yakovlev, Luciano Lavagno, and Peter Vanbekbergen. Designing asynchronous circuits from behavioural specifications with internal conflicts. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, Utah, November 1994.

- Enric Pastor, Jordi Cortadella, and Oriol Roig. A New Look at the Conditions for the Synthesis of Speed-independent Circuits. In *Proc. Fifth Great Lakes Symposium on VLSI*, pp. 230–235, Buffalo, May 1995.

- Alex Kondratyev, Jordi Cortadella, Michael Kishinevsky, Enric Pastor, Oriol Roig, and Alexandre Yakovlev. Checking Signal Transition Graph implementability by symbolic BDD traversal. In *Proc. European Design and Test Conference (EDAC-ETC-EuroASIC)*, pp. 325–332, Paris, March 1995.

- Oriol Roig, Jordi Cortadella, and Enric Pastor. Verification of asynchronous circuits by BDD-based model checking of Petri nets. In *16th International Conference on Application and Theory of Petri Nets*, volume 935 of *Lecture Notes in Computer Science*, pp. 374–391, Torino, June 1995. Springer-Verlag.

- Oriol Roig, Jordi Cortadella, and Enric Pastor. Hierarchical Gate-Level Verification of Speed-Independent Circuits. In *Proc. of the 2nd Working Conference on Asynchronous Design Methodologies*, pp. 128–137, London, May 1995.

- Enric Pastor, Jordi Cortadella, Alex Kondratyev, and Oriol Roig. Structural Methods for the Synthesis of Speed-independent Circuits. In *Proc. European Design and Test Conference (EDAC-ETC-EuroASIC)*, pp. 340–347, Paris(France), March 1996.

- Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alexandre Yakovlev. Complete state encoding based on theory of regions. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, Aizu, Japan, March 1996.

- Marco A. Peña and Jordi Cortadella. Combining Process Algebras and Petri Nets for the Specification and Synthesis of Asynchronous Circuits. In *Proc. International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pp. 222–232, Aizu, Japan, March 1996.

- Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alexandre Yakovlev. Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers. In *XI Conference on Design of Integrated Circuits and Systems*, Barcelona, November 1996. (To appear).

Design of VLSI Architectures for Low power

One of the consequences of the high levels of integration and performance that are achieved in VLSI architectures is the increase in power dissipation. Nowadays, and for certain applications, power dissipation is a design parameter as important as area or delay, with the associated increase in design complexity. Several factors have pushed the concern for low-power:

- reliability: the excessive heat dissipated by a circuit may cause failure mechanisms.
- chip package cost: for power hungry chips, a more expensive package has to be used to withstand the dissipated heat.
- battery life: portable battery-driven applications (the fastest growing segment of the computer industry) require a long battery lifetime. The improvements in battery technology can not meet the high increase in power dissipation of these applications.

The solution to these design challenges relies on applying techniques for low power during the design process.

- Enric Musoll and Jordi Cortadella. Low-Power Array Multipliers with Transition-Retaining Barriers. In *Proc. of the Int. Workshop on Power and Timing Modeling Optimization and Simulation (PATMOS)*, pp. 227–238, October 1995.
- Enric Musoll and Jordi Cortadella. High-level synthesis techniques for reducing the activity of functional units. In *Int. Symposium on Low Power Design*, pp. 99–104, April 1995.
- Enric Musoll and Jordi Cortadella. Scheduling and resource binding for low power. In *Int. Symposium on System Synthesis*, pp. 104–109, September 1995.
- Enric Musoll and Jordi Cortadella. Optimizing CMOS circuits for low power using transistor-reordering. In *Proc. European Design and Test Conference (EDAC-ETC-EuroASIC)*, pp. 219–223, March 1996.
- Tomás Lang, Enric Musoll, and Jordi Cortadella. Redundant adder for reduced output transitions. In *XI Conference on Design of Integrated Circuits and Systems*, November 1996.

Software Pipelining for Super-scalar and VLSI processors

Software pipelining is a widespread family of techniques aiming at finding an instruction-level parallel schedule of a loop. These techniques are useful for processors that can issue more that one instruction at a time (as super-scalar processors) or execute multiple operations simultaneously by using a "long instruction" to define them (as Very Long Instruction Word processors, commonly denoted as VLIW).

The objective of this techniques is execute the loop as parallel as possible by optimizing machine resources. This implies execute each iteration of the loop as fast as possible by using the resources available in the machine, that are limited by its architecture. This problem is NP-Hard.

During the last five years we have been working in software pipelining with resource constraints, attempting to reduce the execution time of a loop by using a given set of functional units. Our best heuristic techniques produce optimal results most times. By using an integer linear programming approach, we can also obtain optimal results (for all cases) or test how good the results obtained

by the heuristic techniques are. Our heuristic techniques consume much less time that our integer linear programming techniques, and obtain very similar results.

Software pipelining a loop increases a lot the "register pressure". Currently, we are working developing techniques to reduce the register pressure in parallel schedules without decreasing their execution throughput. This is an important problem in current machines that traditionally has been neglected. However, if enough registers are not available to execute the loop, some variables must be "spilled out" to memory, or the number of cycles of the schedule (initiation interval) must be increased. In both cases the schedule throughput decreases. Our current efforts are addressed to optimize both the throughput and the register pressure of the schedule, by using the set of functional units available in the architecture.

- Fermín Sánchez and Jordi Cortadella. Resource-Constrained Pipelining Based on Loop Transformations. *Microprocessing and Microprogramming*, vol. 38, no. 1-5, pp. 429–436, September 1993.

- Fermín Sánchez and Jordi Cortadella. Resource-constrained software pipelining for high-level synthesis of DSP systems. In Marc Moonen and Francky Catthoor, editors, *Algorithms and Parallel VLSI Architectures III*, pp. 377–388. Elsevier, 1995.

- Fermín Sánchez and Jordi Cortadella. Time-Constrained Loop Pipelining. In *Proc. of the IEEE/ACM International Conference on Computer Aided Design*, pp. 592–596, San José, (USA), November 1995.

- Fermín Sánchez and Jordi Cortadella. Maximum-Throughput Software Pipelining. In *2nd International Conference on Massively Parallel Computing Systems (MPCS'96)*, pp. 483–490, Ischia (Italy), May 1996.

- Fermín Sánchez and Jordi Cortadella. RESIS: A New Methodology for Register Optimization in Software Pipelining. In *Proc. of the European Conf. on Parallel Processing (EUROPAR)*, August 1996.

- Jordi Cortadella, Rosa M. Badia, and Fermín Sánchez. A mathematical formulation of the loop pipelining problem. In *XI Conference on Design of Integrated Circuits and Systems*, Barcelona, November 1996. (To appear).

Symbolic Analysis of Concurrent Systems

The complexity of current digital systems requires an early introduction of formal methods in the analysis and synthesis cycle. Medium complexity system may easily contain more than 10^{50} states. It is clearly impossible to explicitly represent such a number of states in any existing computer. In particular, highly concurrent systems requires the utilization of symbolic techniques in order to overcome the limitations introduced by its exponential number of states. The current work of the group is based on the utilization of high-level models such as Petri nets, and the development of symbolic methodologies supported by Binary Decision Diagrams. The generality of the Petri net formalism allows tackling multiple research areas, like synthesis and verification of asynchronous systems, test-pattern generation, general Petri net analysis and synthesis, code generation for embedded systems, etc... Hence, this research area must concentrate on the development of efficient models and algorithms for the analysis of concurrent systems based on underlying Petri nets or Transition System formalisms. Memory and CPU preserving state encoding and state exploration techniques are required to —in combination with Binary Decision Diagrams and similar data structures— alleviate the state explosion problem.

- Enric Pastor, Oriol Roig, Jordi Cortadella, and Rosa M. Badia. Petri net Analysis Using Boolean Manipulation. In *15th International Conference on Application and Theory of Petri Nets*, volume 815 of *Lecture Notes in Computer Science*, pp. 416–435. Springer-Verlag, June 1994.

- Oriol Roig, Jordi Cortadella, and Enric Pastor. Verification of asynchronous circuits by BDD-based model checking of Petri nets. In *16th International Conference on Application and Theory of Petri Nets*, volume 935 of *Lecture Notes in Computer Science*, pp. 374–391, Torino, June 1995. Springer-Verlag.

- Jordi Cortadella, Michael Kishinevsky, Luciano Lavagno, and Alexandre Yakovlev. Synthesizing Petri Nets from State-Based Models. In *Proc. of the IEEE/ACM International Conference on Computer Aided Design*, pp. 164–171. IEEE Computer Society Press, November 1995.

- Jordi Cortadella, Michael Kishinevsky, Alex Kondratyev, Luciano Lavagno, and Alexandre Yakovlev. Petrify: a tool for manipulating concurrent specifications and synthesis of asynchronous controllers. In *XI Conference on Design of Integrated Circuits and Systems*, Barcelona, November 1996. (To appear).

3.5.2 R+D Projects and Agreements

- **ACID WG-Asynchonous Circuit Design**
  Project length: May, 1996 – April, 1999.
  Funding body: CEC/ESPRIT WG21949.
  Budget Funding: 2.6 M. ptas.
  Holder: Jordi Cortadella.

- **Asynchonous Circuit Design**
  Department contribution: Synthesis and verification of asynchronous circuits from Signal Transition Graphs.
  Project length: June, 1992 – June, 1995.
  Funding body: ESPRIT-II 7255 ACiD-WG.
  Holder: Jordi Cortadella.
  Partners: Univ. of Oxford, Univ. of Manchester, Philips, IMEC, UPC, Univ. of Surrey.

- **The Cathedral Environment**
  Project length: June, 1994 – September, 1994.
  Funding body: CEC/CAPITAL HUMÀ I MOBILITAT CHGE-CT94-0064.
  Budget Funding: 0.0 M. ptas.
  Holder: Jordi Cortadella.
  Partners: Imec, DAC (UPC Associated).

3.5.3 Grants

- **Diseño y Verificación de Circuitos de Bajo Consumo y Alto Rendimiento** (1994–1995) (CICYT TIC–531/94).
  Budget Funding: 2.5 M. ptas.
  Holder: Jordi Cortadella.

- **Arquitecturas de Alta Velocidad y Bajo Consumo para Aplicaciones de Propósito Específico** (1995–1998) (CICYT TIC–419/95).
  Budget Funding: 13.0 M. ptas.
  Holder: Jordi Cortadella.

- **Parallel Architectures Oriented to Symbolic Applications** (1991–1994) (CICYT TIC–1036/91).
  Budget Funding: 18.2 M. ptas.
  Holder: Jordi Cortadella.

3.6 List of papers

In this section we present an exhaustive list of the papers published by the people from the Computer Architecture Departament since 1992.

1996

- José J. Acebrón, Jaime Delgado, and Ramon Mercé. Working Draft of ISO/IEC 12069 - Information Technology - International Standardized Profiles ADFnn - Document Filing and Retrieval (DFR) - Part 5: ADF13 - Common Filing and Retrieval - Document Store Manipulation Profile, May 1996. EWOS EG/SMMI 96/129.

- Anna M. del Corral and José M. Llabería. Increasing the Effective Memory Bandwidth in Multivector Processors. In *22nd Euromicro Conference*, pp. 38–45, Prague (Czech Republic), September 1996.

- Anna M. del Corral and José M. Llabería. Reducing Inter–Vector–Conflicts in Complex Memory Systems. In *Proccedings of the 10th ACM International Conference on Supercomputing (ICS'96)*, pp. 382–389, Philadelphia (USA), May 1996.

- Toni Juan, Tomás Lang, and Juan J. Navarro. The Difference–bit Cache. In *Proceedings of the 23rd International Symposium on Computer Architecture (ISCA'96)*, pp. 114–121, Philadelphia (USA), May 1996.

- Chris Blondia and Olga Casals. Analysis of Explicit Rate Congestion Control in ATM Networks. In *Australian Telecommunication Networks & Applications Conference*, Melbourne (Australia), December 1996.

- Chris Blondia and Olga Casals. Throughput Analysis of the Explicit Rate Congestion Control Mechanism in ATM Networks. In *ITC Specialists Seminar on Control in Communications*, pp. 89–101, (Sweden), 1996.

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Chapter 4

Undergraduate Studies

The teaching assignments of the Department are presented in this section. It includes just the undergraduate courses, offered in the curricula of several centers of the University, which are responsability of this Department.

The Department of Computer Architecture has teaching assignments in the fields of: Computer Architecture, Computer Networks, Operating Systems, and VLSI design. The DAC offers tuition in several engineering schools of the Polytechnic University of Catalonia (UPC), namely: Faculty of Computer Science of Barcelona (FIB)[1], School of Telecommunications Engineering of Barcelona (ETSETB)[2], Technical College of Baix Llobregat (EUPBLl)[3], and Technical College of Vilanova i la Geltrú (EUPVG)[4]. This implies a teaching load of nearly 500 hours per week, including lectures, application and laboratory tasks.

A brief summary of the different courses given by the Department is listed below. Each course is a semester course, lasting from September to January and/or from March to June. Following the name of each course, the number in brackets indicates credits – 1.5 credits equal to one hour per week of classroom or laboratory lectures –, also some keywords are listed. To obtain a complete description of each course, the WWW home page of each School could be used. In the WWW version of this report every course has this own WWW home page.

4.1 Courses offered in the FIB

- **Introducció als Computadors** (9).
  Coordinator: Fermín Sánchez.
  Keywords: Logic Circuits, Digital Systems, Logic Gates, Combinational Logic, Sequential Logic, Processor Logic Design.

- **Estructura de Computadors I** (7.5).
  Coordinator: Jordi Tubella.
  Keywords: Machine Level Programming, Input / Output Subsystem, Virtual Memory Management.

- **Estructura de Computadors II** (4.5).
  Coordinator: Josep Llosa.
  Keywords: Computer Organization, Processor Design, Cache Memories, Evaluation and Design of the Machine Language Level.

- **Introducció als Sistemes Operatius** (6).
  Coordinator: Enric Morancho.
  Keywords: User-view, System–calls, Virtual Memory, Input / Output, Processes, Concurrency.

- **Sistemes Operatius** (6).
  Coordinator: Luis Doreste.
  Keywords: Processes, File Management, Input / Output, Memory Management.

- **Conceptes Bàsics de Xarxes de Computadors** (4.5).
  Coordinator: Jordi Domingo–Pascual.
  Keywords: Data Communications, Protocols, Computer Networks, LAN, WAN, MAN, Internetworking, OSI Reference Model.

- **Xarxes de Computadors** (6).
  Coordinator: Jordi Iñigo.
  Keywords: Data Communications, Protocols, Computer Networks, LAN, WAN, OSI Reference Model.

[1] http://www-fib.upc.es/
[2] http://citel.upc.es/etsetb
[3] http://www-eupbl.upc.es
[4] http://www-eupvg.upc.es

- **Disseny Bàsic VLSI** (6).
  Coordinator: Jordi Cortadella.
  Keywords: VLSI, Logic Design, Microelectronics, CMOS Technology, Design Tools.

- **Arquitectura de Computadors** (9).
  Coordinator: Enrique Herrada.
  Keywords: Computer Arithmetic, Pipelining, Processor Performance, Instruction Level Parallelism, Models of Pipelined Processor.

- **Administració de Sistemes Operatius** (6).
  Coordinator: Toni Cortés.
  Keywords: Operating Systems Management, UNIX, Local Networks, Security.

- **Sistemes de Transmisió de Dades** (4.5).
  Coordinator: Isabel Gallego.
  Keywords: Internet, OSI (Open Systems Interconnection), Network Service, Transport Service and Protocol, TCP/IP (Transport Control Protocol/ Internet Protocol), ASN.1 (Abstract Syntax Notation One), XDR (eXternal Data Representation), RPC (Remote Procedure Call).

- **Disseny i Avaluació de Configuracions** (6).
  Coordinator: Olga Casals.
  Keywords: Performance Analysis, Modeling Techniques, Measurement Techniques, Queueing Models.

- **Síntesi Automàtica de Circuits** (6).
  Coordinator: Jordi Cortadella.
  Keywords: Design Tools, CAD Tools, Placement, Routing, Logic Synthesis, High–Level Synthesis.

- **Arquitectures Vectorials** (6).
  Coordinator: Juan J. Navarro.
  Keywords: Vector Data Path, Multimodule Memories, Vector Performance, Dependence Analysis, Vectorizing Techniques, Dense and Sparse Matrix Operations, Vectorization of Recurrences.

- **Estructura Interna d'un Sistema Operatiu** (4.5).
  Coordinator: Sergi Girona.
  Keywords: Unix Internals and Unix Device Drivers.

- **Sistemes Públics de Dades** (6).
  Coordinator: Josep Solé–Pareta.
  Keywords: Data Transmission Devices, HDLC protocol, LAN, MAN, ISDN.

- **Conceptes Avançats de Sistemes Operatius** (6).
  Coordinator: Jordi Torres.
  Keywords: Distributed Systems, Distributed Operating Systems, Microkernels, Inter–process–communication, Distributed–file–system.

- **Arquitectura d'Aplicacions Distribuïdes** (6).
  Coordinator: Jaime Delgado.
  Keywords: OSI (Open Systems Interconnection), Internet, Application Layer, Electronic mail, Multimedia documents architecture and protocols, File transfer protocols, Real time protocols, Security in distributed applications.

- **Disseny de Sistemes Operatius** (6).
  Coordinator: José I. Navarro.
  Keywords: Microkernels, Scheduling, Memory Management, Remote Procedure Calls.

- **Multiprocessadors** (6).
  Coordinator: José M. Llabería.
  Keywords: Shared Memory Multiprocessors, Distributed Memory Multiprocessors, Performance Evaluation, Interconnection Networks, Synchronization, Cache Coherence, Parallel Programming Techniques, Parallelization.

- **Avaluació i Sintonització de Sistemes Operatius** (4.5).
  Coordinator: Jesús Labarta.
  Keywords: Performance Evaluation, Tuning, OS Modelization, Benchmarking.

- **Supercomputadors** (6).
  Coordinator: Antonio González.
  Keywords: Parallel processor microarchitecture, Software scheduling, Dynamic scheduled processors, Prefetching, Programming models, Compiling techniques, Parallelization.

4.2 Courses ofered in the ETSETB

- **Introducció als Ordinadors** (6).
  Coordinator: Juan C. Cruellas.
  Keywords: High Level Programming Fundamentals, Basic Algorithms, C Language Software Development & Test.

- **Arquitectura i Sistemes Operatius I** (6).
  Coordinator: Agustín Fernández.
  Keywords: Machine Level Programming, Input / Output Subsystem, Computer Organization.

- **Arquitectura i Sistemes Operatius II** (4.5).
  Coordinator: Dolors Royo.
  Keywords: Operating Systems, UNIX, System Call, Process Management, File System, Pipelined Processors, Memory Hierarchy

- **Programació Avançada per a Sistemes de Telecomunicació** (6).
  Coordinator: Juan C. Cruellas.
  Keywords: Programming, Abstract Data Types, C language, Object Oriented Programming.

- **Segmentació i Paral.lelisme** (6).
  Coordinator: Eduard Ayguadé.
  Keywords: Processor Design, Pipelined and Superscalar Microprocessors, Cache Memory, Multiprocessor Systems and Vector Processors.

- **Arquitectura i Sistemes Operatius** (4.5).
  Coordinator: Cristina Barrado.
  Keywords: Computer Architecture, Operating Systems, Shell, UNIX, System Calls, Scheduling, File System.

- **Laboratori d'Arquitectura i Sistemes Operatius** (3).
  Coordinator: Cristina Barrado.
  Keywords: Operating System Kernel, Shell, UNIX, System Calls, Process Communication.

4.3 Courses ofered in the EUPBLl

- **Introducció als Ordinadors I** (6).
  Coordinator: Manel Medina.
  Keywords: Computer Programming, Basic Algorithms, Software Development Methodology.

- **Laboratori d'Ordinadors** (4.5).
  Coordinator: José Polo.
  Keywords: High Level Programming Fundamentals, C Language, Software Development & Test.

- **Introducció als Ordinadors II** (6).
  Coordinator: Joan M. Parcerisa.
  Keywords: Computer Organization, Assembler Language, Cache Memory, Operating Systems, Multitasking, Virtual Memory.

- **Laboratori de Software I** (4.5).
  Coordinator: Xavier Perramon.
  Keywords: Programming, C Language, Assembler, i8086, Input/Output routines

- **Laboratori de Software II** (4.5).
  Coordinator: José J. Acebrón.
  Keywords: C programming, Databases, MS–Windows.

- **Programació C++** (4.5).
  Coordinator: Llorenç Cerdà.
  Keywords: Programming Language, Object Oriented, C++

- **Entorn de Programació UNIX** (1.5).
  Coordinator: Enric Peig.
  Keywords: C programming, Unix fundamentals, Client/server arquitecture.

4.4 Courses offered in the EUPVG

- **Introducció als Computadors** (9).
  Coordinator: Xavier Masip.
  Keywords: Logic Circuits, Digital Systems, Logic Gates, Combinational Logic, Sequential Logic, Processor Logic Design.

- **Estructura de Computadors I** (7.5).
  Coordinator: Frederic Vila.
  Keywords: Machine Level Programming, Input / Output Subsystem, Virtual Memory Management.

- **Estructura de Computadors II** (4.5).
  Coordinator: Eva Marín.
  Keywords: Computer Organization, Processor Design, Cache Memories, Evaluation and Design of the Machine Language Level.

- **Introducció als Sistemes Operatius** (6).
  Coordinator: Marisa Gil.
  Keywords: User-view, System–calls, Virtual Memory, Input / Output, Processes, Concurrency.

- **Sistemes Operatius** (6).
  Coordinator: Marisa Gil.
  Keywords: Processes, File Management, Input / Output, Memory Management.

- **Arquitectura de Computadors** (9).
  Coordinator: Sergio Sánchez.
  Keywords: Computer Arithmetic, Pipelining, Processor Performance, Instruction Level Parallelism, Models of Pipelined Processor.

- **Arquitectura de Computadors (T)** (4.5).
  Coordinator: Eva Marín.
  Keywords: Computer Architecture, Machine Level Programming, Input / Output Subsystem.

Chapter 5

Graduate Studies

This chapter presents the graduate studies conducted by the Department. A brief description of the contents of each course is given here. A list of the Ph.D. degrees achieved in the Department in the last five years, closes this chapter.

5.1 The Ph.D. program

The Ph.D. program at UPC includes courses, projects, research and a doctoral dissertation. The Computer Architecture Department is responsible for the Ph.D. program on Architecture and Technology of Computers (in catalan: Arquitectura i Tecnologia de Computadors).

DAC offers intense, research-oriented programs leading to the degree of Master of Phylosophy in Computer Science. Current emphasis is on areas of Computer Architecture, Operating Systems and Computer Communications.

Department encourages qualified students with strong background in Computer Science and/or engineering to pursue the Doctor of Phylosophy degree in Computer Science. Students with strong undergraduate records and training in computer science are admitted directly to the doctoral program. In addition, students from other areas without extensive in computer science can pursue the course provide a positive inform given by the UPC's Doctoral Committee.

The Ph.D. curricula in Architecture and Technology of Computers consists of required course work, theoretical and experimental work, and culminates in the dissertation and its defense.

5.2 Program of study

To obtain a doctorate degree, a doctoral student has at least two years to complete 32 graduate level credits, of which at least 18 must be courses offered in the Ph.D. programs at UPC. A credit is equivalent to 10 hours of lectures. Research activities and courses from other Universities can be also validated as credits in a limited way.

After completing these credits and the theoretical and experimental research work the student is expected to write a dissertation. It must be presented by the candidate to the public and to a committee of five distinguished professors, of which no more than two can be from the Department. The advisor cannot be part of the committee.

The cooperative spirit and open atmosphere of the Department is reflected in the tradition of joint work of students and faculty on projects, papers and Department activities. The cooperative structure of the Department encourages students to choose their fields and supervisors on the basis of intellectual interest.

5.3 Admision requirements

Applications for admission are evaluated on the basis of academic record, technical background, and other relevant qualifications. Applicants for admission to graduate studies should have an undergraduate degree in computer science or a closely related field.

All applicants whose native language is not Catalan or Spanish should demonstrate proficiency in one of them. The UPC provides remedial courses on Catalan language and culture.

5.4 Graduate Program Courses

The goal of this program is to introduce students to research topics related to the theory, practice, analysis and design of Computer Systems. In particular the main topics of the program are: Computer Architecture, Supercomputers, VLSI Design, Parallelism, Operating Systems, Distributed Systems, and Communication Networks.

Coordinator: Jordi Cortadella

A brief summary of the different courses given by the Department during the academic course 1996/1997, is listed below. Following the name of each course, the number in brackets indicates credits (1 credit equals 10 hours of lectures).

- **Parallel Algorithms** (3).
  Coordinator: Juan J. Navarro.

The objective is to study small and coarse grained parallel algorithms for linear algebra operations (matrix multiplication, linear system of equations by direct and iterative methods and the computation of eigenvalues of a symmetric matrix). The emphasis is on the adaptation of the algorithms to the underlying architecture. The architectures under consideration are those based on superscalar and vector processors and multiprocessor systems (shared and distributed memory). Modelization and performance evaluations are also considered.

- **Document architectures and protocols** (3).
  Coordinator: Jaime Delgado.
  These course deals with the more advanced aspects of document architectures and protocols, based on existing and under development standards for representation, interchange and manipulation and remote handling of documents. Furthermore, focus is made on the international standarization process. The topics include, after an introduction about distributed applications and electronic mail: ODA (Open Document Architecture), Remote manipulation of documents, DFR (Document Filing and Retrieval), Document communication services, Conferencing services and protocols, Multimedia and hypermedia documents, and, in parallel with the other topics, the standarization process.

- **Architectures oriented to symbolic computing** (3).
  Coordinator: Antonio González.
  This course studies execution models and architectures oriented to provide an efficient support to declarative languages, especially logic and functional languages. The WAM and SECD abstract machines are described and their sequential implementation is analyzed. Finally, different sources of parallelism and the main issues for its exploitation in a multiprocessor environment are are studied.

- **Broadband Communications** (3).
  Coordinator: Jordi Domingo–Pascual and Josep Solé–Pareta.
  The information technology environment is in quick evolution. A bunch of new applications are emerging, some of them involving high performance computation and high transfer rates. New technologies are also being considered. This has an important impact on the communication networks. High speed and service integration are the current major demands. This course focuses on both, broadband networks and service integration. The Asynchronous Transfer Mode (ATM) is the technology that is envisaged to support the Broadband ISDN. The course offers an in–depth presentation of all the technical issues related with ATM networks: the Protocol Reference Model for the B-ISDN defined by the ITU–T, and the UNI 3.1 interface defined by the ATM Forum. It also presents the most recent developments in this fast moving field: ATM traffic Management aspects, ATM signaling, the Private Network Node Interface and the general aspects for ATM Network Management.

- **Distributed Systems Design** (3).
  Coordinator: Leandro Navarro.
  This Course presents the topics related to distributed computing, from the basic paradigms of distribution: time, fault tolerance, group communication, remote procedure call, channel based communication. Several areas of application are discussed: Internet (routing, protocol architecture, applications), distributed file systems, environments for the development of distributed applications, computer supported cooperative work systems.

- **Traffic management in ATM networks** (3).
  Coordinator: Olga Casals.
  This course describes the characteristics of the traffic control and congestion control procedures for ATM technology. In order to fully exploit the advantages of ATM, efficient, effective and easy–to–implement functions which control the traffic streams are needed. We discuss the following functions witch form a framework for managing and controlling traffic and congestion in ATM networks and which may be used in appropriate combinations:

Connection Admission Control (CAC), Feedback controls, Usage Parameter Control (UPC), Priority Control, Traffic Shaping, Network Resource Management (NRM), Frame Discard, ABR Flow Control.

- **Memory Hierarchy in Scalar Processors** (3).
  Coordinator: Angel Olivé.
  The goal is to show techniques to alleviate the memory bottleneck problem, due to the gap between processor cycle time and memory access time. The techniques revised in this course are related to the concept of memory hierarchy. Methods addressed in the course deal with the latency reduction and how to get efficiency in the presence of this memory latency. Organization of memory to increase the bandwidth is also studied.Hardware solutions to assure information coherence in the different memory levels, are also considered.

- **Programming Models and Tools for Supercomputers** (3).
  Coordinator: Eduard Ayguadé.
  In this course we present different programming models for parallel computing (shared and distributed memory, data parallel), as well as tools for parallel program analysis and performance prediction. Finally the course also focuses on tools for the automatic loop parallelization and data distribution from the analysis of sequential code.

- **Parallelism and Segmentation in the Design of General–Purpose Processors** (3).
  Coordinator: José M. Llabería.
  The objetive of this course is to show the application of the pipelining and parallel techniques to the design and implementation of scalar processors. Techniques to reduce the cycle losses, in the processor and in the interaction processor–memory hierarchy, are analysed. An updated overview of commercial processors is presented.

- **Automatic Synthesis of Circuits** (3).
  Coordinator: Rosa M. Badia.
  In this course existent techniques for layout synthesis and high level synthesis are mainly studied. In the area of layout synthesis, the existent approaches to perform the different phases of this level of design are described: partitioning, placement, routing and compaction. With respect to high level synthesis, the different phases that compose it and the different approaches to resolve them are described. This phases are: operation scheduling and resource binding (hardware allocation). Also, an overview of the existent hardware description languages is done, giving special emphasis to VHDL.

- **Logic synthesis and verification of digital circuits** (3).
  Coordinator: Jordi Cortadella.
  In the area of logic synthesis, techniques for two–level and multilevel synthesis are reviewed. Methods for logic minimization, reduction of delay and technology mapping are presented. Next, techniques for the synthesis of sequential circuits are studied: state minimization, state encoding and FSM partitioning. In the area of formal verification, several techniques for combinational and sequential circuits will be reviewed: Binary Decision Diagrams, reachability analysis, symbolic model checking, temporal logic, etc. Finally, the course covers some basic techniques for the synthesis and formal verification of asynchronous circuits.

- **Supercomputers** (3).
  Coordinator: Mateo Valero.
  This course focuses on the study of the architecture of high–performance computers. Since the architecture of such computers evolves very dynamically, the contents of the course will evolve at the same pace to reflect the latest trend in the design of high–performance computers. Currently the course covers three types of architectures: Vector machines, Instruction–Level Parallel processors and Multiprocessors.

- **Parallelization of numerical applications in Engineering** (3).
  Coordinator: José M. Cela.
  This course is focused in the parallelization techniques for the numerical simulations for PDEs and Markov Chains. Sparse linear systems are the numerical kernel of these applications. We describe the iterative solvers used for such systems (Domain Decomposition solvers, Krylov subspace solvers and Multigrid solvers). Emphasis is put in the parallelization approach based in message passing programming model. PVM is used as communication library for practical examples.

- **Broadband, integrated services and Multimedia Applications** (2).
  Coordinator: Jordi Domingo–Pascual.
  Real–time multimedia applications impose several strict requirements to the communication network services in order to obtain the desired Quality of Service (QoS). The Broadband Integrated Services Network (B–ISDN) using the ATM technology is expected to provide this QoS guarantee for distributed multimedia applications. This course reviews the main characteristics of multimedia communications and the demands they impose to the communication network services and describes the basic communication services for real-time multimedia distributed applications.

- **Broadband, integrated services and Multimedia Technologies** (2).
  Coordinator: Josep Solé–Pareta.
  Broadband Communications, Integrated Services and Multimedia Applications are the main key words to identify the currently Computer Networks evolution. Network-based multimedia applications are becoming the norm rather than the exception, the traditional separation between Local and Wide area networks is disappearing with the introduction of ATM and the Personal Communication Systems concept will definitively link Mobile Communications with Computer Networks. This course focuses on the technological and architecture issues, which are making possible these changes.

On the Computer Architecture Departament Ph.D. Program some seminars are given. This seminars are given for worldwide experts in specific topics related to Architecture and Technology of Computers. Seminars given in the academic course 1996/1997 are:

- **Distributed Shared Memory: Concepts and Systems** (1).
  Veljko Milutinovic (University of Belgrad)
  In this seminar, concepts and algorithms for Distributed Memory Multiprocessors, but shared at the programming level, are introduced. This is the architecture of the last commercial platforms. This seminar is based on the book edited by IEEE "Distributed Shared Memory: Concepts and Systems".

- **Current and Future High–performance Processors** (1).
  James E. Smith (University of Wiscosin–Madison)
  This seminar describes the current high performance scalar architectures. The current and future trends on microprocessor design are also presented.

- **High–level Languages, Compilers and Tools for Parallel Scientific** (1).
  Hans Zima (University of Vienna)
  Available programming tools and parallel oriented data programming languages are presented in this seminar. Programming languages as Vienna Fortran and High Performance Fortran (HPF), based on the "Data–Parallel Single–Program Multiple–Data (SPMD)" model, have been introduced to program parallel scalable architectures in an abstract way. Their main features and constrains are analyzed.

5.5 Ph.D. degrees

In this section the Ph. D degrees obtained since 1992 are shown.

- Jordi Tubella. *MULTIPATH: Un Sistema para la Programación Lógica.* PhD thesis, Universitat Politècnica de Catalunya (UPC), November 1996. Advisor Antonio González.

- Enric Musoll. *High–Level and Logic Synthesis for Low Power.* PhD thesis, Universitat Politècnica de Catalunya (UPC), July 1996. Advisor Jordi Cortadella.

- Enric Pastor. *Structural methods for the shyntesis of asynchronous circuits from signal transition graphs.* PhD thesis, Universitat Politècnica de Catalunya (UPC), April 1996. Advisor Jordi Cortadella.

- Montse Peiron. *Optimització del Rendiment del Sistema de Memòria en Multiprocessadors Vectorials.* PhD thesis, Universitat Politècnica de Catalunya (UPC), February 1996. Advisors Mateo Valero and Eduard Ayguadé.

- Josep Llosa. *Reducing the impact of register pressure on software pipelined loops.* PhD thesis, Universitat Politècnica de Catalunya (UPC), February 1996. Advisors Mateo Valero and Eduard Ayguadé.

- José M. Cela. *Algoritmos paralelos de descomposición en dominios para la resolución de sistemas lineales.* PhD thesis, Universitat Politècnica de Catalunya (UPC), February 1996. Advisor Juan J. Navarro.

- Miguel A. García. *Algorithms and architectures for efficient heterogeneous multisensory integration in robotics.* PhD thesis, Universitat Politècnica de Catalunya (UPC), January 1996. Advisor Luis Basáñez.

- Fermín Sánchez. *Loop Pipelining with Resource and Timing Constraints.* PhD thesis, Universitat Politècnica de Catalunya (UPC), January 1996. Advisor Jordi Cortadella.

- Francisco Jordán. *Infraestructura de Seguridad en Aplicaciones y Sistemas Distribuidos.* PhD thesis, Universitat Politècnica de Catalunya (UPC), October 1995. Advisor Manel Medina.

- Josep–L. Larriba–Pey. *Design and Evaluation of Tridiagonal Solvers for Vector and Parallel Computers.* PhD thesis, Universitat Politècnica de Catalunya (UPC), March 1995. Advisor Juan J. Navarro.

- Rosa M. Badia. *Síntesi d'alt nivell de circuits asíncrons.* PhD thesis, Universitat Politècnica de Catalunya (UPC), July 1994. Advisor Jordi Cortadella.

- Marisa Gil. *Cooperación entre la aplicación y el kernel para la planificación de flujos, en sistemas multiprocesadores, como soporte al paralelismo.* PhD thesis, Universitat Politècnica de Catalunya (UPC), July 1994. Advisor José I. Navarro.

- Jordi Torres. *Extracció automàtica de paral.lelisme en bucles seqüències numèrics amb recurrències.* PhD thesis, Universitat Politècnica de Catalunya (UPC), November 1993. Advisor Eduard Ayguadé.

- Alvaro Suárez. *Ordenación de la ejecución de particiones en algoritmos sistólicos.* PhD thesis, Universitat Politècnica de Catalunya (UPC), November 1993. Advisor José M. Llabería.

- German Santos. *Análisis y evaluación de los sistemas de protección contra la congestión en la red digital de servicios integrados en banda ancha.* PhD thesis, Universitat Politècnica de Catalunya (UPC), February 1993. Advisor Jordi Domingo–Pascual.

- Agustín Fernández. *Transformación sistemática de algoritmos sistólicos para la programación de multicomputadores.* PhD thesis, Universitat Politècnica de Catalunya (UPC), December 1992. Advisor José M. Llabería.

- Jorge García. *Modelos analíticos para la evaluación de mecanismos de control de tráfico en redes ATM.* PhD thesis, Universitat Politècnica de Catalunya (UPC), February 1992. Advisor Olga Casals.

- Leandro Navarro. *Una arquitectura distribuida para comunicación de grupos.* PhD thesis, Universitat Politècnica de Catalunya (UPC), January 1992. Advisor Manel Medina.

Chapter 6

Related Research Centers

In this chapter we present some Research Centers, very related with the main research activities of our Department.

6.1 European Center for Parallelism of Barcelona

Introduction

The European Center for Parallelism of Barcelona (CEPBA)[1] belongs to the UPC (Universitat Politècnica de Catalunya) and officially started its activities in October 1991. CEPBA integrated the experiences in parallel computing of the Computer Architecture Department (DAC) with the high-performance computational requirements of other Departments such us Signal Theory and Communications (TSC), Civil Engineering (RME), Computer Systems and Languages (LSI), Nuclear Physics and Engineering (FEN) and Applied Physics (FA).

CEPBA was created by initiative of the Ministry of Education and sponsored with economic funding from the Spanish CICYT (Comisión Interministerial de Ciencia y Tecnología) and from the Catalan CIRIT (Comissió Interdepartamental de Recerca i Innovació Tecnològica).

Since October 1995, CEPBA activities have been coordinated together with those of the CESCA (Supercomputing Center of Catalonia) throughout the C^4 (Computing and Communications Center of Catalonia) founded by the CIRIT, Fundació Catalana per la Recerca and UPC.

Activities

CEPBA develops its activities in three main areas:

- Services: providing access to state-of-the-art parallel platforms,
- Training: giving training courses on algorithms, architectures, operating systems and tools,
- Technology transfer along two complementary lines:
  - Research and Development: being directly involved as a parallelization expert in high technology HPC projects at worldwide level. This activity is carried through the High Performance Computing Group[2] of the Computer Architecture Departament.
  - Promotion of HPC: encouraging local industry and the research community as a whole to use this technology, accompanying them on their initial steps and promoting the ESPRIT culture and objectives among them.

Research Topics

CEPBA has research experience in a wide range of topics in computer architecture and parallel computing. The following point summarize the areas on which research work is done:

- Algorithms and libraries: finite element solvers, domain decomposition techniques.
- Compilers: automatic parallelization, low level scheduling, data distribution.
- Programming models and tools: Definition and implementation, visualization, performance analysis and prediction.
- Operating systems: Microkernels, scheduling, file systems.
- Computer architecture: Processor design, memory hierarchy optimization, and multiprocessors.
- Performace evaluation: Queueing networks, analytical models, simulation.

[1] http://www.cepba.upc.es/
[2] http://www.ac.upc.es/hpc/

Projects

CEPBA has a wide experience in cooperative projects with both industrial and academic orientation. Our research experience is in this way reflected in courses and technology transfer projects. The participation in projects provides topics and ideas which are also important for our research activity. The following list sumarizes the most important projects done by CEPBA and/or the High Performance Computing Group of the Computer Architecture Departament. Most of this activity is through EC funded projects.

- **Management of Technology Transfer**: CEPBA–TTN, PCI–II, PCI–PACOS.
- **Research and Development** : SHIPS, IDENTIFY, PROMENVIR, PARALIN, SHIPS, PERMPAR, COMANDOS II, SUPERNODE II, EDS, GENESIS, PARMAT, SLOEGAT, DDT.
- **Basic and Long Term Research**: NANOS, APPARC, SEPIA, MHAOTEU, HPF Compiler Survey.
- **Mobility of Researchers**: HCM, TMR, PECO.
- **Training**: COMETT, PARANDES, PARALIN.

HPC Facilities

The following machines installed at CEPBA are offered in conjunction with those of CESCA under a common service policy managed by the C^4.

- **SGI Origin 2000 Server**
  from Silicon Graphics, with 32 MIPS R10000 processors (each one with 4 MB of cache), and 4 Gb of main memory. Its theoretical peak performance is 12.5 Gflop/s.
  Coming soon! upgrade to 64 MIPS R10000 processors and 8 Gb of main memory.
- **SGI Power Challenge**
  from Silicon Graphics, with 16 R10000 processors (each one with 2 MB of cache) and 2 Gigabyte of main memory. Its theoretical peak performance is 6.3 Gflop/s.
- **DEC Alpha Server 8400**
  from Digital Equipment Corporation, with 6 Alpha 21164 processors running at 440 MHz, and 2 Gigabyte of main memory. Its theoretical peak performance is 5.28 Gflop/s.
- **Convex C3480**
  from CONVEX Computer Corporation, with 8 vector processors and 1 Gigabyte of main memory. Its theoretical peak performance is 400 Mflop/s for double precision operations and 800 Mflop/s for single precision.
- **CM–200**
  from Thinking Machines, with 2K processors and 256 Megabytes of memory. Its theoretical peak performance is 640 Mflop/s for double precision operations and 1.28 Gflop/s for single precision.
- **Supernode SN–1000**
  from Parsys, with 32 transputers T-800, each one with 4 Megabytes of memory. Its theoretical peak performance is 64 Mflop/s.

User Support

CEPBA has a User Support Team responsible of helping application developpers to optimize their codes on our machines. This includes both sequential optimizations (restructuring for locality, I/O, ...) and parallelization of the codes. In this case, message passing (PVM, MPI), data parallel (HPF) or shared memory (directives) support is provided depending on the users approach and constrains.

The support can be as loose as answering questions throught electronic mail or phone or as tight as direct work on the terminal with the user for several days. We offer some terminals close to our support staff for users to come and work under close supervision.

The address of the CEPBA is:

European Center for Parallelism of Barcelona (CEPBA)[3]
c/ Jordi Girona 1-3. Mòdul D6 Campus Nord
08034 Barcelona (Spain)
Phone: (+34 3) 401 69 86
Fax: (+34 3) 401 70 55

[3] http://www.cepba.upc.es/

6.2 esCERT–UPC: The Spanish Cert

Introduction

On January 1996, esCERT–UPC[4], the Spanish CERT became operative. It is sponsored by the Spanish government (through CICYT: TIC95–0903–C02–01, TEL–96–1626–CE), the Catalan Government (through CUR: PQS–95), and the European Commission (through TA ICE–TEL) and the UPC (Universitat Politècnica de Catalunya), a public university, and plans to give service to the whole Spanish Internet community. Nearly a the same time, RedIris, the Spanish academic network, set up his own CERT, Iris–CERT, that has to give service to the academic network (RedIris) members.

The goals of esCERT–UPC are:

- Provide information about security tools and mechanisms
- Promote awareness and skilful about security problems through conferences, tutorials and seminars
- Help organizations connected to Internet to define security policies.
- Handle Security incidents where Spanish organizations of any kind are involved.

Our team at the UPC has been active in the analysis of the computer security related problems for about 10 years now. We have been participating in computer security European Commission funded projects, and also in the security working groups of European organizations like TERENA (formerly RARE), EWOS (CEN/CENELEC) Standardization organization, etc.

Having been recognized as a Spanish CERT by several Spanish organizations and Internet service access providers, we would like to become a formal member of FIRST, in order to be able to establish full bilateral cooperation with other CERTs around the world, in the co–ordination of incidents or emergencies where Spanish organizations are involved.

This framework describes esCERT–UPC, its organization and its basic policies

esCERT–UPC Staff

esCERT–UPC consists of:

- a kernel of members, including the Chair of esCERT,
- a Steering committee Group, composed by UPC staff, who co–ordinates and gives recommendations to the work carried out by esCERT–UPC,
- a Special Members group, a set of collaborators in the tasks of giving seminars and solving specially difficult security incidents.

The contacts between esCERT–UPC members are made through several private distribution lists, where secure mail is used when its necessary.

esCERT–UPC kernel. The kernel consists of a Chairman and a number of members, all of them belonging to UPC. While chairman co–ordinates the team, the members contribute in internal and external information systems handling, incident resolution and other necessary tasks.

Currently, there are 4 members and a Chairman, but the number of members is expected to grow in the next future.

Special Members. Special Members are specialists on different platforms. Their collaboration is required in case of potentially important security problems wold arise. Some of them also collaborate on security training.

Currently there are 29 special members, and all of them belong to different departments of the UPC.

esCERT Steering Group. The steering group gives new directives and recommendations to esCERT–UPC. esCERT–UPC reports regularly to this group.

[4] http://escert.upc.es/

Contacting esCERT–UPC and Technical Provisions

esCERT–UPC is reachable by telephone, fax, e–mail and postal mail.

There are two levels of priority defined. Telephone and high priority email constitute the highest priority level, and the second level can be obtained through normal email, fax, telephone and postal mail. A secure channel is required in a first level priority.

All the internal and external information systems are protected by logical and physical security mechanisms. Logical security is based on connection and local data encryption, network level filter, application level filter, periodic auditing of sensitive files or configurations and periodic back up. Physical security of hosts, telephone or letter box is also considered.

Operational Activities and Policies

We have three classes of information: internal, confidential internal, and external. esCERT–UPC members use a secure communication channel when the nature of information requires it. Thus, esCERT–UPC has two pairs of public keys, one for singing purposes –the sign key– and another for contact purposes –the contact key–. In addition, every member has his own key pair.

Language used in internal information is Catalan, but public information is produced in English and/or Spanish language as well, Since esCERT–UPC gives service to Spanish Internet community.

Public Keys. Each member has his own key pair, and the other members public keys. While esCERT–UPC has its own key pairs, only esCERT–UPC kernel members can use them. These keys are used through PGP mail, and are published through the Spanish PGP–key server, managed by UPC.

Incident Numbers and Database. When new incidents are reported, they are logged into an incident database. The incident form reported by the involved site is stored into the database, and marked as confidential information. Also, a unique identification number and an alias are assigned to the incident. The format of the unique number is YYYYMMDDNN, where YYYY stands for year, MM for month number, DD for day number and NN for incident number of the day.

The information in the database is used to generate statistics such as number of incidents, as open and closed, number of calls for help desk, number of queries received, number of phone calls received, number of electronic mails processed, average time to solve the problems, breakdown of severity of incidents, and others to be proposed.

Confidential Internal Information. This information is available only for esCERT–UPC kernel members. It mainly consists of incident information, points of contact and vulnerability information.

Internal Information. This information is available for esCERT–UPC members –kernel and specialized members–. It is mainly a vulnerabilities database, contact information and security internal bulletins. Authorized members can use this information through a https interface.

External Information. It comprises public information. Everyone with a web browser and FTP client has access to it, i.e. the information is intended to reach all the Spanish speaking community, and not only our explicit constituency.

Incident Handling. As a CERT, we contribute and co–ordinate the resolution of security incidents where Spanish organizations are involved, establishing also the recommendations to the attacked Spanish computers' system managers to avoid further similar problems, and reporting the incident (with the required confidentiality and non–disclose) to organizations potentially able to become victims of the same kind of attack.

There are many kinds of incidents, but all of them have a common general handling procedure. esCERT–UPC has no authority upon sites involved on a incident, the task is just helping the involved site(s) to solve the incident. When an incident is received the following steps are followed:

- Ask for the incident report through a secure channel
- Mark this information as confidential, and open the new incident.

- Select all the information available about to the incident (historic, vulnerabilities, reference books and so on).
- Establish a strategic reaction plan for the attacked site.
- If necessary alert other sites or other IRTs, or law enforcement agencies.
- Follow up the implementation of the plan and improve it if necessary.
- Close the incident, once reestablished the adequate security level in the attacked site.
- If a new threat is found, report it to the Internet society the society through the opportune channels. Asking for a incident reporting form

The incident reporting form helps to gather incident information. The information the reporting form gives is:

- Names of host(s) compromised at involved site
- Information about architecture and OS (operating system and revision) of compromised host(s) of the site
- Patches applied. Before or after the incident.
- Account name(s) compromised
- Other host(s)/site(s) involved in the incident.
- Other contacted involved site(s) and contact information.
- Ask for permission for giving information to other involved sites in case if were necessary (i.e., name, e–mail address, and phone number).
- Law representants contacted
- Appropriate log extracts.
- Which kind of assistant its expected from esCERT–UPC

Education and Training

One of the goals of esCERT–UPC is to give education and training about security problems to the Spanish Internet community. The activities, which are day to day updated with the new security issues, consist on giving a complete information server about security issues, conference presentations, panel sessions, exercises, courses, journal articles, security audits and consulting.

We give a complete curses or seminars to the organizations that ask for them. The seminars include security polices, risk analysis, UNIX security, firewall configurations, etc. We also include practical sessions of installation and use of security tools. Until now the courses have been given to organizations located close to the UPC, but we have formal compromises to to lecture it in several places in Spain, both at universities and at private organizations.

Information Site

esCERT–UPC selects security information and puts it on its information server. Our WEB and FTP servers give information only about security issues. Organizations can fetch from it security tools such as: auditing, cryptographic, firewalling and miscellaneous for many platforms and architectures. Many documentation, papers and information about security can also be consulted from our information server. In addition, in order to reduce Internet traffic and improve the downloading time, we have mirrors to CERT advisories, CERT bulletins and other interesting sources as SSL development.

Additional information is given to organizations that have subscribed our services.

6.3 Advanced Broadband Communications Center

Introduction

The Advanced Broadband Communications Center (CCABA)[5] – CCABA is the acronym of "Centre de Comunicacions Avançades de Banda Ampla" – was set up in January 1994 with the aim of consolidating a multi–disciplinary research group. Currently this center integrates researchers from several Departments within the Polytechnic University of Catalonia (UPC), which have complementary interests on the communications research fields, namely the Integrated Broadband Communications research group, the Optical Communications research group, and the Radio and Mobile Communications research group. The research center is supported by the University and is being partially funded by the Spanish Education Ministry (CICYT) and by Research Commission of the Catalan Government (CIRIT-CUR) under several grants. The CCABA manages the UPC Spanish National Host platform.

The following paragraphs describe briefly the profile of the research groups within the CCABA.

Integrated Broadband Communications group

This research group belongs to the Computer Architecture Department. Most of the topics covered by this research group are strongly related with B-ISDN/ATM networks and broadband services and applications: ATM switching, communication protocols, source traffic modeling, network resource management policies and bandwidth allocation, traffic and congestion control on ATM networks, routing strategies for ATM networks, ATM local area networks, internetworking through ATM, network management, multicast over ATM, quality of service management, transport protocols over ATM and parallel distributed computing over ATM.

Main researchers: Jordi Domingo–Pascual and Josep Solé–Pareta.

Participation in European R&D projects:

- Technology for ATD (R1022, 1988 - 1992); Exploitation of an ATM Technology Test–Bed for Broadband Experiments and Applications, EXPLOIT (R2061, 1992–1995).
- Multimedia Information Window for National Hosts, InfoWin (AC113, 1996–1998).
- Mobile Integrated Communications in Construction, MICC (AC088, 1996–1998).
- Multimedia Telecommunication Services, COST 237Action (1996–1998).
- Integrated MultiMedia Project, IMMP (AC023, 1997–1999).

Radio Communications group

The Radio Communications group belongs to the Signal Theory and Communications Department. At the present it focuses its main activity in the area of Mobile Communications field where it is active developing research work on modulation, equalization, synchronization, coding related with the transport layers for both TDMA and CDMA access techniques.

Main researchers: Ramon Agustí Comes and Ferran Casadevall Palacio.

Participation in European R&D projects:

- Intelligent Radio Communication Interface. ESPRIT (Ref. 2/20. 1989). CDMA Testbed (CODIT) (R2020, 1992–1995); Advanced TDMA (ATDMA) (R2084, 1992–1995).
- Mobile Integrated Communications in Construction, MICC (AC088, 1996–1998).
- Radio Access INdependent Broadband on Wireless, RAINBOW (AC015, 1996–1998).
- COST: Evolution of Land Mobile (Including Personal) Communications (1989–1996).

[5] http://www.ac.upc.es/ccaba

Optical Communications Group

This research group is part of the Signal Theory and Communications Department. The key research lines of the Optical Communications Group are related with Photonic Technologies and High–Speed Networking, with results on Optical transmission at high bit rates (SDH at 2.5 Gbps), multigigabit sources and receivers, access techniques (such as CDMA Management and control methods for photonic networks), optical wavelength domain transport networks (WDM, HDWDM, SCM) including wavelength stabilizing and monitoring, transparent optical network architectures based on wavelength routing and reuse, and add/drop multiplexers, and operation, administration and maintenance (OAM) for optical networks in accordance to telecommunication management network (TMN).

Main researchers: Gabriel Junyent Giralt and Jesus Roldan.

Participation in European R&D projects:

- Integrated Opto–Electronics towards the Coherent Multichannel IBCN (R1027, 1988–90).
- Management of Photonic Systems and Networks, MEPHISTO (AC209, 1996–1999).
- Management of Optical Networks, MOON (AC231, 1996–1998).

Equipment

The laboratory is equipped with an ATM LAN with the following basic components: an ATM switch, an Ethernet–ATM hub, and a FDDI and CBR (E1 and E3) to ATM adapter (AFTER). The switch is a ForeSystems–ASX200BX equipped with ten 155 Mbit/s ATM/STM–1 ports (8 multimode and 2 singlemode). The Ethernet–ATM hub (Fore Systems PowerHub 6000) has four 10 Mb/s Ethernet ports and one ATM/STM–1 multimode port. The AFTER equipment is a prototype developed in one of the projects of the Spanish Broadband Program (PLANBA) and it includes two constant–bit–rate ports (2 and 34 Mbit/s), an additional FDDI port (DAS) and one ATM/STM–1 multimode port. An ATM/SDH traffic analyzer (HP 75000 Broadband Series Test System) completes the basic equipment. It includes the ATM traffic generator module, the AAL analyzer module with an interface at 155 Mbps. The laboratory has several Sun workstations with ATM cards (Fore SBA–200E). Also, the laboratory provides with different multimedia equipment, such as, video boards and cameras. Furthermore, the UPC has an ATM backbone used for interconnecting all the LANs of the Campus and different auditoriums for distributed presentations within the Campus. The laboratory is linked to the European ATM Pilot network (JAMES) through the ATM node in Barcelona of the Telefónica ATM network (GIGACOM) by means of a single–mode fiber–optic access.

Currently this platform is capable of providing the following communication services: ATM native user–network–interfaces on multimode fibres using STM1/ATM interfaces at 155.52 Mbit/s; ATM access through Classical IP (RFC1577) and Fore IP; ATM Forum based LAN Emulation (V.: 1.0) on top of ATM; Interconnection of LANs through ATM, giving support to 802.3 and FDDI. Also, it includes SMDS services; Circuit Emulation through ATM at 2 Mbit/s and 34 Mbit/s; N–ISDN Basic Access; Multicast IP services. Mbone access (tunneling facilities); and Internet Access.

In the next future the platform will provide also these services: Upgraded Ethernet / ATM hub; Network Management Tool for integrated management of all the equipment; ATM native user–network–interfaces on UTP5; ISDN Primary Access; ATM traffic generation equipment with MPEG analyzer module; Computer network access through mobile terminals (DECT); and IPv6 routing facilities when commercially available.

The Spanish National Host

The idea of "National Host" arose as part of the Fourth General Plan for Research and Development of the European Union, within the sub–program of "Advanced Communications Technologies

and Services" (ACTS). The purpose of these "National Hosts" is to link and coordinate the activities and pilot networks that already exist in each country in the field of networks and services based on advanced broadband communications, with a view to make them available for ACTS projects. This would permit experimentation with advanced communication services designed to incorporate the end users, a basic aspect of programs such as ACTS. In Spain, the National Host was set up in 1994 under the guidance of the Spanish Administration. The Spanish National Host (SNH) comprises five organizations that offer their resources (equipment, technical staff, auditoriums, etc.) to research and development projects in the field of advanced communications (ACTS, for example), generally implying the participation of end users. Each partner in the SNH contributes with resources that belong to its own specific NH communications platform. Taken together, these platforms build up the complete infrastructure of the SNH.

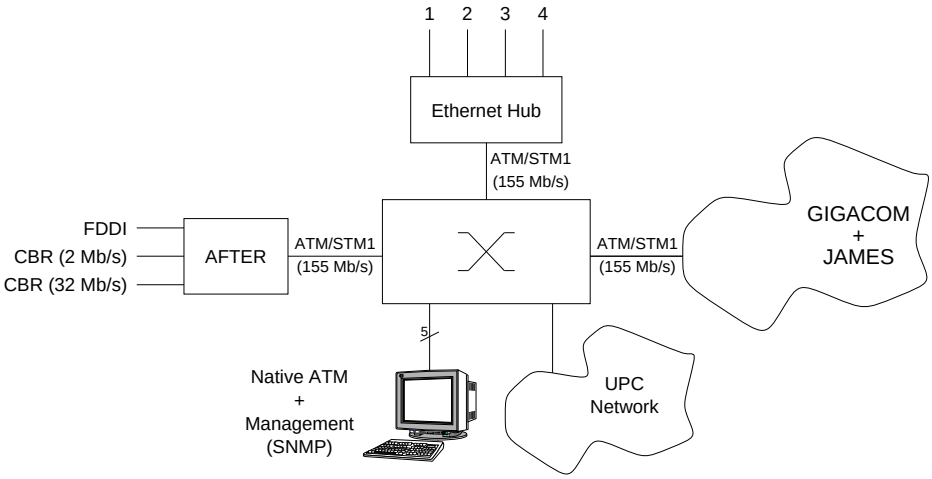
The cost for the service provided by the platform of the UPC, like all the other SNH platforms, consists of three quantities: an amount for using the resources, an amount for assistance of qualified personal and the amount for the usage of the connection. The later depending on the contracted peak rate and time duration of the connection according to GIGACOM tariffs. Connectivity services provided by National Hosts may be used by companies involved in research projects.

Spanish National Host Services
Technically, the NHs provide facilities only for supporting of ACTS projects, but in practice the facilities are open for almost any organization which plans to develop or enhance broadband oriented applications, providing that such usage is not for short–term commercial gain. The NH services will particularly facilitate the involvement in research programs by Small to Medium Enterprises (SMEs). Such participation is consistent with the stated aims of the European Commission, as it is felt that maximum creativity will be achieved by having research consortia composed of a mix of small and large organizations.

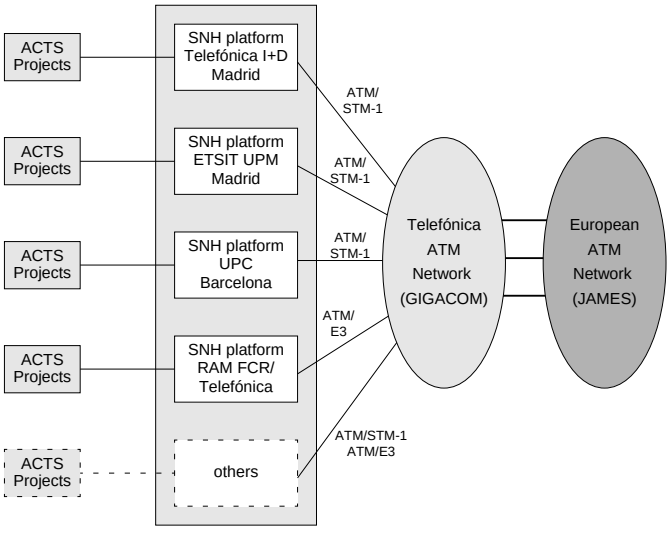
The cost for the service provided by the platform of the UPC, like all the other SNH platforms, consists of three items, namely cost for using the resources, cost for assistance of qualified personal and cost for the usage of the connection. The later depends on the contracted peak rate and time duration of the connection.

Services Provided

Spanish National Host Service. ACTS and TELEMATICS projects rely on National Hosts to perform the trials and experiments. Videoconferencing services over ATM. Support for distributed conferences is offered. Conference halls within the UPC Campus are interconnected by an ATM backbone network. Multimedia applications over ATM are demonstrated. Consulting services on ATM technologies and broadband communications. Postgraduate and training courses on broadband technologies and applications.



CCABA Laboratory Equipment



Structure of the SNH

Chapter 7

Available Technical Reports

In this chapter we present the list of available technical reports of the Computer Architecture Department. These reports are available via WWW in "http://www.ac.upc.es". They are also available via anonymous ftp on "ftp.ac.upc.es".

7.1 1996 DAC Reports

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