# Current Flow Controlling Hybrid DC Circuit Breaker

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***Abstract*—This paper proposes a new device by combining features of interline dual H-bridge current flow controller with the core idea of hybrid HVDC circuit breaker for meshed HVDC grid application. The proposed device can substitute 2 dc circuit breakers at a dc bus with at least 2 adjacent transmission lines. In addition to the current interruption action, the current in one of the adjacent lines can be controlled by the embedded current flow controller. The system level behavior of the proposed current flow controlling hybrid dc circuit breaker is similar to that of typical hybrid dc circuit breaker and the interline dual H-bridge current flow controller. The operation principles of the proposed device are introduced and analyzed in this work. The components ratings are compared to the existing solution and the functionality of proposed device is verified by simulation.**

***Index Terms*—DC Circuit Breaker, Meshed dc Grid, Fault Protection, Current Flow Controller.**

## I. Introduction

DC power transmission technology was revived since the middle of twenties century by realization of the first dc cable link between mainland Sweden and Gotland island in 1953 [1], [2]. Recent advances in the converters technology and the need for transmitting bulk amount of electrical energy over long distances have brought about the HVDC technology as a cost-efficient and reliable solution [2]. Nowadays, multi-terminal HVDC (MT-HVDC) grid concept is widely considered by both academia and industry due to the increasing demand for collecting the offshore wind energy [1]. While MT-HVDC grid offers several advantages, its operation faces a few drawbacks. The MT-HVDC gird protection against dc short circuit fault has been identified as the major difficulty due to inability of most of the VSC topologies in blocking the dc fault current [2]–[4]. Even for VSC technologies able to block the fault current (employing full bridge cells), there is a need to use additional protective devices when complex MT-HVDC grids with more than one protection zones are considered [1]. Moreover, the interruption of dc current is technically difficult due to the lack of natural zero crossing [5], [6]. In addition to the protection problem, a meshed HVDC (M-HVDC) grid as a complex form of the MT-HVDC grid may face power flow control problems. Typically, the power flow in the M-HVDC grid is controlled by regulating the converters' dc side voltage considering the transmission line impedance. Due to the M-HVDC grid topology, there are multiple paths for the current to circulate between two different nodes. Consequently, some of the transmission lines can be overloaded because of their lower impedances [7].

The research leading to these results has received funding from the People Programme (Marie Curie Actions) of the European Unions Seventh Framework Programme (FP7/2007-2013) under REA grant n° 317221.

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Over the last decade, the dc current interruption problem has been addressed by the introduction of several dc circuit breaker (DCCB) topologies [5], [8]–[11]. Among the proposed devices, the hybrid dc circuit breaker (HCB) merges the fast turn-off feature of semiconductor switches with the low-loss performance of metallic contacts and hence is technically highly attractive [12], [13]. The HCB requires hundreds of semiconductor switches in its main breaker (MB) branch to tolerate the system voltage [14], [15], hence its implementation cost is expected to be high. The number of required semiconductor switches for protection of a dc bus with two adjacent lines would be comparable to that of a modular multilevel converter (MMC) station [14].
Furthermore, several current flow controller (CFC) devices have been introduced to solve the power flow problem in M-HVDC grid [16]–[21]. The series CFCs demonstrate less power losses and reduced cost due to their lower voltage requirement and hence the fewer number of switches. The interline dual H-bridge CFC with reduced number of switches can be considered as one of the most efficient CFCs [18].
The coordinated operation of HCBs and CFCs is expectable in the future M-HVDC grids. As an alternative solution, this paper proposes a new device, which benefits from the core idea of typical HCB [12] and possesses an embedded CFC [18] and therefore can be named as current flow controlling circuit breaker (CFCCB). The CFCCB has three ports and can connect a dc bus to two adjacent transmission lines. The CFCCB can regulate the current in one of the adjacent lines and upon receiving a trip command can interrupt the fault current and isolate the faulty line from the dc bus. The proposed approach requires fewer number of semiconductor switches as compared to the typical approach. Moreover, the ratings of required surge arresters in DCCB part can be reduced remarkably by employing the proposed device.
This paper is organized as follows: the CFCCB topology and operation principles are detailed in section II. The case study model is explained in section III and section IV provides the analysis of CFCCB operation. The simulation results are presented and discussed in section V. A comparison between the typical approach and the proposed CFCCB is included in section VI and the paper is concluded in section VII.

### A. CFCCB topology

The topology of proposed CFCCB is shown in Fig. 1. The CFCCB has three terminals and can connect a dc bus to two adjacent transmission lines.

## II. Current Flow Controlling dc Circuit Breaker

The CFCCB consists of main breaker ($MB_i$) units, ultra fast disconnectors ($UFD_i$), surge arresters ($SA_i$), disconnectors ($DS_i$), seven semiconductor valves and one capacitor. Moreover

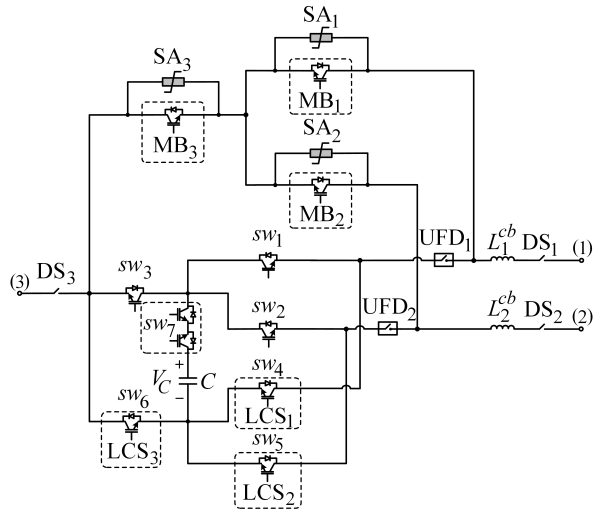


Fig. 1. Current flow controlling dc circuit breaker topology

($L_1^{cb}$) and ($L_2^{cb}$) are employed as current limiting inductors. The MB units consist of several semiconductor switches with antiparallel diodes in series connection. The semiconductor switches are connected in one direction and hence the MB units are unidirectional. $\text{UFD}_1$-$\text{UFD}_3$ are assumed to be similar to the UFDs in typical HCB [12]. $\text{DS}_1$-$\text{DS}_3$ are standard high voltage disconnectors to provide the electrical isolation after CFCCB action. As shown in Fig. 1, $\text{sw}_1$-$\text{sw}_6$ together with capacitor $C$ form an interline dual H-bridge CFC with reduced number of switches [18]. However, $\text{sw}_4$-$\text{sw}_6$ are also exploited as load commutation switches (LCSs). Therefore, $\text{sw}_4$-$\text{sw}_6$ are also referred as $\text{LCS}_1$-$\text{LCS}_3$ in this paper.

### A. Operation principles

*1) CFC bypassed mode:* In this mode, the CFCCB does not control the current and only maintain the power flow between the dc bus and the adjacent lines. The equivalent representation of CFCCB in the CFC bypassed mode is depicted in Fig. 2(a). Note that the semiconductor switches are represented by ideal switches in Fig. 2. In this mode, $\text{sw}_1$-$\text{sw}_3$ and $\text{sw}_7$ are opened whereas $\text{sw}_4$-$\text{sw}_6$ are closed. $\text{DS}_1$-$\text{DS}_3$ and $\text{UFD}_1$-$\text{UFD}_2$ are closed while $\text{MB}_1$-$\text{MB}_3$ are opened. It can be seen in the figure, the current can flow between the terminals of CFCCB irrespective of its direction.

*2) Active CFC mode:* The equivalent representation of CFCCB in the active CFC mode is depicted in Fig. 2(b). In this mode the CFCCB controls the current in one of the adjacent lines by operating its embedded dual H-bridge CFC. Depending on the current direction, the desired voltage can be generated by selecting a suitable set of states of switches. Table I illustrates the switching states for both negative and positive currents. The capacitor voltage is represented by $V$ in Table I. The current can be controlled using a PI and second order compensator. The linearized average model of the CFC represented by a couple of voltage sources can be used to design the current control system [7]. The embedded CFC operation modes and control scheme have been extensively investigated in [18] and [7]. As shown in Fig. 2, $i_1$, $i_2$ and $i_3$ are the currents flowing through terminal 1, 2 and 3 of CFCCB, respectively. Based on the switching states in Table I, $i_2$ can be controlled only by applying PWM signal to $\text{sw}_6$ assuming the following scenario:

- $i_3$ is incoming current into the CFCCB and $i_2$ and $i_1$ are outgoing currents.
- The currents are positive.

TABLE I
SWITCHING STATES FOR POSITIVE AND NEGATIVE CURRENT SCENARIOS [7]

| **Positive Curents** | | | | | |
|---|---|---|---|---|---|
| **Set** | $\mathbf{sw_1}$ | $\mathbf{sw_6}$ | $\mathbf{sw_2}$ | $\boldsymbol{V_31}$ | $\boldsymbol{V_32}$ |
| **1** | 0 | 0 | 0 | $-V$ | $-V$ |
| **2** | 0 | 0 | 1 | $-V$ | 0 |
| **3** | 0 | 1 | 0 | 0 | $-V$ |
| **4** | 0 | 1 | 1 | 0 | 0 |
| **5** | 1 | 0 | 0 | 0 | 0 |
| **6** | 1 | 0 | 1 | 0 | $+V$ |
| **7** | 1 | 1 | 0 | $+V$ | 0 |
| **8** | 1 | 1 | 1 | $+V$ | $+V$ |
| **Negative Curents** | | | | | |
| **Set** | $\mathbf{sw_3}$ | $\mathbf{sw_4}$ | $\mathbf{sw_5}$ | $\boldsymbol{V_31}$ | $\boldsymbol{V_32}$ |
| **9** | 0 | 0 | 0 | $+V$ | $+V$ |
| **10** | 0 | 0 | 1 | $+V$ | 0 |
| **11** | 0 | 1 | 0 | 0 | $+V$ |
| **12** | 0 | 1 | 1 | 0 | 0 |
| **13** | 1 | 0 | 0 | 0 | 0 |
| **14** | 1 | 0 | 1 | 0 | $-V$ |
| **15** | 1 | 1 | 0 | $-V$ | 0 |
| **16** | 1 | 1 | 1 | $-V$ | $-V$ |

*3) Fault mode:* The CFCCB can receive three independent trip commands including two line faults and one dc bus fault trip commands. Upon receiving a trip command the corresponding terminal(s) of CFCCB must interrupt(s) its(their) current(s). Note that the CFCCB may enter to the fault mode either when it operates in the CFC bypassed or in the active CFC modes.

*a) Fault on adjacent transmission line:* Assume a permanent short circuit fault happens on the line connected to the terminal 1 of CFCCB. Hence the terminal 1 of CFCCB should trip and interrupt the fault current. It is assumed that the fault incepts at time $t_f$ and the trip command is received by the CFCCB at time $t_1$. At time $t_1$, $\text{sw}_1$-$\text{sw}_3$ should be opened and consequently $\text{sw}_4$-$\text{sw}_6$ must be closed at time $t_2$. This action redirects the fault current path into the LCS units and prevents the capacitor from charging or discharging by reducing its current to zero. Thereafter $\text{sw}_7$ can be opened at time $t_3$ in zero current to ensure that the capacitor is disconnected from the system. Upon opening of $\text{sw}_7$, $\text{MB}_1$-$\text{MB}_3$ must be closed at time $t_4$. The equivalent representation of this stage is shown in Fig. 2(c). As can be seen in the figure, the fault current is shared between MB and LCS units. At time $t_5$, $\text{sw}_4$-$\text{sw}_6$ should be opened and commutate the current into the MB units. At this stage, the current in UFD units is almost zero. Therefore, $\text{UFD}_1$ can be opened at time $t_6$ in order to isolate the terminal 1 of CFCCB (Faulty line corresponding terminal) from the dc bus and the other adjacent line. Consequently, $\text{sw}_4$-$\text{sw}_6$ should be closed at time $t_7$. Fig. 2(d) shows the equivalent representation of CFCCB at time $t_7$. Note that, the current cannot flow through $\text{LCS}_1$ due to the open state of $\text{UFD}_1$. Finally, $\text{MB}_1$-$\text{MB}_3$ opens and redirect the currents into the $\text{SA}_1$-$\text{SA}_3$ at $t_{br}$. The time period between $t_7$ and $t_{br}$ is named as current sharing stage. The current in $\text{SA}_1$ will be zero due to the conduction of antiparallel diodes of $\text{MB}_1$. Fig. 3 illustrates the sequential operation of CFCCB in the line fault mode. The operation sequence for a fault on the line connected to terminal 2 of CFCCB is similar to the explained case. However, in the latter scenario $\text{UFD}_2$ must be opened instead of $\text{UFD}_1$. To provide the electrical isolation,

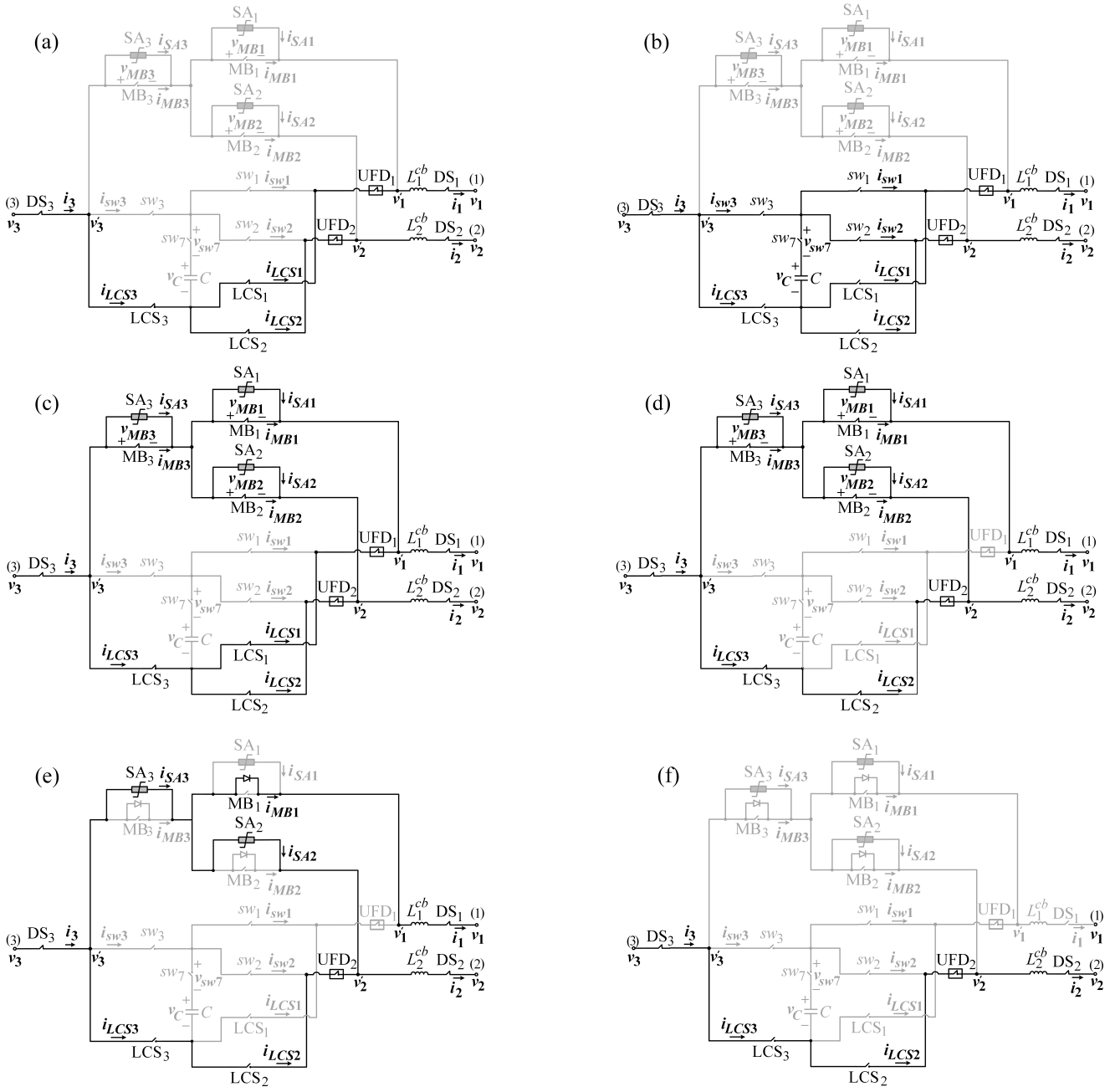


Fig. 2. Operation stages of current flow controlling hybrid dc circuit breaker

the corresponding terminal disconnector (DS) can be opened.

*b) Fault at dc bus:* Upon detection of a permanent dc bus fault, all adjacent lines must be isolated from the dc bus. The operation sequence for a bus fault interruption is illustrated in Fig. 3. As it is shown in the figure, the operation sequences for line and bus faults are the same until time $t_5$. To interrupt a dc bus fault, it is necessary to open both $\text{UFD}_1$ and $\text{UFD}_2$ at time $t_6$. For the bus fault interruption there is no current sharing stage and $\text{MB}_1$-$\text{MB}_3$ can be directly opened at time $t_{br}$ to interrupt the fault current and redirect it into the surge arresters. Note that the current in $\text{SA}_3$ will be zero due the conduction of the antiparallel diodes of $\text{MB}_3$. The bus fault current interruption is expected to be faster than the line fault scenario due to the lack of current sharing stage. Finally, the electrical isolation can be provided by opening $\text{DS}_1-\text{DS}_3$.

*c) Recloser mode:* The recloser mode might be required before completely opening of the CFCCB. The CFCCB can be reclosed by reclosing $\text{MB}_1$-$\text{MB}_3$ after opening the faulty line corresponding UFD. The equivalent circuits of reclosing mode are equal to Fig. 2(d) and (f). Finally, in case of a non-permanent fault, the faulty line corresponding UFD can be again closed and the CFCCB shifts to its normal conduction state by closing $\text{sw}_4$-$\text{sw}_6$ and opening $\text{MB}_1$-$\text{MB}_3$.

## III. Case Study Model

The current interruption operation of CFCCB does not depend on the grid topology. Therefore, an average model

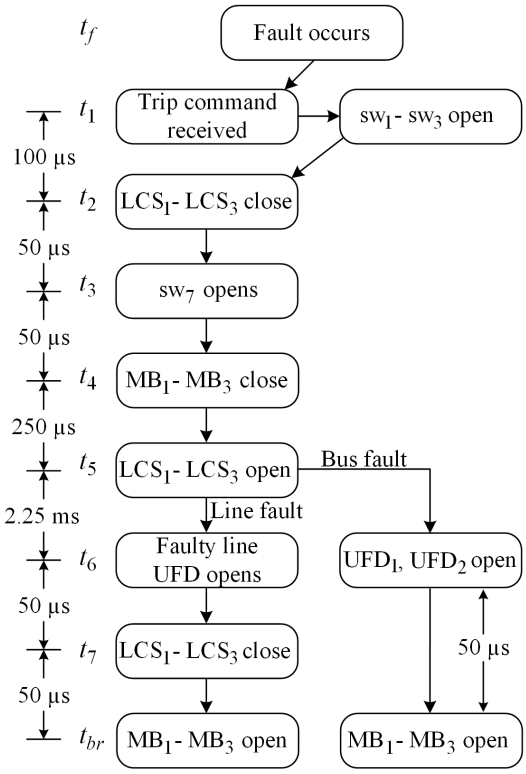


Fig. 3. Line and bus faults isolation process

of a three-terminal meshed grid is selected for performing the analysis and simulation. The three-terminal grid model is shown in Fig. 4. The transmission lines are modeled using lumped T-equivalent model. The parameters of test system are illustrated in Table V. The analysis and simulations are carried out for both proposed and typical schemes. As illustrated in Fig. 4, in the typical scheme, a CFC is installed at bus $B_1$ to regulate the current in line 12. In addition, two HCBs are installed between two adjacent lines (12 and 13) and the CFC. In this study, the HCBs from [12] are considered. A detailed schematic of the HCB is illustrated in Fig. 5. In the proposed scheme, the CFC and the HCBs are substituted by the CFCCB (see Fig. 4). The CFC control system is designed based on [7] for both typical and proposed schemes. The parameters of CFC are the same for both mentioned schemes and are illustrated in Table V.

## IV. Analysis

The operation of embedded CFC has been analyzed in [7], [18]. Therefore, only the current interruption mode of CFCCB is considered in this section. In order to clarify the differences between the proposed and the typical methods the analysis is simplified by considering the following aspects:

- The permanent dc fault and prompt fault interruption strategy are considered [15], [22].
- Voltage at dc buses are assumed to be constant during the DCCB operation time [23].
- Transmission line and dc bus short circuit faults are modeled by a voltage source, whose value is equal to the system steady-state voltage value in normal condition and it changes to 0 V as soon as a fault happens.

Considering the aforementioned assumptions, the grid model can be simplified by eliminating the connection between buses $B_2$ and $B_3$. The simplification can be done due to

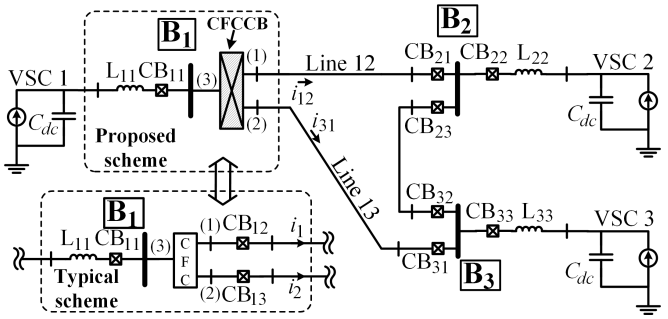


Fig. 4. Average model of three-terminal grid

assumed constant dc bus voltage during the fault condition. The simplified model for analysis is depicted in Fig. 5.

### A. Impact of the embedded CFC on the fault current

The embedded CFC is composed of six switches with their antiparallel diodes and one bidirectional switch. Due to arrangement of the switches and the capacitor, the CFC cannot block the fault current until the capacitor is charged up to the nominal line voltage. The voltage rating of the capacitor lies in the range of few kilo volts. Therefore, the CFC capacitor must be disconnected from the fault current path to prevent it from being charged or discharged. The capacitor can be retained by opening $sw_1$-$sw_3$ while closing $sw_4$-$sw_6$ and then opening $sw_7$. Considering the embedded CFC structure, it can be found out that all the switching states may only change the fault current path inside the CFC and the fault current may charge or discharge the capacitor. Hence, during the fault clearing time period (which lies in range of few milliseconds) the CFC has almost no impact on the fault current. When $0 < t \leq t_2$, the current flows through $sw_1$-$sw_7$ depending on their state. Therefore considering the scope of paper the analysis considers the current equations for $t_2 < t \leq t_{br}$.

### B. Transmission line fault $F_1$ and CFCCB

A low impedance ($R_{fault} \approx 0\ \Omega$) pole-to-ground fault occurs on line 12 at point $F_1$ at $t = 0$ s. The voltage at fault location ($v_{F1}$) becomes zero after fault occurs. The following equations can be given considering the initial conditions and assumptions:

$$\begin{aligned} &v_{F1}(0) = V_{dc}, \\ &v_{F1}(0^+) = 0, \\ &v_j(t) = V_{dc}; \quad 0 < t \leq t_{br}, \quad j = 1,2,3, \\ &i_j(0) = I_{pre,j}; \quad j = 1,2,3. \end{aligned} \tag{1}$$

In (1) $v_{F1}(t)$, $v_j(t)$ and $I_{pre,j}$ represent the voltage at fault location, dc bus $B_j$ voltage and pre-fault current of port $j$ of the CFCCB. $t_{br}$ represents the current interruption instant. The current at port 3 can be given as follows:

$$i_3(t) = \begin{cases} i_{LCS3}(t), & t_2 < t \leq t_5 \\ i_{MB3}(t), & t_5 < t \leq t_7 \\ i_{MB3}(t) + i_{LCS3}(t), & t_7 < t \leq t_{br} \\ i_{SA3}(t) + i_{LCS3}(t), & t_{br} < t \leq t_e \end{cases}, \tag{2}$$

and for port 1:

$$i_1(t) = \begin{cases} i_{LCS1}(t), & t_2 < t \leq t_5 \\ i_{MB1}(t), & t_5 < t \leq t_7 \\ i_{MB1}(t), & t_7 < t \leq t_{br} \\ i_{MB1}(t), & t_{br} < t \leq t_e \end{cases}, \tag{3}$$

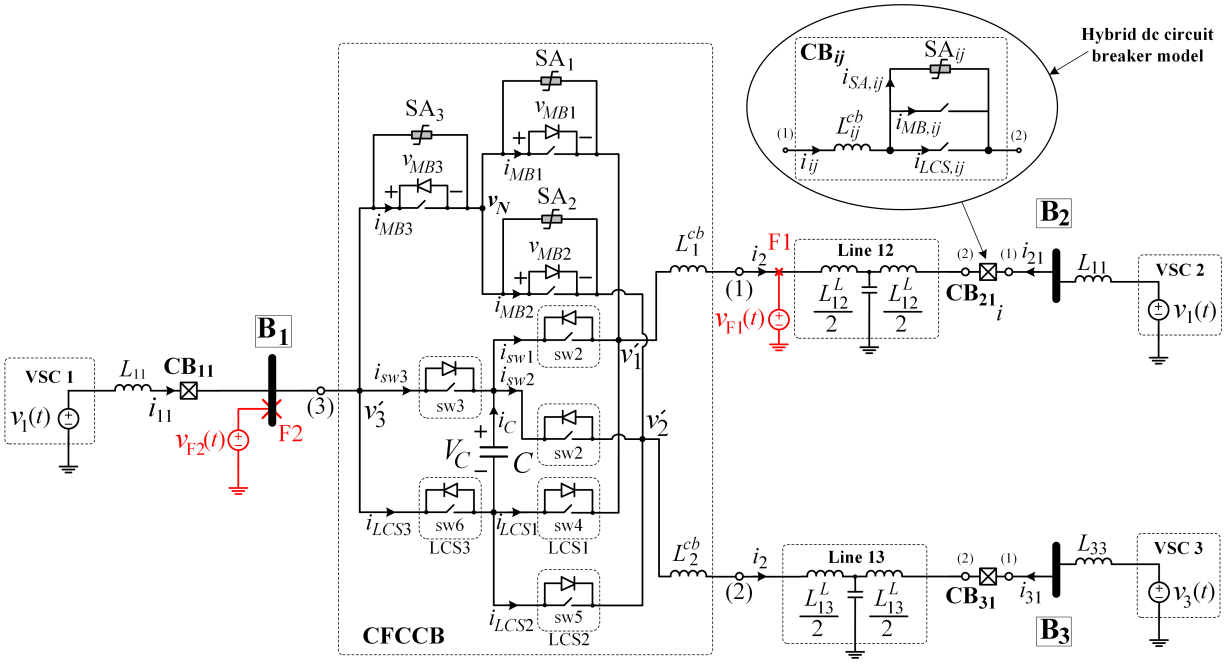


Fig. 5. Equivalent circuit of test system in presence of CFCCB

and for port 2:

$$i_2(t)=\begin{cases} i_{LCS2}(t), & t_2<t\le t_5 \\ i_{MB2}(t), & t_5<t\le t_7 \\ i_{MB2}(t)+i_{LCS2}(t), & t_7<t\le t_{br} \\ i_{SA2}(t)+i_{LCS2}(t), & t_{br}<t\le t_e \end{cases}. \quad (4)$$

We replace the sum of half of line $1j$ inductance ($L^L_{1j}$) and corresponding port current limiting inductor value ($L^{cb}_{j-1}$) by $L'_{1j}$:

$$L'_{1j}=L^{cb}_{j-1}+\frac{1}{2}L^L_{1j} \quad for \quad j=1,2$$
$$L'_{11}=L_{11}+L^{cb}_{11}. \quad (5)$$

Therefore, considering the impact of transmission line lumped T-equivalent model capacitance during the short fault clearing time period, the initial rate of rise of current at port 1, which is equal to that of fault current can be given by:

$$\frac{\mathrm{d}i_1(0^+)}{\mathrm{d}t}=\frac{V_{dc}}{\left((L'_{11}\,\|\,L'_{13})+L^{cb}_1+L^f_{12}\right)} \quad (6)$$

where $L^f_{12}$ represents the inductance between the CFCCB and the fault location. The current derivative at the other ports of CFCCB can be given as:

$$\left|\frac{\mathrm{d}i_2(0^+)}{\mathrm{d}t}\right|=\frac{L'_{11}}{(L'_{11}+L'_{13})}\left|\frac{\mathrm{d}i_1(0^+)}{\mathrm{d}t}\right|,$$
$$\left|\frac{\mathrm{d}i_3(0^+)}{\mathrm{d}t}\right|=\frac{L'_{13}}{(L'_{11}+L'_{13})}\left|\frac{\mathrm{d}i_1(0^+)}{\mathrm{d}t}\right|. \quad (7)$$

The current in MB and LCS units can be obtained using (2)-(4), (6) and (7).

*1) Main breaker (MB) units:* When $t_4<t<t_{br}$ MB$_1$-MB$_3$ are closed. Therefore, assuming instantaneous current commutation at $t=t_5$ the current in MB$_1$ can be given as:

$$i_{MB1}(t)=I_{pre,1}+\left|\frac{\mathrm{d}i_1(0^+)}{\mathrm{d}t}\right|t \quad (8)$$

The maximum current in MB$_1$ ($I^{MB1}_{max}$) happens at $t=t_{br}$. The current in MB$_2$ and MB$_3$ when $t_4<t<t_7$ can be given by:

$$i_{MBi}(t)=I_{pre,i}+sgn(i-2.5)\left|\frac{\mathrm{d}i_i(0^+)}{\mathrm{d}t}\right|t; \quad i=2,3. \quad (9)$$

The maximum current in MB$_2$ and MB$_3$ is reached at $t=t_7$. When $t_7<t<t_{br}$, the current is shared between two mentioned MBs and their current will be decreased.

*2) Load commutation switch (LCS) units:* As was explained, the LCS switches conduct the current in two periods of time: i) $t_2<t<t_5$ ii) $t_7<t<t_{br}$. In the first stage (when $t_2<t<t_5$), the current in LCS$_j$ for $j=1$ and for $j=2,3$ holds the same equations as (8) and (9), respectively. The maximum current in the first stage in the LCS units happens at $t=t_5$. The second maximum of current in the LCS units occurs at time $t_{br}$. Fig. 2(d) shows the equivalent circuit of the CFCCB when $t_5<t\le t_{br}$. The MBs have several IGBTs in series whereas the LCSs have only few IGBTs. The on-state voltage drop on an MB can be hundred times larger than the on-state voltage drop of an LCS. Hence, the voltage drop on the LCSs can be neglected against that of MB units. Therefore, the following equation can be given considering Fig. 2(d):

$$v'_2\approx v'_3 \quad (10)$$

$v'_1$-$v'_3$ are illustrated in Fig. 2. Based on (10), MB$_2$, MB$_3$ can be considered as parallel branches during the mentioned time period and their currents will be almost equal. The absolute value of current in MB$_j$ at $t=t_7^+$ can be given by:

$$\left|i_{MBj}(t_7^+)\right|=\frac{\left|i_{MB3}(t_7^-)\right|+\left|i_{MB2}(t_7^-)\right|}{2}; \quad j=2,3 \quad (11)$$

Using (2), the current in LCS$_n$ can be given as follows:

$$i_{LCS3}(t_7^+)=i_{LCS1}(t_7^+)=\frac{\left|i_{MB3}(t_7^-)\right|-\left|i_{MB2}(t_7^-)\right|}{2} \quad (12)$$

The time $t_{br}-t_7$ lies in the range of tens of microseconds. However, using the obtained current derivative in (6), the second maximum of current in LCS$_j$ for $j=2,3$ can be obtained as:

$$I^{LCSj}_{max2}=i_{LCSj}(t_7^+)+\frac{\mathrm{d}i_1(0^+)}{\mathrm{d}t}\cdot\frac{t_{br}-t_7}{2} \quad (13)$$

*3) Surge arresters (SA):* Surge arresters have a non-linear voltage-current characteristic. Only for comparison purposes, SA's parameters are approximated by assuming its voltage to

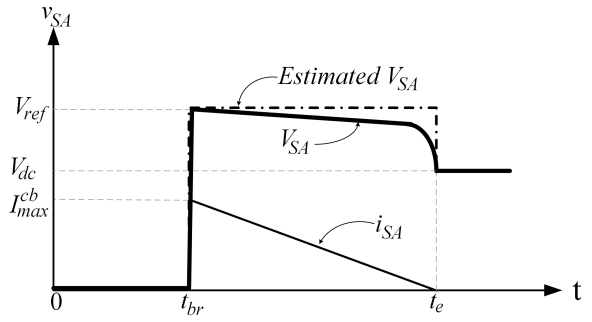


Fig. 6. Surge arrester approximated current and voltage

be constant until its current falls to zero for both proposed and typical schemes. Fig. 6 illustrates the voltage and current approximation method used for the SAs. It is assumed that the SA current reaches its maximum instantaneously and then decreases linearly. This method is used to identify the maximum possible energy absorption in the surge arresters. Neglecting the practical mismatch between $V-I$ characteristics of surge arresters, the current can be given as:

$$\begin{aligned} |i_{SAj}| &= \left|\frac{i_{MB1}}{2}\right|; \quad j=2,3 \\ |i_{SA1}| &= 0, \end{aligned} \tag{14}$$

The current in $SA_1$ is zero due to the conduction of antiparallel diodes in $MB_1$. Considering (10) it can be assumed that $SA_2$ and $SA_3$ operate in parallel connection. The rated voltage of each surge arrester is assumed to be equal to $V_r$. The transient interruption voltage ($TIV$) across $MB_2$ and $MB_3$ can be given by:

$$TIV = V_{dc} + \left((L'_{11} \parallel L'_{13}) + L_1^{cb} + L_{12}^{f}\right)\frac{I_{max}^{MB1}}{t_e - t_{br}} \tag{15}$$

The current in SA reaches zero when its voltage falls below its rated voltage. The maximum required time for SA current to fall to zero ($t_e - t_{br}$) can be given as:

$$(t_e - t_{br}) \le \left((L'_{11} \parallel L'_{13}) + L_1^{cb} + L_{12}^{f}\right)\frac{I_{max}^{MB1}}{V_r - V_{dc}}, \tag{16}$$

The maximum absorbed energy in all the surge arresters holds:

$$E_{SA,T} = \int_{t_{br}}^{t_e} V_r \cdot i_1(t)dt \tag{17}$$

Consequently, the maximum absorbed energy in $SA_j$ can be given as:

$$\begin{aligned} E_{SAj} &= \frac{V_r I_{max}^{MB1}(t_e - t_{br})}{4}; \quad j=2,3, \\ E_{SA1} &= 0. \end{aligned} \tag{18}$$

### C. DC bus fault $F_2$ and CFCCB

As shown in Fig. 5, a low impedance pole-to-ground fault ($R_{fault} \approx 0\ \Omega$) occurs at dc bus $B_1$ at time 0 s. The initial conditions and study assumptions are similar to (1) and also similar approach to subsection IV-B is used for analysis. The current at port $j$ for various time periods can be given by:

$$i_j(t) = \begin{cases} i_{LCSj}(t), & t_2 < t \le t_5 \\ i_{MBj}(t), & t_5 < t \le t_{br} \\ i_{SAj}(t), & t_{br} < t \le t_e \end{cases}; \quad j=1,2,3 \tag{19}$$

The current derivative at ports of CFCCB can be given by:

$$\begin{aligned} \frac{\mathrm{d}i_3(0^+)}{\mathrm{d}t} &= V_{dc}\frac{L'_{12}+L'_{13}}{L'_{12}L'_{13}}, \\ \left|\frac{\mathrm{d}i_i(0^+)}{\mathrm{d}t}\right| &= \frac{V_{dc}}{L'_{1(i+1)}}; \quad i=1,2. \end{aligned} \tag{20}$$

*1) Main breaker (MB) units:* The currents in MB units when $t_5 < t \le t_{br}$ can be given as:

$$i_{MBi}(t) = \begin{cases} I_{pre,i} - \frac{V_{dc}}{L'_{1(i+1)}}t; & i=1,2 \\ I_{pre,i} - V_{dc}\frac{L'_{12}+L'_{13}}{L'_{12}L'_{13}}t; & i=3 \end{cases} \tag{21}$$

The maximum current in $MB_j$ ($I_{max}^{MBj}$) is reached at $t = t_{br}$.

*2) Load commutation switch (LCS) units:* Despite the line fault scenario, the current in LCS units has one maximum at $t = t_5$ and can be given as:

$$I_{max}^{LCSi}(t) = \begin{cases} I_{pre,i} - \frac{V_{dc}}{L'_{1(i+1)}}t_5; & i=1,2 \\ I_{pre,i} - V_{dc}\frac{L'_{12}+L'_{13}}{L'_{12}L'_{13}}t_5; & i=3 \end{cases} \tag{22}$$

*3) Surge arresters (SA):* The SA current can be given as:

$$\begin{aligned} |i_{SAj}| &= \left|\frac{i_{MB3}}{2}\right|, \quad j=1,2 \\ |i_{SA3}| &= 0. \end{aligned} \tag{23}$$

Depending on the length of adjacent lines, the absorbed energy in the surge arresters of the CFCCB and also the energy absorption time ($t_{ej} - t_{br}$) can be different for each surge arrester. The range of energy absorption time can be given as:

$$t_{ej} - t_{br} \le \frac{L'_{1(j+1)} I_{max}^{MBj}}{V_r - V_{dc}}, \quad j=1,2 \tag{24}$$

where $t_{ej}$ is the time when the current in $SA_j$ becomes zero. Due to conduction of antiparallel diode $D_3$, the current in $SA_3$ remains zero and consequently the absorbed energy in $SA_3$ is also zero. The absorbed energy in $SA_j$ can be given by:

$$E_{SAj} = \frac{V_r I_{max}^{MBj}(t_{ej} - t_{br})}{2}, \quad j=1,2 \tag{25}$$

### D. Typical scheme

In the typical scheme, after receiving a trip command by the corresponding HCB at time $t_1$, its MB unit is closed. Thereafter, the LCS unit opens at time $t_2$ and consequently MB unit opens at time $t_3$ [24]. Similar line and bus fault scenarios to subsection IV-B to subsections IV-B and IV-C are considered. For sake of brevity, only the most relevant equations are included in this section.

*1) Transmission line fault and HCB:*

*a) Load commutation switch (LCS) units:* The LCS current in $CB_{12}$ reaches its maximum at $t = t_2$ whereas the current in LCS unit of $CB_{13}$ reaches its maximum at $t = t_{br}$. The maximum current in LCS unit of $CB_{12}$ can be given by:

$$I_{max}^{LCS12}(t) = I_{pre,12} + \left|\frac{\mathrm{d}i_{12}(0^+)}{\mathrm{d}t}\right| t_2 \tag{26}$$

and for LCS unit of $CB_{13}$:

$$I_{max}^{LCS13}(t) = I_{pre,13} - \left|\frac{\mathrm{d}i_{13}(0^+)}{\mathrm{d}t}\right| t_{br} \tag{27}$$

*b) Main breaker (MB) units:* It is assumed that only the MB unit of corresponding HCB of the faulty line is activated. Therefore, the current in MB units of other HCBs remain zero. The current in MB unit of $CB_{12}$ for $t_2 < t \le t_{br}$ can be given as:

$$I_{max}^{MB12}(t) = I_{pre,12} + \left|\frac{\mathrm{d}i_{12}(0^+)}{\mathrm{d}t}\right| t \tag{28}$$

The maximum current in the MB unit in $CB_{12}$ ($I_{max}^{MB12}$) is reached at time $t_{br}$.

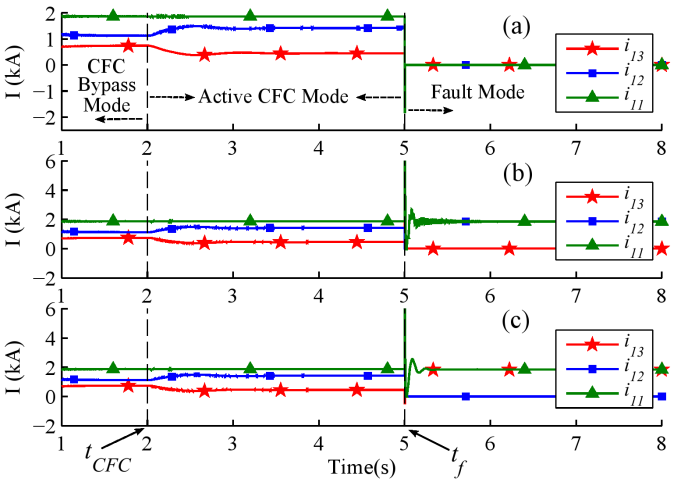


Fig. 7. Transmission lines and dc bus currents during fault at: a) dc bus $B_1$, b) line 13, c) line 12

*c) Surge arresters (SA):* The currents in surge arresters of all the HCBs are zero except the faulty line HCB ($SA_{12}$). The absorbed energy in the surge arrester can be given by:

$$E_{SA12}=\frac{V_r I_{max}^{MB12}(t_e-t_{br})}{2} \tag{29}$$

*2) DC bus fault and HCB:*

*a) Load commutation switch (LCS) units:* During the bus fault, all the adjacent HCBs of the faulty dc bus are activated. The maximum current in the LCS unit of all adjacent HCBs ($I_{max}^{LCS1i}$) can be given as:

$$I_{max}^{LCS1i}=I_{pre,1i}-\frac{V_{dc}}{L'_{1i}}t_2;\quad i=2,3 \tag{30}$$

*b) Main breaker (MB) units:* The currents of MB units for $t_2<t\leq t_{br}$ can be given as:

$$i_{MB1i}(t)=I_{pre,1i}-\frac{V_{dc}}{L'_{1i}}t;\quad i=2,3 \tag{31}$$

The maximum current in the MB unit ($I_{max}^{MB1i}$) is reached at $t=t_{br}$.

*c) Surge arresters (SA):* The absorbed energy in $SA_{1j}$ can be given by (32).

$$E_{SA1j}=V_r I_{max}^{MB1j}(t_{ej}-t_{br}),\quad j=2,3 \tag{32}$$

## V. Simulation Results

In this section the simulation results of the three-terminal grid (Fig. 4) for line 12 and dc bus fault scenarios are presented and compared to the obtained numerical values from the analysis of simplified grid model in section IV. The simulations are carried out using PSCAD. The non-linear $V-I$ characteristic of surge arresters are also considered. The transmission lines are protected by standard overcurrent protection scheme. The line fault trip command is sent to the CFCCB or the corresponding HCB when the line current exceeds 2.8 kA. The dc buses are protected by the differential protection scheme. In this scheme, when the sum of incoming and outgoing currents at a dc bus becomes non-zero, the dc bus trip signal is activated.

*1) Power flow:* The currents flowing from the dc bus and the transmission lines in presence of the CFCCB are depicted in Fig. 7. Fig. 7(a), (b) and (c) depict the currents for dc bus $B_1$, line 13 and 12 fault scenarios, respectively. The CFCCB operates in CFC bypassed mode for $0<t<2$ s. Thereafter the CFCCB changes its operation mode to active CFC mode at time $t_{CFC}=2$ s. In all scenarios, the fault happens at time $t_f=5$ s. The behavior of CFCCB has been found out to be similar to the typical scheme during normal operation and fault condition from the grid point of view.

*2) Transmission line Fault:* To consider the most sever scenario, a low impedance pole-to-ground fault (100 mΩ) is placed very close to the CFCCB (distance from CFCCB is equal to 0 km.) on line 12 at $t=0$ s. In the typical approach $CB_{12}$ and $CB_{21}$ and in case of the proposed CFCCB, $CB_{21}$ and port 1 of the CFCCB should trip. Fig. 8 and Fig. 9 show different waveforms for the proposed and typical schemes, respectively. The important numerical values obtained from simulation and analysis are also illustrated in Table II. The interrupted current in the CFCCB is almost 5% larger than the interrupted current in the typical scheme due to the additional time that is considered in the modeling of current sharing stage in the CFCCB. As shown in Fig. 8(b) and Fig. 9(b), the current in $sw_1$-$sw_3$ in both schemes are almost equal. However, a large difference in the current of $sw_4$-$sw_6$ can be observed in Fig. 8(c) and Fig. 9(c). The absolute value of current in $sw_4$ and $sw_6$ in the typical scheme reaches almost 10 kA whereas in $sw_5$ and $sw_6$ in the proposed scheme does not exceed 5 kA. Fig. 8(d) depicts the CFCCB capacitor voltage and current and also the voltage across $sw_7$. The absolute value of voltage across $sw_7$ does not exceed 2.5 kV. As shown in Fig. 8(f) and Fig. 9(f), the fault current is redirected into two surge arresters ($SA_2$ and $SA_3$) in CFCCB whereas it is handled by one surge arrester in the typical method. Since the rated voltage of surge arresters in CFCCB are equal to that of HCBs, the maximum voltage across MB units in both methods are equal (Fig. 8(g) and Fig. 9(g)). Fig. 8(h) and Fig. 9(h) show the absorbed energy in the surge arresters in both methods. The amount of absorbed energy in each surge arrester in the CFCCB reaches almost 7.2 MJ whereas it reaches approximately 14 MJ in the typical scheme. The results confirm that the absorbed energy in the surge arrester in the typical scheme is almost equal to twice the absorbed energy in each surge arrester in the proposed scheme.

*3) DC bus Fault:* A low impedance pole-to-ground fault (100 mΩ) is placed at bus $B_1$. In the typical scheme $CB_{11}$, $CB_{12}$ and $CB_{13}$ and in the proposed scheme $CB_{33}$ and all the ports of CFCCB should trip. Fig. 10 and 11 depict the results for the proposed and the typical schemes, respectively. The most relevant numerical values obtained from analysis and simulation are illustrated in Table III. The obtained approximated values from analysis are close to the values obtained from simulation. Fig. 10(a) and 11(a) show that the behavior of both schemes from system point of view are similar. As can be seen in Fig. 10(b) and 11(b) the current in $sw_1$-$sw_3$ for both schemes are equal. Fig. 10(c) and 11(c) show that the current in $sw_4$-$sw_6$ in the typical scheme may reach higher values as compared to the proposed scheme. The maximum current in $MB_{12}$ and $MB_1$ and also in $MB_{13}$ and $MB_2$ are equal (see Fig. 10(e) and 11(e)). The absolute value of current in $MB_3$ of CFCCB reaches almost 1.8 kA, which is higher than the current in MB units of $CB_{12}$ and $CB_{13}$. However, this does not necessarily mean that the antiparallel diodes of $MB_3$ should to be rated for higher current than the antiparallel diodes of $MB_1$ and $MB_2$. In fact, $MB_1$ and $MB_2$ may be required to carry higher currents during a line fault and should be rated for that. Fig. 10(f) and 11(f) illustrate that the maximum current in the surge arresters of both schemes are equal. In contrary with $MB_1$ and $MB_2$, the current in $MB_3$ does not redirected to the surge

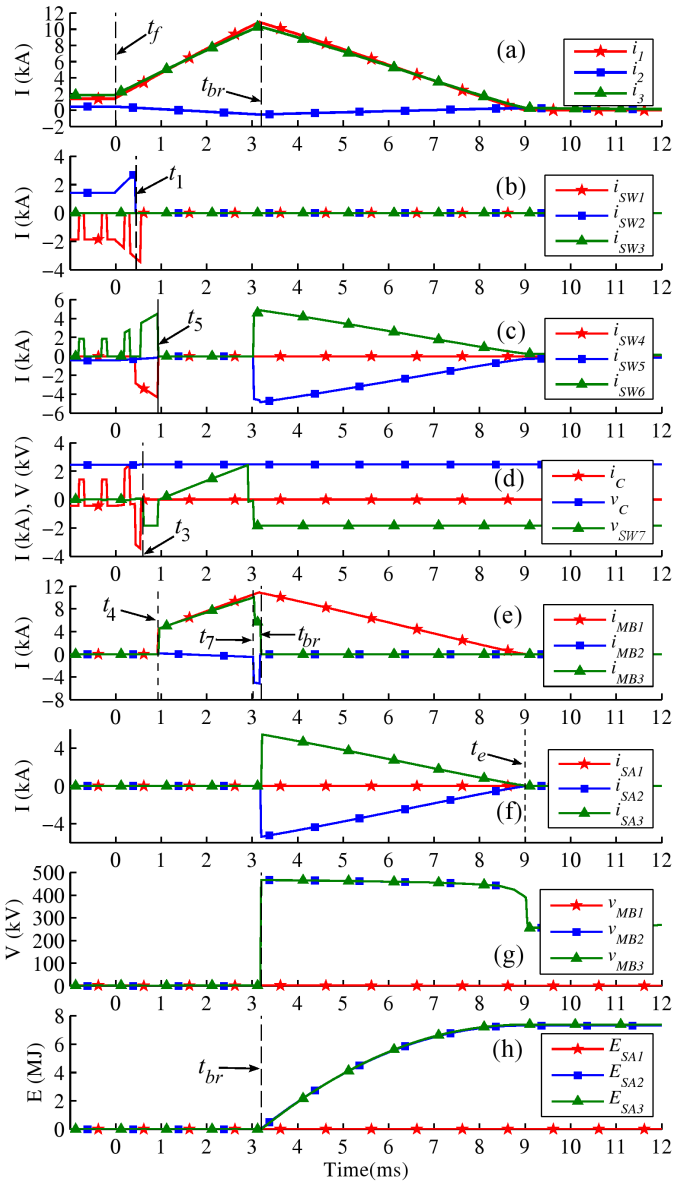


Fig. 8. CFCCB waveforms for fault on line 12

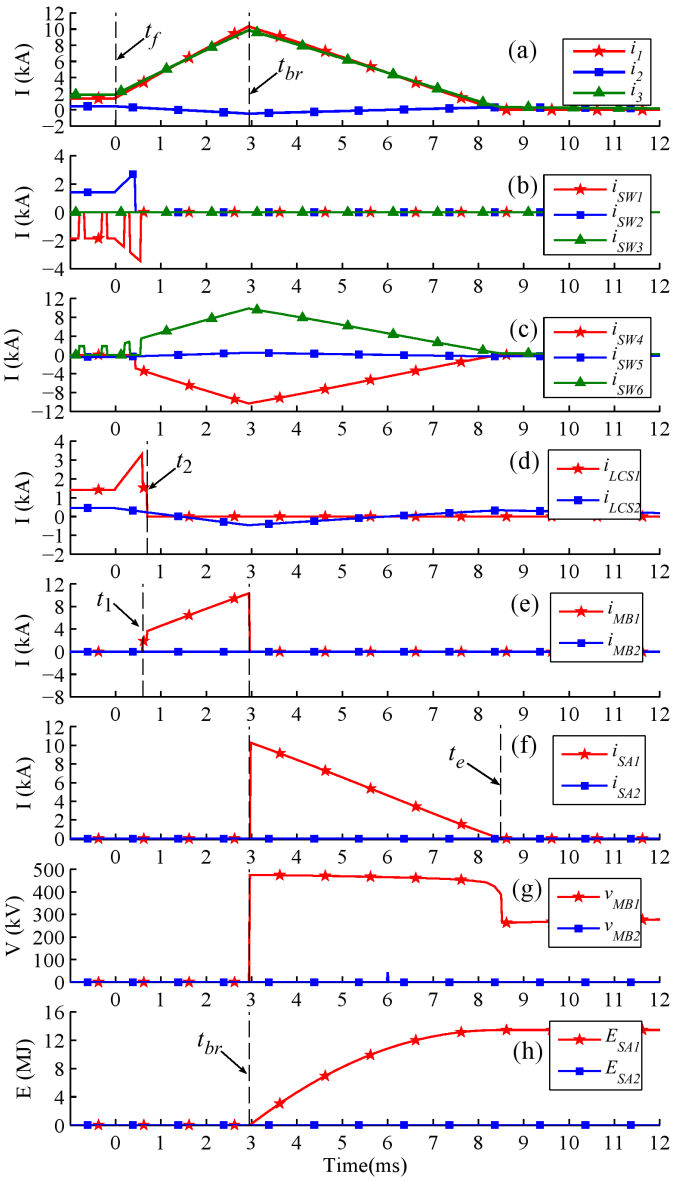


Fig. 9. Typical scheme waveforms for fault on line 12

TABLE II
CFCCB AND HCB PARAMETERS DURING LINE FAULT

| Parameters | CFCCB | | HCB | |
|---|---|---|---|---|
| CFCCB (HCB) | Analysis | Simulation | Analysis | Simulation |
| $I_{max1}^{LCS1}(I_{max}^{LCS12})$ [kA] | 4.18 | 4.28 | 3.20 | 3.28 |
| $I_{max2}^{LCS1}$[kA] | 4.48 | 4.62 | - | - |
| $I_{max}^{MB1}(I_{max}^{MB12})$[kA] | 11.10 | 10.9 | 10.43 | 10.33 |
| $E_{SA1}(E_{SA12})$[MJ] | 0 | 0 | 16.98 | 13.69 |
| $E_{SA2}(E_{SA13})$[MJ] | 8.99 | 7.31 | 0 | 0 |
| $E_{SA3}$[MJ] | 8.99 | 7.38 | - | - |

arrester due to explained reason in section IV. The absorbed energy in the surge arresters in the CFCCB and the typical scheme are depicted in Fig. 10(h) and 11(h), respectively.

## VI. COMPARISON

The proposed scheme is compared to the typical scheme in this section. As shown in Fig. 4, to fully protect a dc bus with 2 adjacent lines and one converter station with an asymmetric monopole HVDC configuration, 3 HCBs are required in the typical scheme. The number of HCBs can be doubled in symmetric monopole and bipole configurations. Although the comparison study is done for asymmetric monopole configuration, it is valid for other mentioned configurations. The HCBs and the CFC can be replaced by the CFCCB. The converter station HCB ($CB_{11}$) will not be removed. Therefore, the requirements of $CB_{11}$ in both cases are equal and will not be compared and included in calculations. Table IV compares different aspects of both the proposed and typical devices assuming $t_6 \approx t_{br}$.

*1) CFC:* The CFC can be bypassed during the fault either by the explained method in IV-A or using bypass valves. Considering the method from IV-A $sw_4$-$sw_6$ are required to carry the fault current till the corresponding HCBs interrupt the fault (at time $t_{br}$). In contrary, the same switches in the embedded CFC of CFCCB are only required to carry the fault current till the the LCS units are opened (at time $t_5$). In addition, $sw_4$-$sw_6$ are closed at time $t_7$ and share the fault current with the MB units in the line fault scenario. Comparing (30) and (13) imply that $sw_4$-$sw_6$ should be rated for higher current in the typical scheme than the proposed scheme.

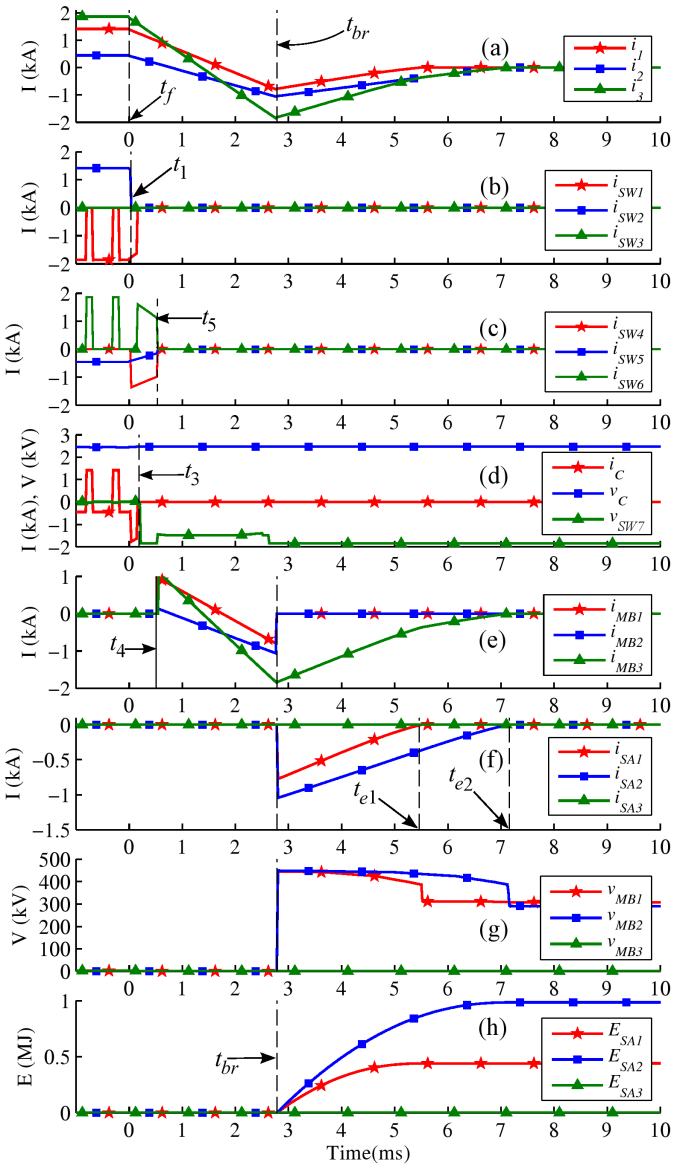


Fig. 10. CFCCB waveforms for fault at bus $B_1$

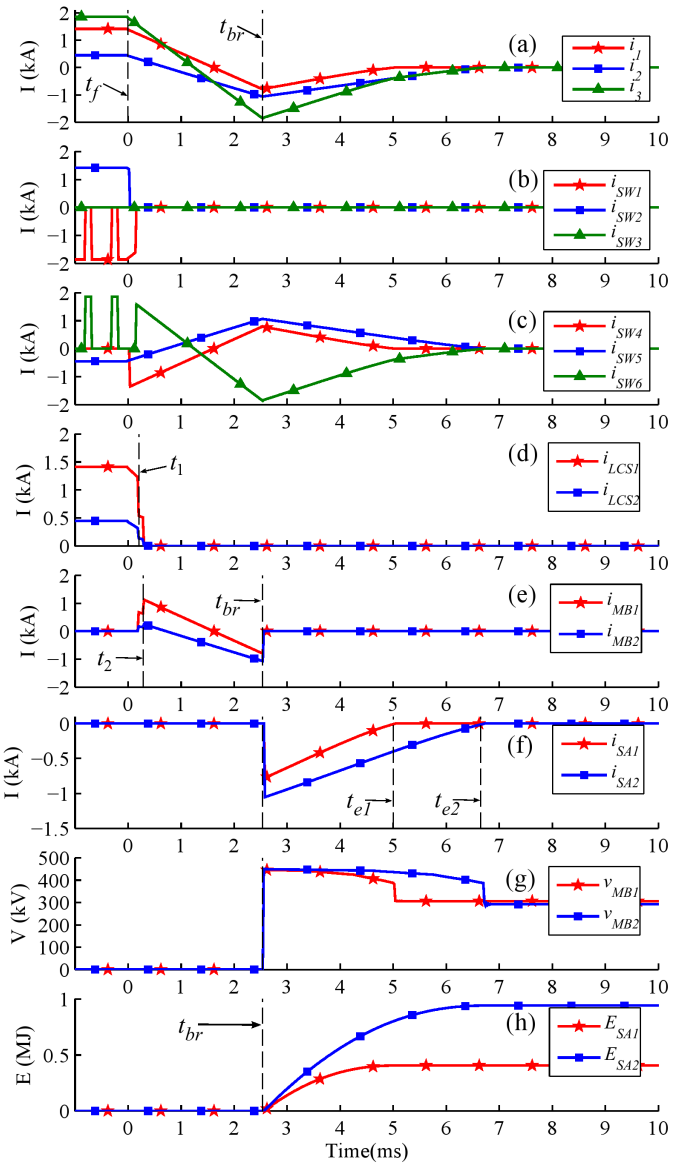


Fig. 11. Typical scheme waveforms for fault at bus $B_1$

TABLE III
CFCCB AND HCB PARAMETERS DURING BUS FAULT

| Parameters | CFCCB | | HCB | |
|---|---|---|---|---|
| CFCCB (HCB) | Analysis | Simulation | Analysis | Simulation |
| $I_{max}^{LCS1}(I_{max}^{LCS12})$ [kA] | -0.96 | -0.98 | -1.19 | -1.24 |
| $I_{max}^{LCS2}(I_{max}^{LCS13})$ [kA] | -0.133 | -1.151 | -0.29 | -0.33 |
| $I_{max}^{LCS3}$ (-) [kA] | -1.103 | -1.13 | - | - |
| $I_{max}^{MB1}(I_{max}^{MB12})$ [kA] | -0.933 | -0.81 | -0.75 | -0.78 |
| $I_{max}^{MB2}(I_{max}^{MB13})$ [kA] | -1.19 | -1.056 | -1.059 | -1.06 |
| $I_{max}^{MB3}$ (-) [kA] | -2.12 | -1.84 | - | - |
| $E_{SA1}(E_{SA12})$ [MJ] | 0.534 | 0.442 | 0.452 | 0.406 |
| $E_{SA2}(E_{SA13})$ [MJ] | 1.249 | 0.995 | 1.056 | 0.941 |
| $E_{SA3}$ [MJ] | 0 | 0 | - | - |

TABLE IV
CFCCB AND HCB BASED METHODS PARAMETER COMPARISON

| Parameter | HCB | CFCCB |
|---|---|---|
| Number of UFDs | 2 | 2 |
| Number of limiting ind. | 2 | 2 |
| Number of surge arresters | 2 | 3 |
| Surge arresters energy | $E$ | $\frac{E}{2}$ |
| Surge arresters voltage | $V_r$ | $\frac{V_r}{2}$ |
| Number of IGBTs in LCS | $2N_{LCS}$ | 0 |
| Number of IGBTs in MB | $\frac{4V_r}{V_{CES}}$ | $\frac{3V_r}{V_{CES}}$ |

### A. Load commutation switches

The CFCCB uses $sw_4$-$sw_6$ of the embedded CFC as the LCSs. In fact, CFCCB saves all the IGBTs, which are required for implementing the LCS units ($N_{LCS}$) in the HCBs. The maximum current in LCS unit of $HCB_{1j}$ is equal to the first maximum current in $LCS_j$ of CFCCB for the line fault scenario. Depending on the grid topology, the second maximum current in LCS units of CFCCB might be greater as compared to the typical HCB. During the dc bus fault condition the current in $LCS_2$ and $LCS_3$ of CFCCB are equal to the current in LCS units of $HCB_{11}$ to $HCB_{12}$. The current in $LCS_1$ is equal to sum of currents in $LCS_2$ and $LCS_3$ of CFCCB and therefore is higher than the currents in other units. Note that the current in $LCS_1$ flows through its antiparallel diodes during the bus fault. Hence, the current rating of the IGBTs are equal.

### B. Main breaker units

During the line fault the current in corresponding MB units of the CFCCB and HCB are equal. Similar to the previous subsection, the antiparallel diodes of $MB_1$ in CFCCB may need to be able to carry higher current as compared to the other units depending on the fault identification time and the grid topology. As it is illustrated in Table IV the typical approach requires larger number of IGBTs in MB units of HCBs as compared to the proposed CFCCB. $V_{CES}$ represents the collector-emitter blocking voltage of IGBTs in Table IV.

### C. Surge arresters

*1) Rated voltage:* The rated voltage for the surge arrester of the HCB would lie in range of $1.4V_{dc}-1.5V_{dc}$ [13], [14]. The rated voltage of surge arresters of CFCCB are also assumed to lie in the same range.

*2) Discharge current:* (14) illustrates that the maximum discharge current in the surge arresters of the CFCCB in line fault scenario is almost half of the fault current at the interruption instance. However, the maximum discharge current in the surge arrester in typical HCB is almost equal to the interrupted current. Therefore, the maximum discharge current in the surge arresters of the CFCCB is almost 50% smaller than that of the typical scheme.

*3) Energy:*

*a) Transmission line Fault:* In the typical scheme and during the line fault, only the faulty line HCB interrupts the current and its surge arrester absorbs the energy. When using the CFCCB the faulted line corresponding surge arrester does not absorb the energy and the energy absorption is shared between 2 surge arresters. Using (18) and (29) and assuming identical current at the interruption instant in both schemes the ratio of total absorbed energy in both schemes can be given as:

$$\frac{E_{SA,T}^{CFCCB}}{E_{SA,T}^{HCB}}=\frac{1}{2} \tag{33}$$

where $E_{SA,T}^{CFCCB}$ and $E_{SA,T}^{HCB}$ represents the total absorbed energy in the surge arresters of CFCCB and HCB, respectively. (33) implies that the energy rating of surge arresters in CFCCB is almost 50% smaller than that of HCB.

*b) DC bus Fault:* The CFCCB performance during the dc bus fault was found to be similar to the typical method. Therefore, equal amount of energy is absorbed in the surge arresters in both schemes.

### D. Ultra-fast disconnector

Each HCB has an ultra-fast disconnector (UFD). As shown in Fig. 1, the CFCCB has 2 UFDs. Therefore, there is no difference in number of required UFD units for both typical and the proposed schemes.

### E. Current limiting inductors

The number of current limiting inductors in both schemes are identical. Also, the inductances of current limiting inductors for the proposed and typical devices are equal.

## VII. Conclusion

In this paper, a novel current flow controlling dc circuit breaker (CFCCB) has been proposed and analyzed. The proposed CFCCB has three ports and can connect a dc bus to two adjacent transmission lines. Each port of the CFCCB can interrupt its current, independent of the other ports and irrespective of the current direction. Furthermore, the proposed device possesses an embedded interline dual H-bridge current flow controller (CFC), which can regulate the current in one of the adjacent transmission lines.

While the proposed device shows similar behavior compared to the typical scheme from the system level view, it can reduce the requirements of different elements of system. The analysis and simulations imply that the proposed CFCCB requires fewer IGBTs compared to the typical approach. For a dc bus with two adjacent transmission lines, CFCCB needs at least 25% fewer IGBTs as compared to the typical scheme. Moreover, the proposed device requires smaller size surge arresters due to the less energy absorption in its surge arresters. In addition, the maximum current discharge in the surge arresters in the proposed method is smaller that that of typical method. The results from this study confirm that the energy and discharge current ratings of the surge arresters can be reduced by almost 50%. Considering the improvements by applying the proposed device, its implementation cost is expected to be remarkably lower than the cost of typical scheme. The future work will concern with the cost-benefit and reliability studies of the proposed device.

## Appendix

TABLE V
THREE-TERMINAL TEST GRID AND CFC PARAMETERS

| **Transmission Lines Parameters** | | | |
|---|---|---|---|
| Lumped T-model Parameters | R [Ω/km] | L [mH/km] | C [$\mu$F/km] |
| | 0.01105 | 3.245 | 0.382 |
| Length [km] | Line 12 | Line 13 | Line 23 |
| | 200 | 300 | 200 |
| **VSC Parameters** | | | |
| Bus | **1** | **2** | **3** |
| Capacitance [$\mu$F] | 1000 | 1000 | 1000 |
| Power [MW] | 600 | - | - |
| $V_i^*$ [kV] | - | 300 | 300 |
| Droop Constant $k_i$ [A/V] | - | 0.05 | 0.5 |
| Voltage [kV] | 320 | 320 | 320 |
| Filter reactor [mH] | 10 | 10 | 10 |
| **CFC Parameters** | | | |
| Nominal Voltage [kV] | 4 | | |
| Capacitor [mF] | 10 | | |
| Switching Frequency [kHz] | 2 | | |
| PI | $0.012+\frac{0.398}{s}$ | | |
| Compensator | $\frac{0.3421s^2+1.2978s+21.5213}{s^2+120.5323s+3207.9071}$ | | |
| Filter | $\frac{1}{0.08s+1}$ | | |

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