Performance Analysis and Design Optimization of a Self-Powered Gate-Driver Supply Circuit

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***Abstract*- In this paper, the performance of a self-powered unipolar gate driver supply circuit for power devices is studied, with the aim of analyzing the viability of using such circuits in high voltage applications with discrete components. A simplified model of the circuit, capturing the essential features, is proposed, from which practical design guidelines are provided to optimize the overall circuit performance. These design guidelines allow a proper component selection that can result in significant improvements in the circuit performance. Experimental results of typical parameters characterizing the turn-on and turn-off transients, including the turn-on and turn-off energy loss, are provided for a wide range of current values and different gate resistances. The results are compared to those obtained using a conventional gate driver power supply.**

I. INTRODUCTION

In many power electronics applications, the topologies involved include a number of power switches. Each power switch requires a gate driver and the corresponding gate driver power supply (GDPS), in many cases with galvanic isolation. The conventional use of external GDPS (EGDPS) often involves small dc-dc power supplies with high-frequency transformers. These solutions present drawbacks such as finding an appropriate dc voltage source to extract the energy, the size of the circuits itself, or even electromagnetic compatibility issues, since the voltage of large conductor surfaces oscillates at high frequency with respect to ground, introducing common mode electromagnetic paths through the gate drive circuitry where significant current may flow, affecting its performance.

Bootstrap power supplies based on the charge pump concept are an alternative [1], [2]. But, again, an appropriate dc voltage source to extract the energy is needed. Additionally, there is no galvanic isolation between the high-power stage and the low-power dc voltage source, and these circuits introduce functionality limitations such as (in a half-bridge configuration): top-side switch GDPS is dependent on bottom-side switch control, no permanent on state of the top switch is possible, no permanent off state of the bottom switch is possible (both switches cannot be off permanently), and there is a minimum on time of the bottom switch to charge the top switch GDPS capacitance.

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Several self-powered supply circuits connected across the power switch overcoming the above limitations are proposed in the literature. In [3], for instance, a resonant circuit topology is employed. In [4]-[8], topologies that can be monolithically integrated within the main power switch are investigated. Fig. 1 presents one of such topologies. Metal-oxide semiconductor field-effect transistors (MOSFETs) of the same technology and voltage rating (600 V CoolMOS) are considered here as the main (S_m) and auxiliary (S_a) devices. Currently, no commercial power switch with an integrated GDPS circuit is available. Nowadays, a viable use of these circuits in most applications calls for a discrete component implementation. This paper investigates the performance of such circuit when implemented with discrete components, and its design optimization, to determine the feasibility of using it in high voltage applications.

The paper is organized as follows. Section II reviews the operation principle of the circuit. Section III presents the circuit design guidelines and design optimization, from the analysis of a simple model of the circuit. Section IV presents the analysis of the experimental performance of two proposed designs as compared to the performance of a conventional EGDPS. Finally, Section V outlines the conclusions.

II. GATE DRIVER POWER SUPPLY OPERATION PRINCIPLE

In the circuit of Fig. 1, capacitor C_s stores the energy necessary to power the main power switch S_m gate driver. When the current i_m is positive at the S_m turn-off transition, this energy is obtained from the energy that is otherwise lost during this transition. If i_m is not positive, the energy will be obtained from the dc voltage source connected across the switch during its off state, with a low conversion efficiency (equal to V_{Cs}/V_{dc}) for high dc-source voltages (V_{dc}). Thus, this

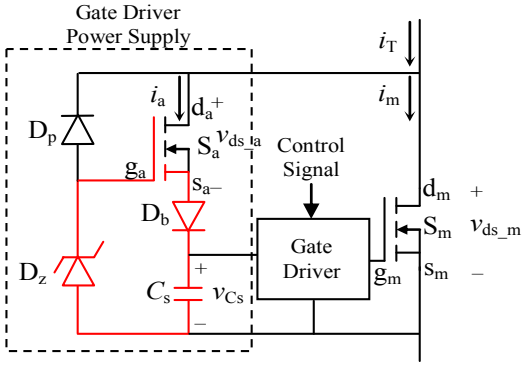

Fig. 1. Internal gate driver power supply (IGDPS) circuit.

circuit is especially interesting in applications with $i_m > 0$ at S_m turn-off. During the turn-off process, part of the current initially flowing through the main switch flows through the auxiliary switch S_a charging capacitor C_s. The zener diode D_z, polarized by diode D_p, limits the value of v_{Cs} and the blocking diode D_b prevents the discharging of C_s when S_m is on. In a discrete implementation of the GDPS circuit, it is convenient to replace D_p by a resistor R_p to better control the polarizing current thorough D_z.

S_m and S_a typically share the resulting turn-off loss.

III. CIRCUIT DESIGN

A. General Considerations

The performance of the selected circuit varies significantly depending on the component selection, especially in high voltage applications. The main goal is to achieve the capacitor C_s recharge as fast as possible during turn-off, while the main switch voltage v_{ds_m} is still low, to maximize the efficiency of the charging process.

The auxiliary device S_a is selected to be of the same device technology and voltage rating as S_m. At the beginning of the S_m turn-off transient, S_a turns-on mainly due to the current flowing through the parasitic capacitances C_{dg_a} and C_{gs_a}. Therefore, a high C_{dg_a}/C_{gs_a} ratio is desired, to avoid a significant increase of v_{ds_a} before the charging process begins. Alternatively, an external capacitor can be added to increase C_{dg_a}, but its value will be limited by the maximum effective output capacitance (across d_m and s_m) of the circuit in Fig. 1 for the application (this constraint is typical if zero voltage switching at turn-on is pursued). Switch S_a average current will be typically very low, since it is only conducting during the turn-off transients, although it may have to withstand a significant peak current during the charging process.

Diodes D_z and D_b, and capacitor C_s are low voltage components. It is desired that the zener current of D_z be as low as possible in order to minimize the losses in the polarization resistor R_p (replacing D_p in Fig. 1). A Schottky diode is a meaningful choice for D_b.

B. Auxiliary Circuit Model

The performance of the circuit is strongly dependent on the design of the red loop in Fig. 1. This loop can be modeled as a series RLC circuit with a diode, as shown in Fig. 2.

The variables in Fig. 2 are defined as

$$\begin{aligned} V_e &= V_z - V_{th\_Sa} - V_{th\_Db} \\ R_e &= 1/G_m + R_{Db} + R_{Cs} \\ L_e &= L_{Sa} + L_{Db} + L_{Cs} + L_{layout} \\ C_e &= C_s \end{aligned} \tag{1}$$

where V_z is the zener voltage, V_{th_Sa} is the gate-to-source conduction threshold voltage of S_a, V_{th_Db} is the conduction threshold voltage of D_b, G_m is the transconductance of S_a, R_{Db} is the equivalent series on resistance of D_b, R_{Cs} is the equivalent series resistance of C_s, L_{Sa} is the parasitic source inductance of S_a, L_{Db} is the parasitic inductance of D_b, L_{Cs} is the parasitic inductance of C_s, and L_{layout} is the loop parasitic inductance.

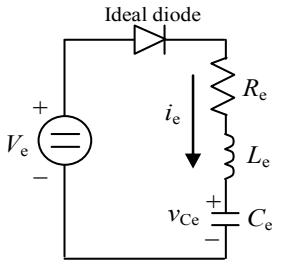

Fig. 2. Equivalent circuit of the red loop in Fig. 1.

The circuit in Fig. 2, omitting the diode, is governed by the second-order differential equation

$$i_e''(t) + \frac{R_e}{L_e} \cdot i_e'(t) + \frac{1}{L_e C_e} \cdot i_e(t) = 0. \tag{2}$$

with three possible solutions:

1) Overdamped solution ($\alpha > \omega_0$):

$$i_e(t) = A \cdot e^{\left[-\alpha+\sqrt{\alpha^2-\omega_0^2}\right]\cdot t} + B \cdot e^{\left[-\alpha-\sqrt{\alpha^2-\omega_0^2}\right]\cdot t}. \tag{3}$$

2) Critically damped solution ($\alpha = \omega_0$):

$$i_e(t) = (C + D \cdot t) \cdot e^{-\alpha \cdot t}. \tag{4}$$

3) Underdamped solution ($\alpha < \omega_0$):

$$i_e(t) = e^{-\alpha \cdot t} \cdot \left[E \cdot \sin(\omega_c \cdot t) + F \cdot \cos(\omega_c \cdot t)\right] \tag{5}$$

where

$$\alpha = R_e/(2L_e) \tag{6}$$

is the attenuation factor,

$$\omega_0 = 1/\sqrt{L_e \cdot C_e} \tag{7}$$

is the resonant frequency,

$$\omega_c = \sqrt{\omega_0^2 - \alpha^2}, \tag{8}$$

and A, B, C, D, E, F are constant values dependent on the boundary conditions.

The initial value of the charging current is $i_e(0) = 0$. The initial value of its first derivative is $i_e'(t) = [V_e - v_{Ce}(0)] / L_e$, where $v_{Ce}(0)$ is the value of v_{Cs} at the beginning of the turn-off process. In all three possible cases, $i_e(t)$ first increases and then falls towards zero. During this stage, since $i_e(t) \geq 0$, the solutions of (2) also describe the behavior of the circuit in Fig. 2, which includes an ideal diode.

As the channel of S_m closes, the portion of the current that can not flow through the S_m and S_a channels will flow through the parasitic capacitances of S_m and S_a, increasing voltages v_{ds_m} and v_{ds_a}, therefore decreasing the efficiency of the recharging process. Thus, it is desirable that the auxiliary circuit produces a recharge of the GDPS capacitor C_s as fast as possible.

C. Design Optimization

In order to avoid an exponential decay of the current at the end of the charging process, with small but positive values of the current when v_{ds_m} has already reached its off state value, therefore producing significant losses at S_a, especially in high voltage applications, it is better to operate the circuit in the underdamped mode. In this case, the current will quickly reach a zero value, defining the end of the recharging process.

The diode in Fig. 2 will then prevent the current from oscillating around zero as usual in the underdamped mode.

From (5)-(8), to produce an underdamped recharge process as fast as possible, it is clear that R_e and C_e must take a minimum value, therefore guaranteeing that $\alpha < \omega_0$ and maximizing the value of ω_c. An appropriate selection of S_a, D_b and capacitor C_s will produce a minimum value of R_e. To minimize the value of $C_e = C_s$, the maximum zener voltage value possible, defined by the maximum input voltage rating of the gate driver, will have to be selected. This is because

$$C_s = \frac{Q_g + Q_{loss}}{\Delta v_{Cs}} = \frac{Q_g + Q_{loss}}{V_z - V_{gs\_min}} \tag{9}$$

where Q_g is the gate charge of S_m, Q_{loss} is the charge lost in the gate driver, and V_{gs_min} is the minimum gate-to-source voltage of S_m in on state.

Fig. 3 shows the variation of ω_c as a function of L_e in a particular case (R_e = 250 mΩ, C_e = 22 nF). The curve presents a maximum at

$$L_{e\_op} = R_e^2 \cdot C_e/2; \quad \omega_{c\_op} = 1/(R_e \cdot C_e). \tag{10}$$

This is the optimum value of the equivalent inductance, from the point of view of recharging time, which will be typically much lower than the parasitic value in a discrete component implementation. Therefore, better performance should be expected from an implementation within a module or a monolithically integrated implementation.

In Fig. 4, the waveforms of i_e and v_{Ce} are plotted for several values of L_e. As can be seen, the duration of the charging process (period of time where $i_e > 0$) decreases as the value of L_e decreases. The minimum value is obtained for L_e = 1 nH. For lower values of inductance, the circuit enters into the overdamped mode, and i_e decays exponentially over a long period of time. This extended period where $i_e > 0$ will produce significant losses since v_{ds_m} will have reached its permanent off state value. On the other hand, it is interesting to note that in the underdamped condition, voltage v_{Ce} reaches a value beyond the threshold voltage for which S_a starts to conduct in the off state. This extra charge injected into C_e will allow to feed the gate driver during the off state with S_a off and therefore avoiding the low conversion efficiency of the recharging process at the S_m off state under high v_{ds} voltages. As it can be observed in Fig. 4, there is a tradeoff between the recharging time and the amount of extra charge injected; i.e., large values of L_e will lead to significant extra charge and long recharging times while small values of L_e will lead to short recharging times and small extra charge.

The duration of the charging process can be estimated as

$$T_{charge} = \pi/\omega_c \,[\mathrm{s}]. \tag{11}$$

In general, a good performance of the circuit (no increase in the turn-off losses compared to the EGDPS case) will be achieved roughly if T_{charge} is lower than the turn-off transition time (time for v_{ds_m} to rise plus time for i_m to fall) with an EGDPS at the maximum load current value. This is a conservative design guideline.

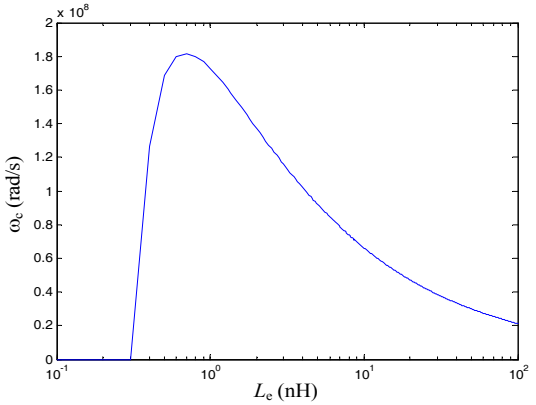

Fig. 3. Variation of ω_c as a function of L_e (R_e = 250 mΩ, C_e = 22 nF).

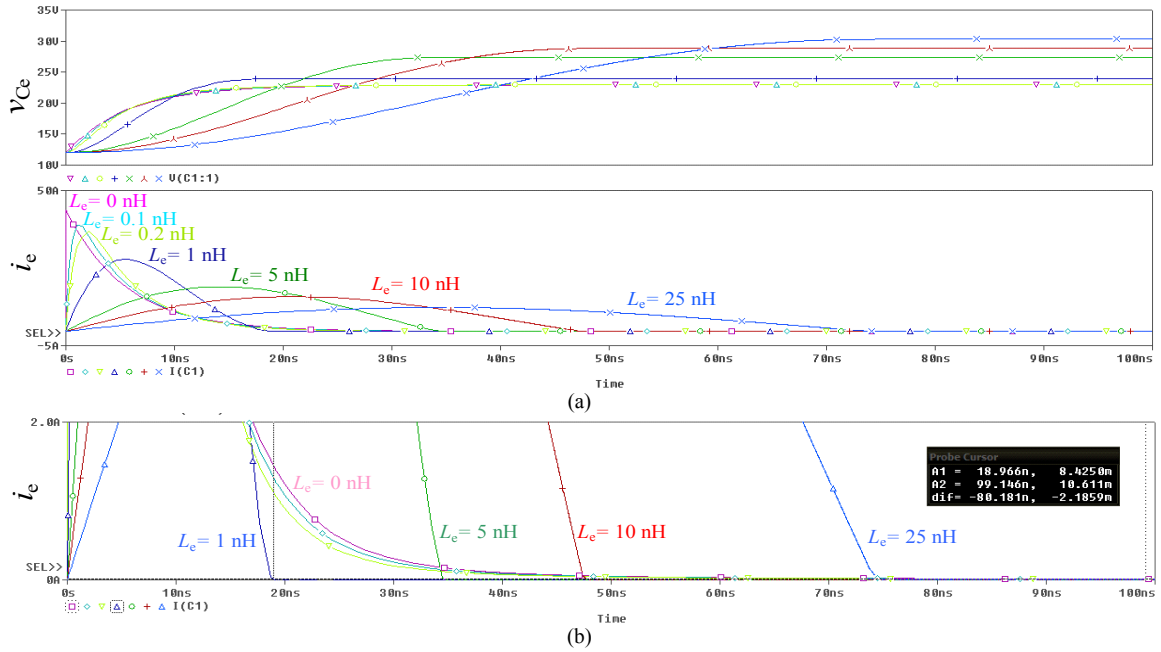

Fig. 4. Simulated i_e and v_{Ce} for V_e = 23 V, R_e = 250 mΩ, C_e = 22 nF, and different values of L_e. (a) Panoramic view. (b) Zoom view.

IV. EXPERIMENTAL RESULTS

The performance of the IGDPS circuits designed has been evaluated in the topology presented in Fig. 5. A 600 V, 46 A CoolMOS device is selected as the main power MOSFET. A 1200 V, 15 A SiC Schottky diode is connected across the boost inductor. The circuit is initially operated with a conventional EGDPS. The EGDPS generates a driving voltage V_s = 12 V. Then, the EGDPS is replaced by the IGDPS in Fig. 1 (replacing D_p by resistor R_p), and two possible designs are tested (IGDPS1 and IGDPS2). The components of these two designs are specified in Table I, and their equivalent circuit parameters are specified in Table II. Two values of the gate resistance are employed: R_g = 10 Ω and R_g = 5 Ω.

TABLE I
IGDPS COMPONENTS

Component	IGDPS1	IGDPS2
S_a	SPP04N60C3 (650 V, 4.5 A)	SPP011N60C3 (650 V, 11 A)
D_z	DDZ9705 (18 V @ 50 µA)	DDZ9711 (27 V @ 50 µA)
D_b	10BQ040 (40 V, 1 A)	V8P10 (100 V, 8A)
R_p	300 kΩ	300 kΩ
C_s	68 nF MKP	22 nF MKT

TABLE II
IGDPS PARAMETERS

Parameter	IGDPS1	IGDPS2
V_e	≈14 V	≈23 V
R_e	450 mΩ	250 mΩ
L_e	≈20 nH	≈20 nH
C_e	68 nF	22 nF
T_{charge}	127 ns	67 ns

Fig. 6 depicts a burst of switching transitions at low i_L current levels for both IGDPS designs. The GDPS capacitor voltage v_{Cs} decreases at turn-on to charge the gate of S_m and is recharged at turn-off. Voltage v_{Cs} oscillation is larger in the case of IGDPS2 (17 V versus 4 V, approximately), because a higher zener voltage and lower capacitance C_s have been selected. It is interesting to note that in the case of IGDPS1, and after the turn-off transition, v_{Cs} reaches a value lower than the value corresponding to a permanent off state (the initial value in Fig. 6(a)). This means that after the turn-off transition, capacitor C_s will continue to be charged through S_a, because it has not yet reached the final steady-state value. Since during this process $v_{ds\_m} = V_{dc}$, the efficiency of this final charge stage will be low, especially for high V_{dc} voltages. Instead, in the case of IGDPS2, at the end of the turn-off transition voltage v_{Cs} reaches a value higher than the initial. An extra charge is injected into C_s, that will allow powering the gate driver during the off state for a period of time before the polarizing branch of the circuit in Fig. 1 forces S_a to conduct a current to recharge C_s. This significantly improves the overall efficiency of the circuit.

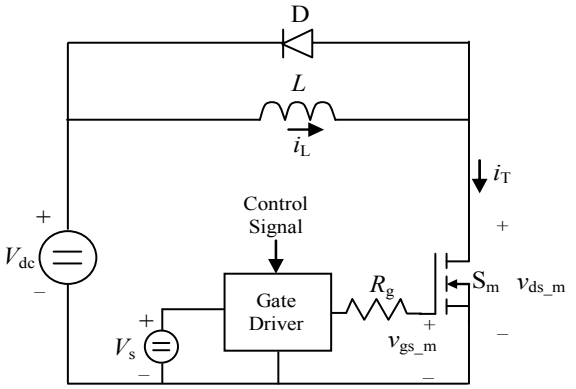

Fig. 5. Test circuit with EGDPS: V_{dc} = 300 V, S_m: APT47N60BCFG (600V, 46 A CoolMOS), D: IDH15S120 (1200 V, 15 A SiC Shottky), V_s = 12 V.

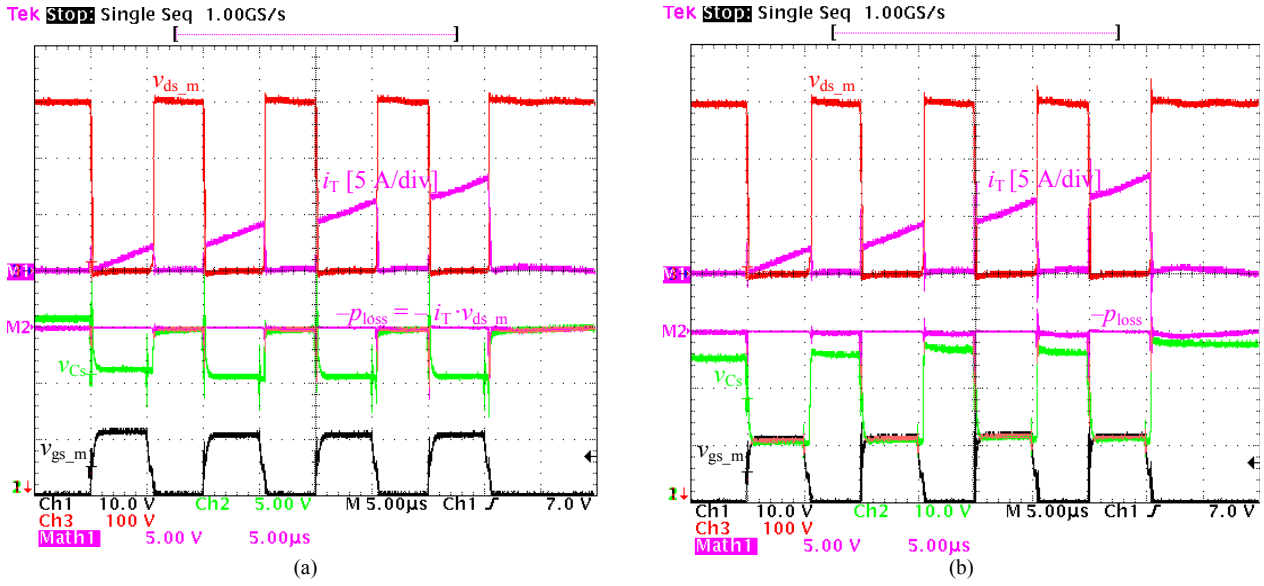

Fig. 6. Relevant waveforms under repetitive switching at low i_L current values. (a) IGDPS1. (b) IGDPS2.

Fig. 7 presents detailed turn-off waveforms at i_L = 6 A. In the case of IGDPS1, since the maximum current that the auxiliary circuit can take is lower than 3 A and T_{charge} is too high, a current tail appears at the end of the turn-off transition, significantly increasing the turn-off losses (92 μJ) in comparison with the EGDPS case (27 μJ). In IGDPS2, the performance clearly improves, producing a total turn-off loss of 38 μJ. Note that the current fall time in Fig. 7(d) is similar to the current fall time in Fig. 7(b), despite using a higher value of the gate resistance. An IGDPS has an effect of speeding up the turn-off transition compared to an EGDPS with the same value of R_g.

Fig. 8 presents detailed turn-off waveforms at i_L = 20 A. At high currents, IGDPS1 does not perform well because S_a cannot properly turn-on during the S_m turn-off transient. At the beginning of the turn-off process, the current that stops flowing through the S_m channel exceeds the maximum current that can flow through C_s, according to the analysis of the equivalent circuit in Fig. 2. The excess in current will have to flow through the parasitic capacitances of the circuit (S_m, S_a, D…). In particular, the current flowing through the parasitic capacitances of S_a will have to flow through D_z. On one hand, part of the current will flow through C_{dg_a} and D_z. On the other hand, part of the current will flow through C_{ds_a}, C_{gs_a}, and D_z. The later path will produce a decrease of the S_a gate charge, delaying the turn-on of S_a, which will occur after the S_m turn-off transient has already finished (C_{gs_a} will be recharged slowly through R_p). In the case of IGDPS2, instead, due to a higher current limit through C_s, the recharge of C_s is accomplished satisfactorily before the end of the switching transition, producing a total turn-off loss lower than in the EGDPS with the same value of R_g. This reduction in turn-off loss is due to the reduction of the current fall time that the IGDPS produces as compared with an EGDPS.

Fig. 9 presents the results of the turn-on and turn-off performance of all cases tested. Several parameters are plotted as a function of the switched current i_L to characterize these two switching transitions. For the turn-on transition, the parameters are:

1) $t_{d(on)}$: Time elapsed from v_{gs_m} = 1.2 V to $i_T = 0.1 \cdot i_L$.
2) t_r: Time elapsed from $i_T = 0.1 \cdot i_L$ to $i_T = 0.9 \cdot i_L$.
3) E_{on}: Energy lost from $i_T = 0.05 \cdot i_L$ to $v_{ds\_m} = 0.05 \cdot V_{dc}$.

For the turn-off transition, the parameters are:

1) $t_{d(off)}$: Time elapsed from v_{gs_m} = 10.8 V to $i_T = 0.9 \cdot i_L$.
2) t_f: Time elapsed from $i_T = 0.9 \cdot i_L$ to $i_T = 0.1 \cdot i_L$.
3) E_{off}: Energy lost from v_{gs_m} = 10.8 V to i_T = 0.

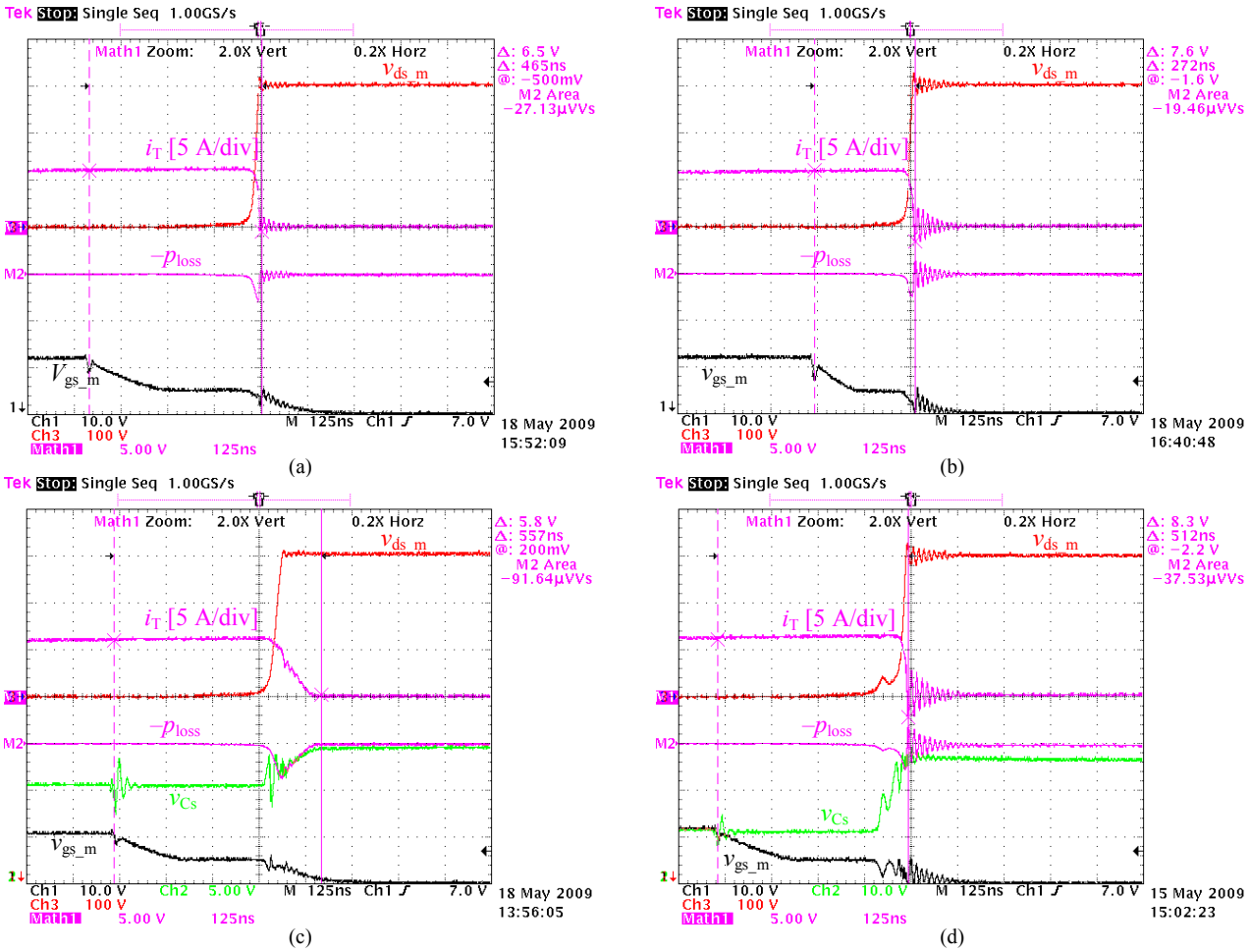

Fig. 7. Detailed turn-off waveforms at i_L = 6 A. (a) EGDPS, R_g = 10 Ω. (b) EGDPS, R_g =5 Ω. (c) IGDPS1, R_g = 10 Ω. (d) IGDPS2, R_g = 10 Ω.

The turn-on transition is much faster with an IGDPS, because the effective GDPS voltage for turn-on is higher than with an EGDPS (V_s = 12 V), producing lower turn-on losses. For instance, the effective V_s in the case of IGDPS2 has a value in between 12 V and 30 V. If a slower turn-on transition is desired to avoid current spikes, R_g can be increased.

With regard to the turn-off transition, it is interesting to note that the IGDPS2 design presents lower E_{off} than the EGDPS design at R_g = 10 Ω due to lower values of t_f. However, this advantage is lost as we reduce the value of R_g (speeding up the turn-off transition). Another drawback of the IGDPS is that $t_{d(off)}$ presents a higher value and a wider variation than in the EGDPS case, which may increase the complexity in determining blanking times for complementary commutation of switches.

In the IGDPS1 case, E_{off} has been computed up until v_{Cs} reaches 95 % of its final steady-state value at the S_m off state, due to the lack of enough precision in the current measurement. A real value of E_{off} higher than those presented in Fig. 9 should be expected.

V. Conclusion

In this paper, the performance of a self-powered unipolar gate driver supply circuit for power devices has been studied, with the aim of analyzing the viability of using such circuits in high voltage applications with discrete components. A simplified model of the heart of the circuit has been proposed, from which simple design guidelines have been provided to optimize the overall circuit performance. These design guidelines allow a proper component selection that can result in significant improvements in the design performance. In particular, the performance of the circuit can be significantly improved if modular (devices interconnected within a module) or integrated circuits are used [5], due to the reduction of the equivalent inductance L_e to values close to the optimum.

The performance of the circuit is satisfactory if turn-off transitions at a moderate speed and current levels are desired.

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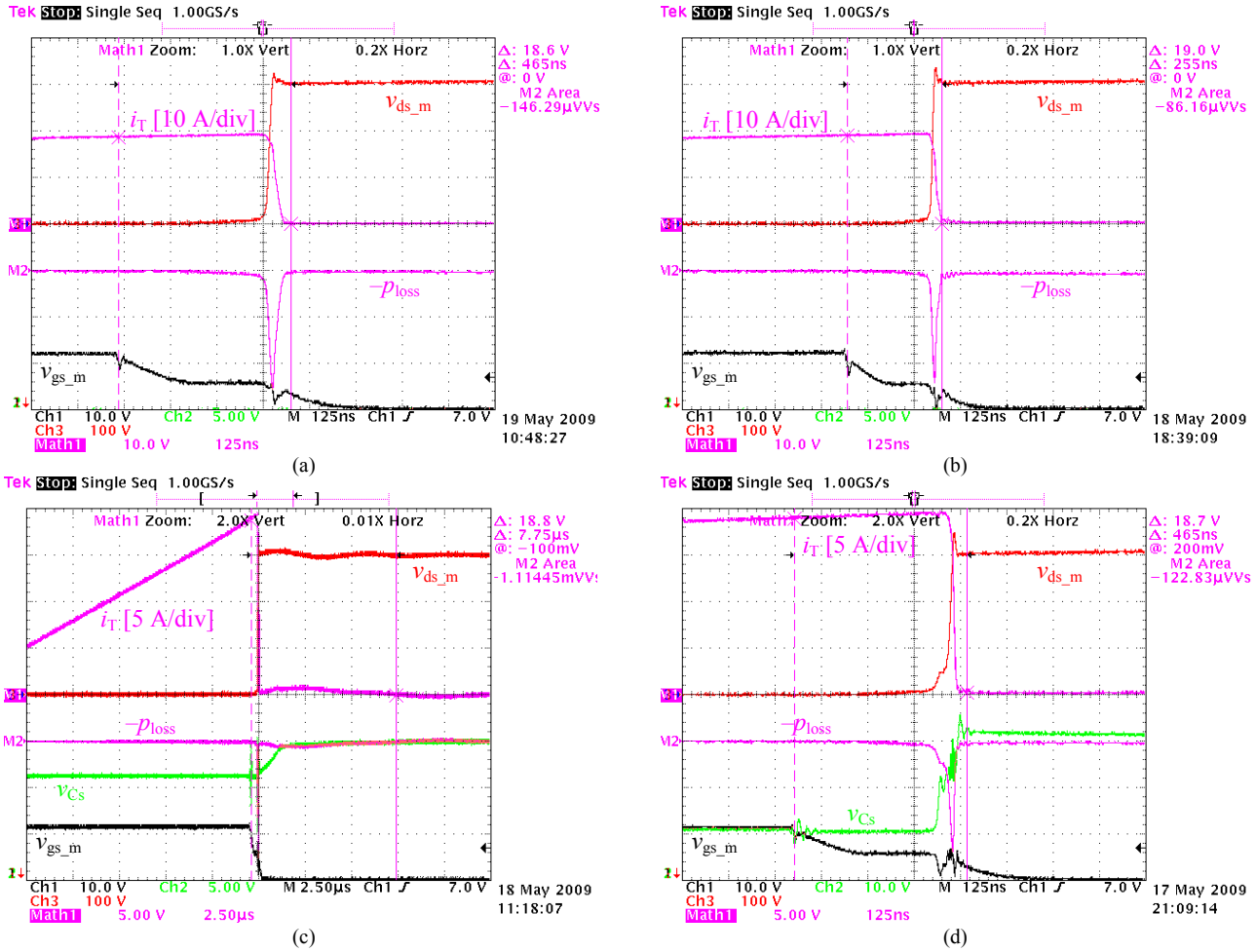

Fig. 8. Detailed turn-off waveforms at i_L = 20 A. (a) EGDPS, R_g = 10 Ω [125 ns/div]. (b) EGDPS, R_g =5 Ω [125 ns/div]. (c) IGDPS1, R_g = 10 Ω [2.5 µs/div]. (d) IGDPS2, R_g = 10 Ω [125 ns/div].

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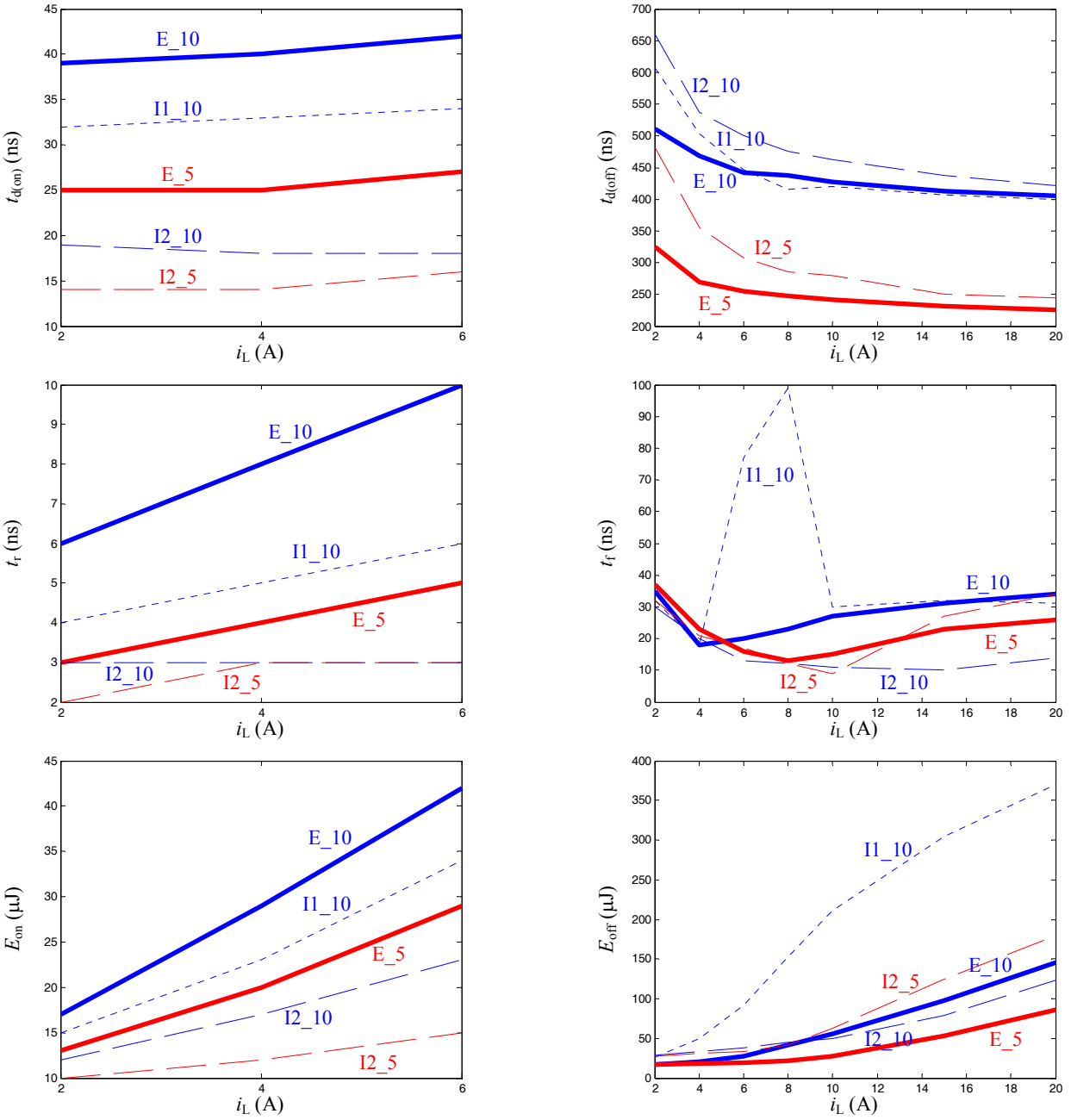

Fig. 9. Turn-on and turn-off parameters as a function of i_L for EGDPS R_g = 10 Ω (E_10), EGDPS R_g = 5 Ω (E_5), IGDPS1 R_g = 10 Ω (I1_10), IGDPS2 R_g = 10 Ω (I2_10), and IGDPS2 R_g = 5 Ω (I2_5).