An *m*-Level Active-Clamped Converter Topology – Operating Principle

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***Abstract*- This paper presents a novel multilevel active-clamped converter topology, which is an extension to *m* levels of the three-level active neutral-point-clamped topology. The operating principle is established through the definition of a proper set of switching states and a transition strategy between adjacent switching states. The benefits of the proposed converter topology and control in comparison to alternative multilevel converter topologies are discussed. Simulation results of a simple dc-dc converter configuration are presented to illustrate the converter performance features.**

I. INTRODUCTION

Multilevel converters [1]–[4] have opened a door for advances in the electrical energy conversion technology. These converters present the advantages of a lower device voltage rating, a lower harmonic distortion, and higher efficiency compared to conventional two-level converters.

These converters are typically considered for high power applications, because they allow operating at higher dc-link voltage levels with the current available semiconductor technology. But they can also be attractive for medium or even low power/voltage applications, since they allow operating with lower voltage-rated devices, with potentially better performance/economical features [5], [6].

There are three basic multilevel converter topologies: diode clamped, flying capacitor, and cascaded H-bridge with separate dc sources. A number of hybrid topologies combining them have also been proposed in the literature. This paper presents a novel multilevel topology built upon a single semiconductor device. This topology is an extension to an arbitrary number of levels of the popular three-level active neutral-point-clamped topology. A proper set of switching states and a switching state transition strategy are defined to obtain the maximum benefits from the proposed topology.

The paper is organized as follows. Section II presents the converter leg topology. Section III defines the operating principle. Section IV discusses the features of the proposed topology compared to alternative topologies and the possible converter configurations built upon the converter leg presented in Section II. Section V presents simulation results in a four-level dc-dc converter configuration to illustrate the operation features, and Section VI outlines the conclusions.

II. TOPOLOGY

Fig. 1 presents one leg of the generalized multilevel converter proposed in [7]. The topology is formed by a pyramidal connection of $m\cdot(m-1)/2$ instances of the basic cell defined in the inset of Fig. 1. The leg presents one output terminal (o) and m input terminals (i_k, $k\in\{1, 2,\ldots, m\}$), where m is the number of converter levels. A capacitor or a voltage source is connected across every two adjacent input terminals, being the dc voltage of each of these components typically the same ($V_{dclink}/(m-1)$). In this case, and if the converter is properly operated [7], each device of the basic cell (capacitor, switch, and diode) has to withstand a voltage equal to $V_{dclink}/(m-1)$. The topology is general, in the sense that several topologies can be derived from this one. For instance, as discussed in [7], removing the flying capacitors and the inner switches leads to the diode-clamped topology. Removing the inner switches and diodes leads to the flying capacitor topology.

Another option to simplify the topology, not considered in [7], is to remove only the flying capacitors. This leads to the active clamped topology proposed here and presented in Fig. 2. Removing the flying capacitors allows generating the topology from a single device (e.g., metal-oxide semiconductor field-effect transistor (MOSFET), where the diodes in the topology of Fig. 2 can be implemented through the MOSFET body diode) and opens new operational possibilities that are explored in the next section.

The active neutral-point-clamped topology presented in [8] and [9] represents the particular three-level case of the *m*-level topology presented here.

III. OPERATING PRINCIPLE

A. Switching States

The functional model of the converter leg in Fig. 2 is equivalent to the functional model of a diode-clamped converter, where a single-pole *m*-throw switch allows the connection of the output terminal (o) to each of the *m* possible input terminals (i_k). A set of *m* switching states are defined to implement these *m* possible connections. The switching states are defined with the aid of *m*–1 independent control variables (c_k, $k\in\{1, 2,\ldots, m-1\}$) and their complementary values ($\bar{c}_k$), representing the state (on: 1, off: 0) of the switches in Fig. 2. Each switch has an associated control variable, indicated within brackets in Fig. 2.

To connect the output terminal (o) to the input terminal (i_k), the control variable values are

$$\begin{aligned} c_j &= 0 \quad (j < k) \\ c_j &= 1 \quad (j \geq k). \end{aligned} \tag{1}$$

This work was supported by the Ministerio de Ciencia e Innovación, Spain, under Grant CSD2009-00046.

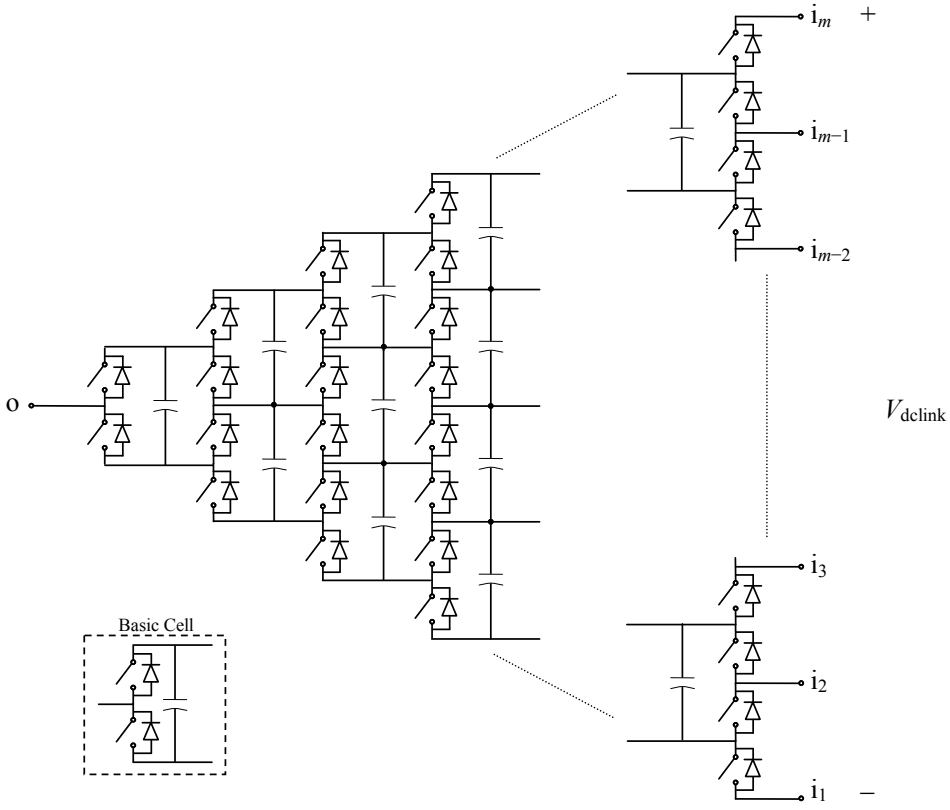


Fig. 1. Generalized multilevel converter leg topology (*m* levels) [7].

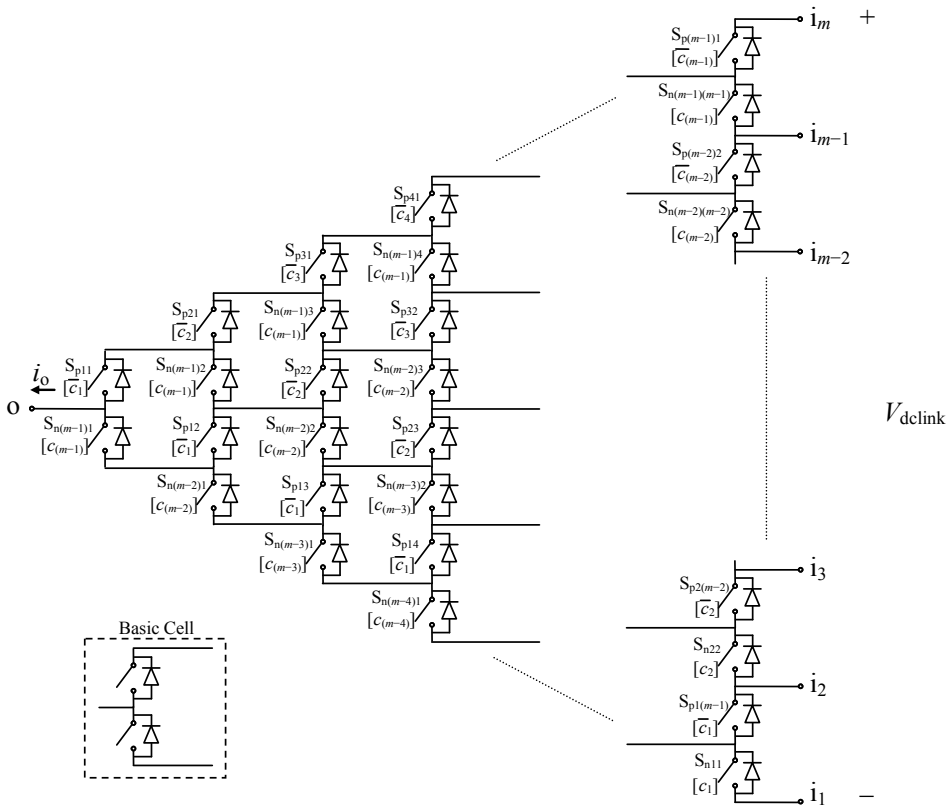


Fig. 2. Proposed multilevel active-clamped converter leg topology (*m* levels).

Table I presents a summary of the m possible switching states, defined according to (1).

Fig. 3 presents these switching states in the particular case of a five-level converter leg. The uncircled switches are off-state devices. The circled switches are on-state devices. The solid-line circled switches connect the output terminal to the desired input terminal and conduct the output terminal current (i_o). The arrows in Fig. 3 indicate the direction of the current flow through these switches. The dotted-line circled switches do not conduct any significant current and simply clamp the blocking voltage of the off-state devices to the voltage across adjacent input terminals (i_k and i_{k+1}).

It can be observed that the connection of the output terminal to the inner input terminals (i_k, $k \in \{2,\ldots, m-1\}$) presents more than one path of m–1 series-connected on-state switches to conduct the output current. The distribution of the output current i_o through the different current paths will depend upon the switch characteristics. If MOSFETs are used, in which the on resistance presents a positive temperature coefficient, current will be properly distributed through the solid-line circled devices. Assuming a value of the on resistance of an elementary switch equal to r, Table II presents the values of the equivalent on resistance of the connection of the output terminal to each input terminal in three-, four-, and five-level converter legs.

TABLE I
SWITCHING STATES

Switching State	Connection of 'o' to	c_1	c_2	c_3	…	c_k	…	c_{m-1}
1	i_1	1	1	1	…	1	…	1
2	i_2	0	1	1	…	1	…	1
3	i_3	0	0	1	…	1	…	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
k	i_k	0	0	0		1	…	1
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
m	i_m	0	0	0	…	0	…	0

TABLE II
EQUIVALENT ON RESISTANCE

Switching State	$m = 3$	$m = 4$	$m = 5$
1	$2r$	$3r$	$4r$
2	r	$1.4r$	$1.875r$
3	$2r$	$1.4r$	$1.5r$
4	—	$3r$	$1.875r$
5	—	—	$4r$

B. *Transitions between Switching States.*

The transition between two adjacent switching states (k and k+1) requires changing the state of m switches. The transition from switching state k to switching state k+1 requires turning off k diagonal switches (S_{nkj}, j = 1, 2, …, k) and turning on m–k diagonal switches (S_{pkj}, j = 1, 2, …, m–k). Obviously, the transition from switching state k+1 to switching state k requires turning off m–k switches (S_{pkj}, j = 1, 2, …, m–k) and turning on k diagonal switches (S_{nkj}, j = 1, 2, …, k).

In the transition between adjacent switching states, it is required to first turn off the devices to be turned off. Then, after a proper blanking time, we can proceed to turn on the devices to be turned on.

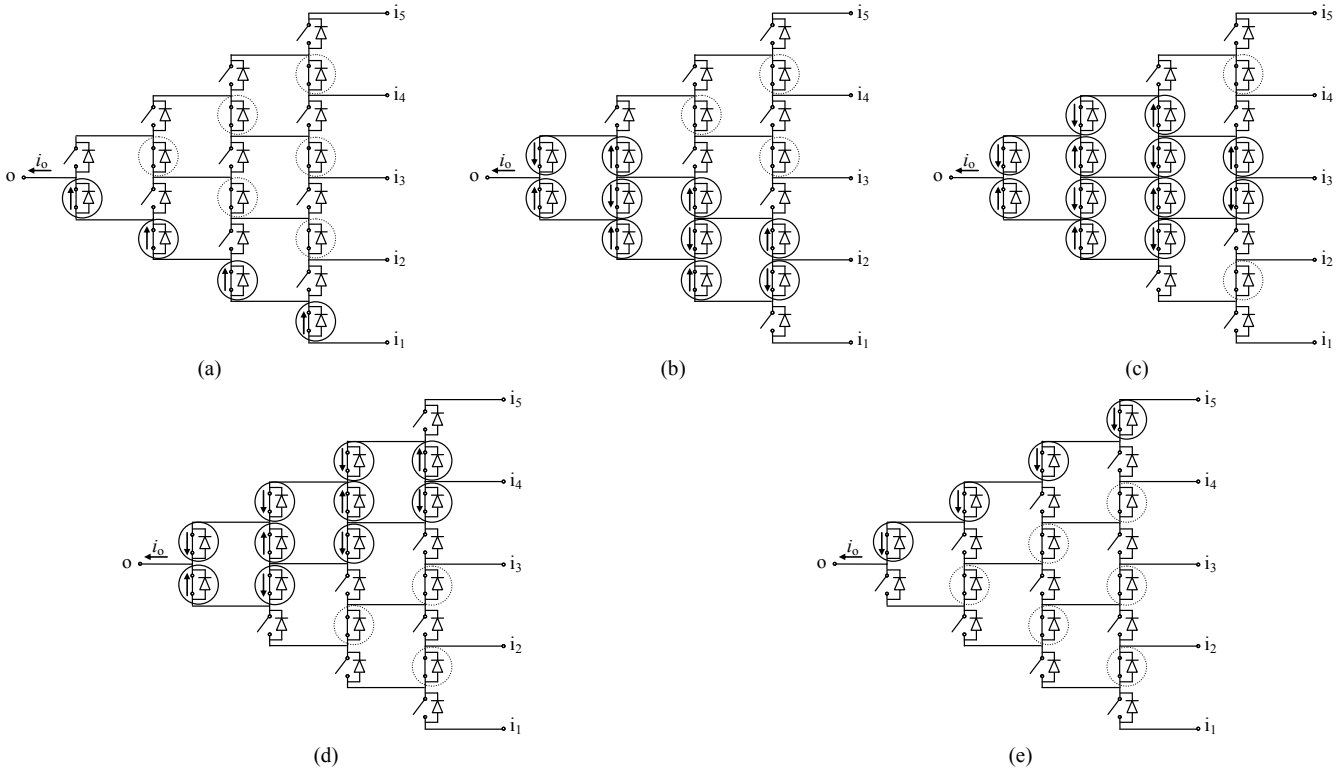


Fig. 3. Five-level converter-leg switching states. (a) Connection to node i_1. (b) Connection to node i_2. (c) Connection to node i_3. (d) Connection to node i_4. (e) Connection to node i_5.

In the transition between two adjacent switching states, if $(k_f–k_i)\cdot i_o>0$, where k_i and k_f are the initial and final switching states, respectively; then, the switching losses concentrate on the first switch being turned on. All the remaining switches produce negligible switching losses since the voltage across them when they turn on or off is approximately zero.

In the transition between two adjacent switching states, if $(k_f–k_i)\cdot i_o<0$; then, the switching losses concentrate on the last switch being turned off. As before, all the remaining switches produce negligible switching losses since the voltage across them when they turn on or off is approximately zero.

Therefore, an interesting strategy to distribute the switching losses among the devices is to alternate the first device being turned-on and to alternate the last device being turned-off in every transition between adjacent switching states. On the other hand, those devices experiencing lower conduction losses could be selected to concentrate the switching losses so that all devices present similar overall losses, and ultimately similar junction temperatures.

IV. DISCUSSION

The converter leg in Fig. 2 can be employed to implement the same converter configurations as with a diode-clamped topology. Fig. 4(a) and Fig. 4(b) show two possible configurations connecting capacitors between adjacent input terminals to form a dc-link. Fig. 4(a) represents a five-level boost-buck dc-dc converter with common grounding for the source and load systems [10]. Fig. 4(b) represents a multiphase dc-ac conversion system (it can also be used for dc-dc conversion applications not requiring a common grounding for the load and source). In a single phase configuration, two converter legs are needed. In a multiphase system with p phases, p converter legs are needed. The balancing of the dc-link capacitor voltages can be guaranteed in every switching cycle through using appropriate pulsewidth modulation (PWM) strategies ([10]-[12]) and controls [13], without the need of introducing additional hardware. The balance is achieved by extracting, in every switching cycle, a zero average current from the inner dc-link points.

If the dc-link capacitors can be replaced by dc voltage sources, the operational capabilities of the converter significantly improve (higher efficiency, lower output-voltage distortion, …), because the capacitor voltage balance is no longer a problem and more degrees of freedom are available to design the PWM strategies. Fig. 4(c) shows an example of a possible dc-dc or dc-ac converter configuration using a single converter leg.

The converter leg topology of Fig. 2 presents a total of $m\cdot(m–1)$ controlled switching devices. The number of switches is clearly higher than in alternative topologies. However, these extra switches provide some advantages.

Compared to diode-clamped topologies, the proposed topology clamps the blocking voltage of all devices to $V_{dclink}/(m–1)$ (this is not the case in diode-clamped topologies under certain operating conditions [9]), may present lower

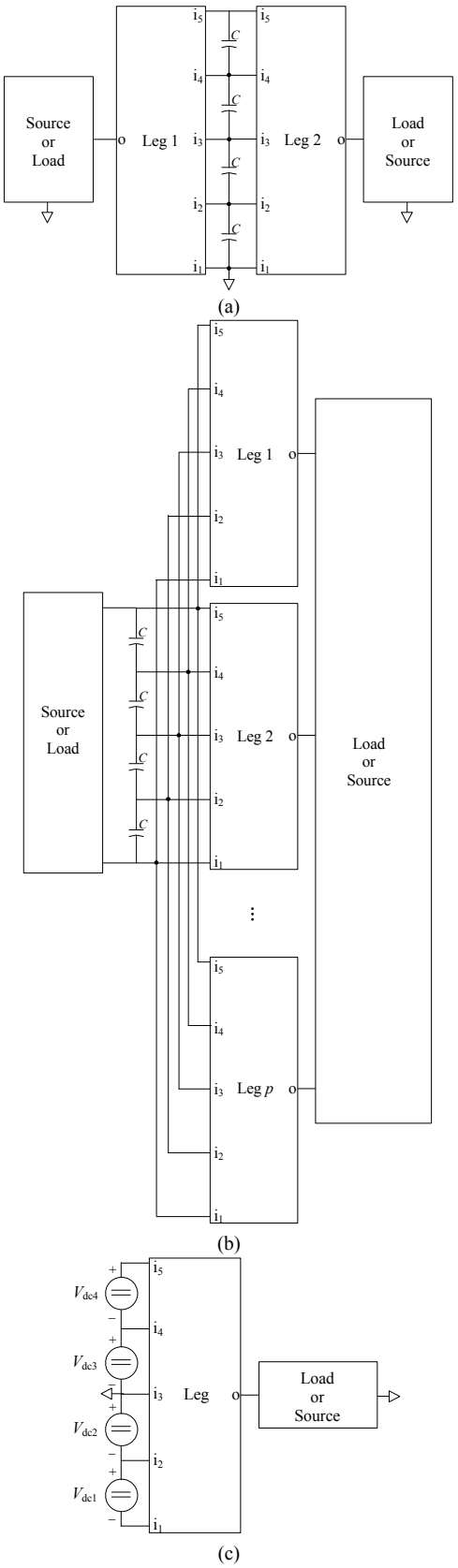


Fig. 4. Converter configurations (five-level example). (a) Boost-buck dc-dc converter with dc-link capacitors. (b) Multiphase dc-ac converter with dc-link capacitors. (c) Dc-dc or dc-ac single-phase converter with dc-link voltage sources.

conduction losses (due to the availability of several paths for the current to flow, while there is only one possible path in diode-clamped topologies), and allows distributing the switching losses among all the devices (in a diode-clamped topology, switching losses are concentrated in the available switches).

Compared to topologies with flying capacitors, the proposed topology avoids dealing with the precharge of the flying capacitors or the losses and high peak currents that occur when flying capacitors with different voltages are connected in parallel [7]. The cost and reliability of these capacitors can also be a problem.

In cases where separate dc voltage sources are available (e.g. Fig. 4(c)), the comparison with cascaded H-bridge topologies is also meaningful. Despite using a significantly higher number of devices, the proposed topology allows operating with a common dc-link for all legs and dc-link node voltages that are constant with respect to ground. In a cascaded H-bridge topology, these dc-link node voltages may oscillate at high frequency, requiring galvanic isolation of the dc voltage source terminals and producing common mode currents through parasitic elements that could be a problem in the design.

The comparison of the presented topology to conventional two-level converter configurations in terms of efficiency and reliability remains a pending issue.

Efficiency is expected to be higher, not only because low voltage-rated devices can be used with better relative performance features, but also because all switching transitions occur at lower blocking voltage levels, which in principle should produce lower switching losses for the same switching frequency and switching characteristics ([10]-[12]).

Reliability might be seen as an important drawback of the presented topology because of the use of a high number of components. However, while in a two-level converter the failure of one switch usually leads to a full system shut down, here the converter may continue operating, with obviously some reduction of the converter performance capabilities.

V. SIMULATION RESULTS

This Section presents simulation results to illustrate the performance of the proposed topology and control strategy. A simple four-level boost-buck dc-dc converter configuration, shown in Fig. 5, is selected to facilitate the presentation and discussion of results. The modulation strategy applied is described in [10]. Modulation Scheme 2 and a value of the modulation parameter $\delta = 0.25$ are chosen to produce an output voltage equal to the input voltage (V_A=V_B) [10]. The simulations are performed using SPICE-based software.

Fig. 6 presents relevant waveforms over two switching cycles. In Fig. 6(a), note that the dc-link capacitor voltages (v_{C1}, v_{C2}, and v_{C3}) are balanced at the end of every switching cycle because a zero switching-cycle-averaged current is injected into the inner dc-link points. Note also that the output leg currents (i_a and i_b) present an almost sinusoidal shape. This implies that the output leg currents present only one harmonic at the switching frequency, as opposed to a conventional two-level converter, where the output leg currents, presenting a triangular shape, include additional harmonics at multiples of the switching frequency.

Fig. 6(b) presents the current and voltage of each switch in the bottom half of the input converter leg. As can be observed, in each switching state, the output current is conducted through all on-state devices that connect the corresponding input terminal to the output terminal. The output current is shared by all possible current paths. The average conduction losses are in general different for each device.

The gating signals of the last six-switch pole (S_{n11}, S_{p13}, S_{n22}, S_{p22}, S_{n33}, and S_{p31}) have been adjusted so that these devices are the first to be turned-on and the last to be turned-off in a switching state transition and, therefore, they concentrate the switching losses. Fig. 7 presents the relevant switch current and voltage waveforms under a transition from switching state 2 to 3 (Fig. 7(a)) and a transition from switching state 3 to 2 (Fig. 7(b)). In Fig. 7(a), S_{n21} is initially turned off at *time* = 24.75 μs. S_{n22} is turned off 50 ns later. At *time* = 25.2 μs, S_{p22} is turned on. S_{p21} is turned on 50 ns later. In Fig. 7(b), S_{p21} is initially turned off at *time* = 34.75 μs. S_{p22} is turned off 50 ns later. At *time* = 35.2 μs, S_{n22} is turned on. S_{n21} is turned on 50 ns later. In both cases, as desired, switch S_{n22} concentrates the switching losses. The other devices change their state at zero voltage with no significant losses.

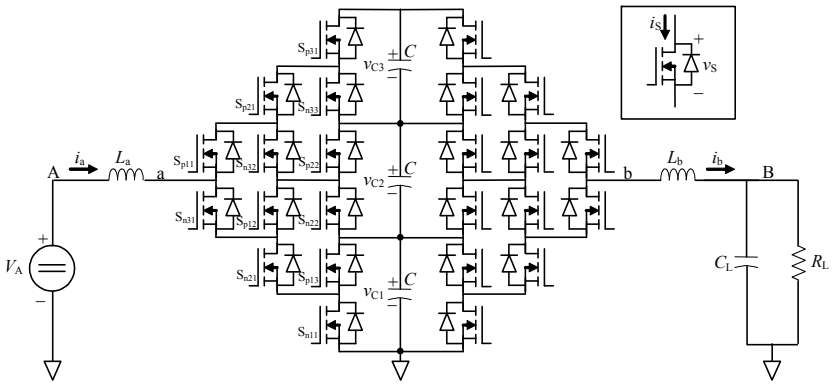
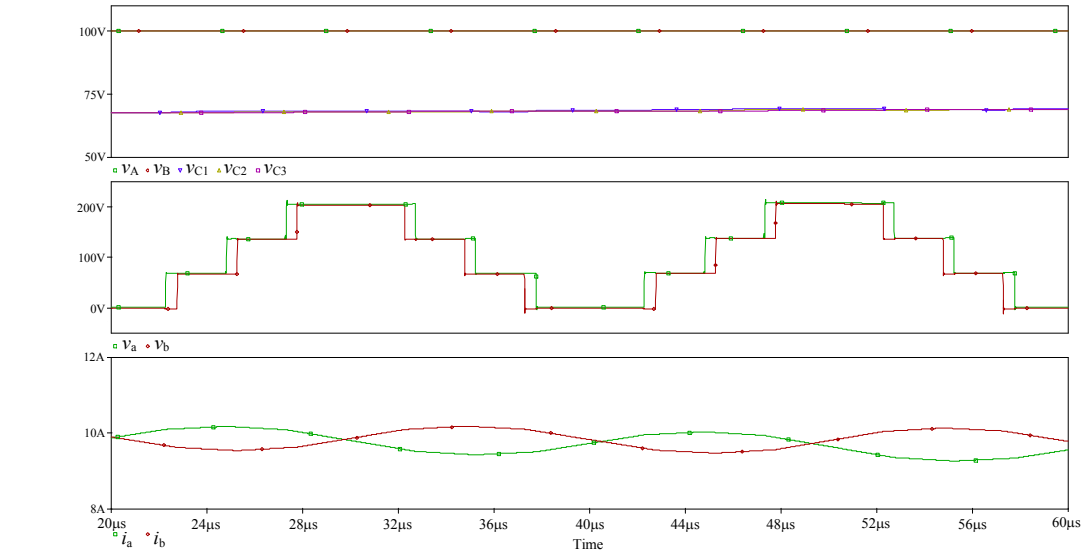


Fig. 5. Four-level boost-buck dc-dc converter implemented with MOSFETs.



(a)

(b)

Fig. 6. Simulation results over two switching cycles in the following conditions: V_A = 100 V, C = 10 µF, $L_a = L_b$ = 1 mH, R_L = 10 Ω, C_L = 100 µF, switching frequency f_s = 50 kHz, FDPF3860T (100 V, 20 A MOSFETs), gate resistance R_g = 10 Ω, gate supply voltage V_g = 10 V, blanking time t_b = 500 ns, and no output voltage regulation (open-loop control). (a) Input and output dc voltages (v_A, v_B), dc-link capacitor voltages (v_{C1}, v_{C2}, v_{C3}), leg output voltages (v_a, v_b), leg output currents (i_a, i_b). (b) Voltages and currents of the switches from the bottom half of the input converter leg.

VI. Conclusion

A novel multilevel topology and operating principle (patent pending) has been presented. The topology is an extension of the three-level active neutral-point-clamped converter. Switching states are defined so that all possible current paths connect the corresponding input terminal to the output terminal and blocking voltages are clamped to the desired level. Transitions between adjacent switching states can be performed selecting the device that concentrates the switching losses.

If a particular device (e.g., MOSFET) at specific voltage and current ratings is available with good performance, low cost, and ideally integrated auxiliary circuitry (gate driver, gate driver power supply [14], ...); then, this topology and control could be applied to implement a universal and easily scalable converter to be used in a number of applications.

Due to space limitations, experimental results and other aspects will be presented in a future paper.

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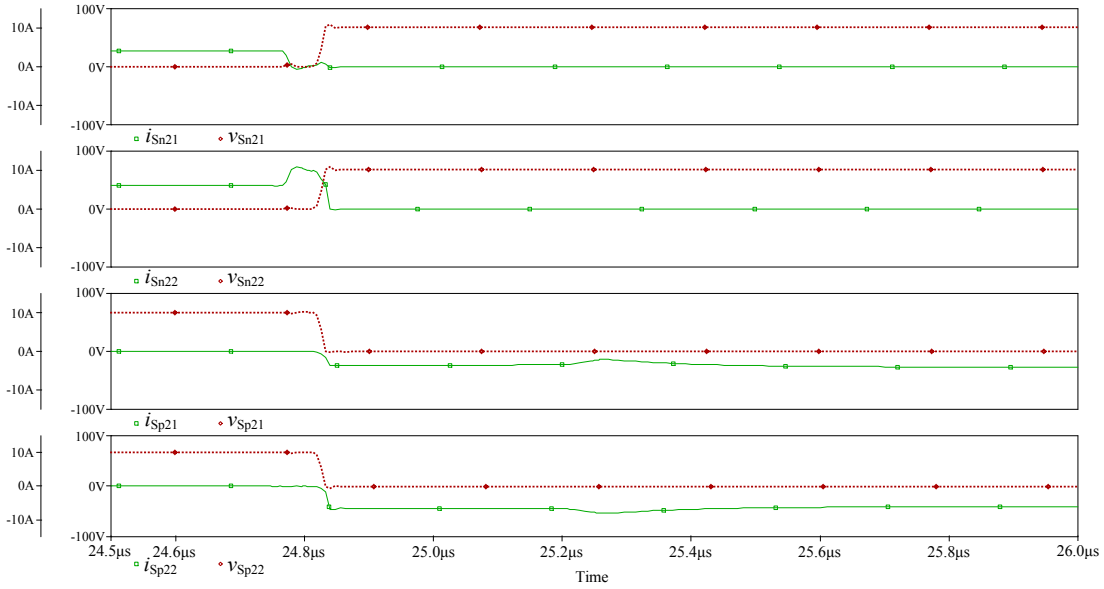

(a)

(b)

Fig. 7. Simulation results over switching state transitions in the same conditions of Fig. 6.
(a) Transition from switching state 2 to switching state 3. (b) Transition from switching state 3 to switching state 2.