Carrier-Based PWM Strategies for the Comprehensive Capacitor Voltage Balance of Multilevel Multileg Diode-Clamped Converters

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***Abstract*- This paper presents four carrier-based PWM strategies for diode-clamped converters of any number of levels and any number of legs (phases). These carrier-based PWM strategies guarantee the dc-link capacitor voltage balance in every switching cycle without the need of additional hardware and with low dc-link capacitance values for any modulation index and load, provided that the sum of leg currents equals zero. The performance of the presented carrier-based PWM strategies, in terms of dc-link capacitor voltage balance and total harmonic distortion in the output line-to-line voltages, is evaluated through simulation, showing a tradeoff between the simplicity of the carrier-based PWM implementation and its total harmonic distortion performance.**

I. INTRODUCTION

Multilevel converters [1]–[3] have opened a door for advances in the electrical energy conversion technology. These converters present the advantages of a lower device voltage rating, a lower harmonic distortion, and higher efficiency compared to conventional two-level converters.

These converters are typically considered for high power applications, because they allow operating at higher dc-link voltage levels with the current available semiconductor technology. But they can also be attractive for medium or even low power/voltage applications, since they allow operating with lower voltage-rated devices, with potentially better performance/economical features [4], [5].

There are three basic multilevel converter topologies: diode-clamped, flying capacitor, and cascaded H-bridge with separate dc sources. Among these topologies, diode-clamped converters are especially interesting because of their simplicity: the multiple voltage levels are generated passively through a set of series-connected capacitors (see Fig. 1.) However, these converters present the challenge of balancing the dc-link capacitor voltages. This problem has been extensively reported and analyzed in the literature.

References [6] and [7] present specific pulsewidth modulation (PWM) strategies to operate *n*-level two-leg (H-bridge, single phase) and three-leg (three phase) dc-ac diode-clamped converters with dc-link capacitor voltage balance without the need of introducing additional hardware. The balance of all dc-link capacitor voltages is guaranteed in every switching cycle, for any value of the modulation index and any load (balanced, unbalanced, linear, nonlinear…) provided that the sum of leg output currents is zero (load with isolated neutral) and that the leg output currents are approximately constant over the switching cycle. The balance is achieved by extracting, in every switching cycle, a zero average current from the inner dc-link points.

These PWM strategies are defined in terms of the leg duty-ratios of connection to the dc-link points as

$$\begin{aligned} &0 \le \theta < \pi:\ d_{1,1} = d_{2,n} = 0;\ \ d_{1,n} = d_{2,1} = m \cdot \sin(\theta) \\ &\pi \le \theta < 2\pi:\quad d_{1,1} = d_{2,n} = -m \cdot \sin(\theta);\ \ d_{1,n} = d_{2,1} = 0 \\ &d_{1,i} = d_{2,i} = \frac{1 - d_{1,1} - d_{1,n}}{n-2} = \frac{1 - d_{2,1} - d_{2,n}}{n-2} \\ &i = 2,3,\ldots,n-1, \end{aligned} \tag{1}$$

for two-leg (single phase) converters, and

$$\begin{aligned} &0 \le \theta < 2\pi/3:\quad d_{1,n} = m \cdot \cos(\theta - \pi/6),\ d_{2,n} = m \cdot \cos(\theta - \pi/2),\ d_{3,n} = 0 \\ &2\pi/3 \le \theta < 4\pi/3:\ d_{1,n} = 0,\ d_{2,n} = m \cdot \cos(\theta - 5\pi/6),\ d_{3,n} = m \cdot \cos(\theta - 7\pi/6) \\ &4\pi/3 \le \theta < 2\pi:\quad d_{1,n} = m \cdot \cos(\theta + \pi/6),\ d_{2,n} = 0,\ d_{3,n} = m \cdot \cos(\theta + \pi/2) \\ &-\pi/3 \le \theta < \pi/3:\ d_{1,1} = 0,\ d_{2,1} = m \cdot \cos(\theta + \pi/6),\ d_{3,1} = m \cdot \cos(\theta - \pi/6) \\ &\pi/3 \le \theta < \pi:\quad d_{1,1} = m \cdot \cos(\theta - 5\pi/6),\ d_{2,1} = 0,\ d_{3,1} = m \cdot \cos(\theta - \pi/2) \\ &\pi \le \theta < 5\pi/3:\quad d_{1,1} = m \cdot \cos(\theta - 7\pi/6),\ d_{2,1} = m \cdot \cos(\theta + \pi/2),\ d_{3,1} = 0 \\ &d_{1,i} = d_{2,i} = d_{3,i} = \frac{1 - d_{1,1} - d_{1,n}}{n-2} = \frac{1 - d_{2,1} - d_{2,n}}{n-2} = \frac{1 - d_{3,1} - d_{3,n}}{n-2} \\ &i = 2,3,\ldots,n-1, \end{aligned} \tag{2}$$

for three-leg (three phase) converters, where $d_{x,y}$ represents the leg x duty-ratio of connection to dc-link point y, m is the modulation index ($m \in [0,1]$ in the linear modulation range, overmodulation is not considered), and θ is the ac-side line-cycle angle.

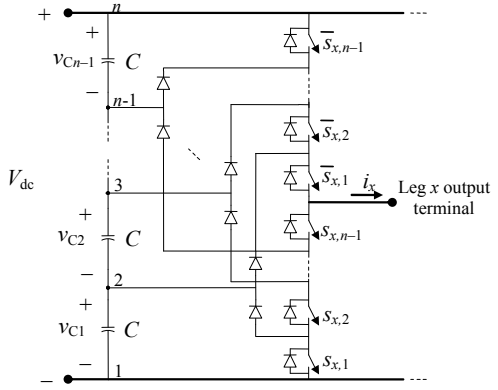

Fig. 1. Topology of an *n*-level diode-clamped converter leg.

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These expressions summarize the proposed PWM strategies and allow a simple digital implementation. Fig. 2 shows an example of the leg duty-ratio pattern obtained from (2).

The previous results were obtained from a space vector modulation approach. A carrier-based (CB) PWM approach is often more intuitive and instructive, and has a potential for computation load reduction resulting in more practical solutions.

This paper presents two new CB PWM strategies, equivalent to those defined in [6] and [7], offering an alternative implementation. These new CB PWMs are compared to conventional CB PWM strategies, highlighting the differences.

Additionally, two extra CB PWM strategies guaranteeing the dc-link capacitor voltage balance are proposed, featuring a more practical implementation.

All four proposed CB PWM strategies are defined for the general case of an n-level ($n \geq 3$) p-leg ($p \geq 2$) converter (the leg outputs are connected to p phases), extending the application scope beyond the three-leg case previously reported ([6] and [7]).

The paper is organized as follows. Section II reviews the two conventional CB PWM schemes for multilevel converters. Section III presents the four proposed CB PWM strategies to comprehensively guarantee capacitor voltage balance. Section IV presents simulation results to evaluate the performance of the PWM strategies presented, and Section V outlines the conclusions.

II. Conventional Carrier-Based PWM Strategies

Fig. 3 and Fig. 4 illustrate the two conventional CB PWM strategies for diode-clamped multilevel converters within a switching cycle with period T_s: level-shifted (LS) and phase-shifted (PS) PWM [8]. For each converter leg x, a modulating signal (d_x) is compared to n–1 carrier waveforms (c_1, c_2, …, c_{n-1}). In Fig. 3, the carrier waveforms are level shifted, with a possible phase-shift ($\varphi_{i,j}$) among them. In Fig. 4, the carrier waveforms are phase-shifted.

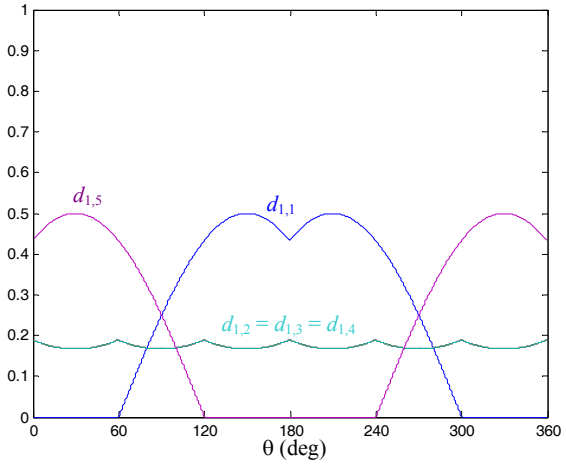

Fig. 2. Leg 1 duty-ratios from (2) over a line cycle for a five-level ($n = 5$) three-leg dc-ac converter with $m = 0.5$.

In both cases, the operating law is as follows: at any point in time, the leg output terminal is connected to the dc-link point j, where $j = 1 +$ (number of carriers < d_x).

Typically, in dc-ac conversion applications and in both LS and PS PWM

$$d_x(\theta) = m \cdot \cos\left(\theta - (x-1)\cdot\frac{2\pi}{p}\right) \qquad (3)$$

where $m \in [0, 1]$ is the modulation index, $\theta = \omega_o \cdot t$ is the ac-side line-cycle angle, p is the number of converter legs and $x \in \{1, 2, \ldots, p\}$ is the leg number.

In LS PWM, the phase-shift between consecutive carriers, $\varphi_{i,i+1}$, is typically equal to zero (LS phase-disposition (PD) PWM). In PS PWM, typically $\varphi_{i,i+1} = \pi/(n-1)$.

In general, these conventional PWM strategies, as defined above, lead to the unbalance of the dc-link capacitor voltages, either through low-frequency capacitor voltage oscillations or through the collapse of some capacitor voltages. An exception is the three-level two-leg (single phase) case ($n = 3$, $p = 2$), in which these conventional PWM strategies produce capacitor voltage balance in every switching cycle [6].

For dc-link capacitor voltage balanced operation, LS PD PWM provides optimal line-to-line voltage quality (lowest harmonic distortion), as in nearest-three space vector PWM, for the entire range $0 < m < 1$. This is the reason that carrier-based PWM research for diode-clamped converters has mainly focused on LS PWM. PS PWM only provides optimal voltage quality for $0 < m < 1/(n-1)$. For further modulation index increase, voltage quality is gradually compromised.

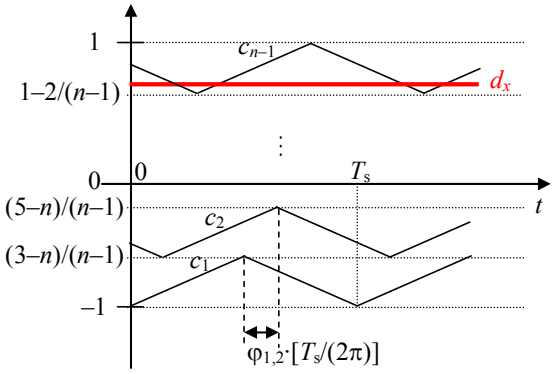

Fig. 3. Level-shifted PWM.

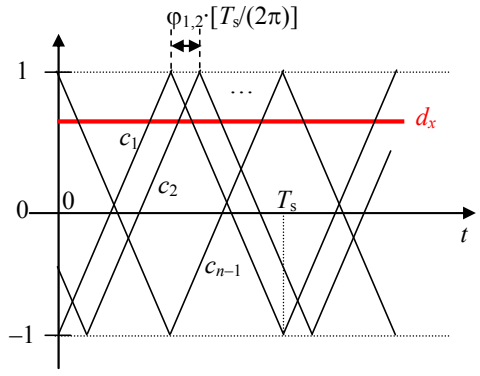

Fig. 4. Phase-shifted PWM.

However, PS PWM offers in return dc-link capacitor voltage balance opportunities that are explored in this paper.

III. Proposed Carrier-Based PWM Strategies

In the following, four CB PWM strategies are presented. These PWMs maintain the dc-link capacitor voltage balance in every switching cycle if the sum of output leg currents is equal to zero.

A. CB1 PWM

The first CB PWM strategy considers n–1 modulating signals ($d_{Sx,1}$, $d_{Sx,2}$,…, $d_{Sx,n-1}$) and one carrier (c) per leg, as depicted in Fig. 5 (the carrier is common to all converter legs). The comparison of the modulating signals to the carrier generates the switch control signals $s_{x,1}$, $s_{x,2}$,…, $s_{x,n-1}$; i.e., the crossings of each modulating signal with the carrier defines the switching instants of the corresponding pair of switches in Fig. 1.

The value of the modulating signals can be computed from the value of the typical modulating signals per leg in (3), modified by a factor k to be able to use a normalized value of the modulation index $m \in [0,1]$:

$$d_x(\theta) = m \cdot k \cdot \cos\left(\theta - (x-1)\cdot\frac{2\pi}{p}\right)$$
$$\begin{cases} \text{Even } p: \; k = 1 \\ \text{Odd } p: \; k = \dfrac{1}{\cos(\pi/(2p))} \end{cases} \quad (4)$$

The value of the modulating signals is then computed

$$d_{x,1}(\theta) = \frac{\max(d_1(\theta), d_2(\theta),..., d_p(\theta)) - d_x(\theta)}{2}$$
$$d_{x,j}(\theta) = \frac{2 - \max(d_1(\theta), d_2(\theta),..., d_p(\theta)) + \min(d_1(\theta), d_2(\theta),..., d_p(\theta))}{2\cdot(n-2)} \quad (5)$$
$$j = 2,3...,n-1$$
$$d_{Sx,i}(\theta) = \sum_{k=1}^{i} d_{x,k}(\theta)$$
$$i = 1,2,...,n-1.$$

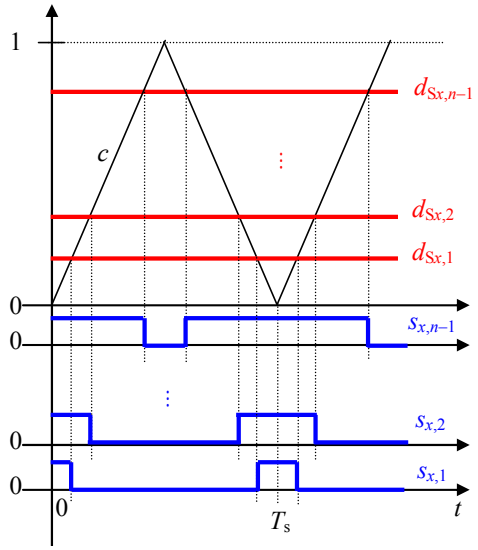

Fig. 5. CB1 PWM.

Fig. 6 shows the modulating signals over a line cycle in the same conditions of Fig. 2 (n = 5, p = 3, and m = 0.5). This PWM strategy is equivalent to the PWM strategy in [6] and [7] (i.e., if the modulating signals are regularly sampled, it produces exactly the same switch gate control waveforms) because the values of $d_{x,y}$ in (5) are equal to the values in (1) and (2), as can be observed by comparing Fig. 2 and Fig. 6: the modulating waveforms in Fig. 6 are obtained by addition of the appropriate leg duty ratios of Fig. 2. However, (5) extends the application of this PWM strategy to any number of converter legs (ac-side phases) $p \geq 2$.

This PWM strategy can be also understood as a LS PWM with n–1 modulating signals being compared (one to one) to n–1 level-shifted carriers in phase. From Fig. 5, each modulating signal could be compressed multiplying by 2/(n–1) and level-shifted, to be compared with the corresponding carrier in the LS PWM scheme of Fig. 3, and generate the switch control signals. In fact, this is the LS PWM strategy presented in [9] for a four-level three-leg converter. In the present paper, the definition of the modulating signals is extended to a higher number of levels and any number of converter legs. In addition, the PWM strategy is further simplified by considering one single carrier (Fig. 5). The use of several modulating waveforms in LS PWM schemes has also been considered in [10] to decrease the harmonic distortion of the output line-to-line voltages.

B. CB2 PWM

The remaining proposed CB PWM strategies are PS PWMs with specific modulating signals and phase-shifts for the carriers. To obtain the modulating signals we simply add an offset to the modulating signals in (4):

$$d_{\text{offset}}(\theta) = -\frac{\max(d_1(\theta), d_2(\theta),..., d_p(\theta)) + \min(d_1(\theta), d_2(\theta),..., d_p(\theta))}{2}$$
$$d_x'(\theta) = d_x(\theta) + d_{\text{offset}}(\theta) \quad (6)$$

Fig. 7 shows the modulating signals over a line cycle for p = 3 and m = 0.5.

Finally, we compare the modulating signals to a set of n–1 phase-shifted symmetric triangular carriers, where the phase-shift between consecutive carriers ($\varphi_{i,i+1}$) is such that the modulating signal with the highest value ($d'_{\max}$) and the modulating signal with the lowest value ($d'_{\min}$) pass through the crossing points of the first (c_1) and last (c_{n-1}) carriers (see Fig. 8). The value of the phase-shift between consecutive carriers is:

$$\varphi_{i,i+1}(\theta) = \frac{1 - \max(d_1(\theta), d_2(\theta),..., d_p(\theta))}{(n-2)} \cdot \pi; \; i = 1,2,...,n-2 \quad (7)$$

All modulating waveforms fall within the shaded area of Fig. 8, which is the necessary and sufficient condition for capacitor voltage balance in every switching cycle.

This PS PWM strategy is again equivalent to the PWM strategy in [6] and [7]. The problem of this PS PWM strategy is that it requires a variable phase shift between consecutive carriers along the line cycle, which may make its implementation difficult.

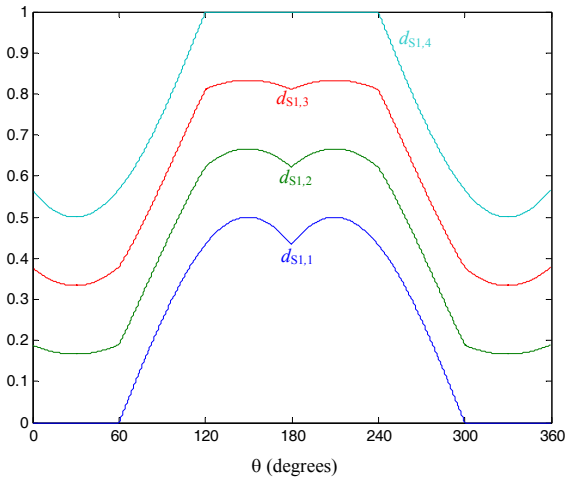

Fig. 6. Modulating waveforms in CB1 PWM for $n = 5$, $p = 3$, and $m = 0.5$.

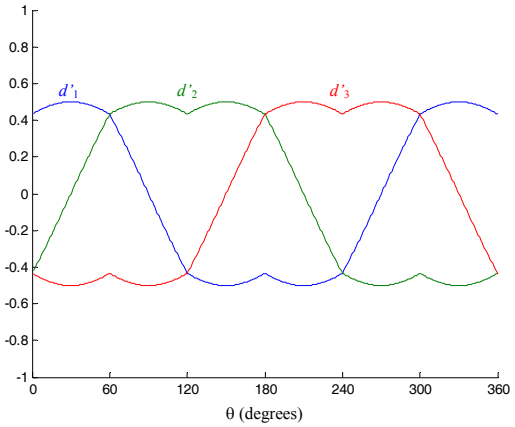

Fig. 7. Modulating waveforms in the CB2 PWM for $p = 3$ and $m = 0.5$.

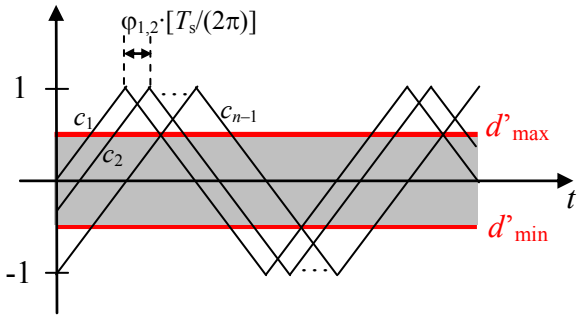

Fig. 8. Location of the maximum and minimum modulating signals in the CB2 PWM.

C. CB3 PWM

CB3 PWM is the same as CB2 PWM but with a value of the phase shift between carriers:

$$\varphi_{i,i+1}(\theta) = \frac{1-m}{(n-2)} \cdot \pi;\ i = 1,2,\ldots,n-2 \qquad (8)$$

In this case, and for constant m, the phase shift among carriers is constant over the line cycle.

D. CB4 PWM

CB4 PWM is the same as CB2 PWM but with a value of the phase shift between carriers:

$$\varphi_{i,i+1}(\theta) = \varphi_{\min};\ i = 1,2,\ldots,n-2 \qquad (9)$$

where $\varphi_{\min}$ is a constant value equal to the minimum phase shift achievable in practice between consecutive carriers. The phase shift among carriers is therefore constant for all operating conditions (for all values of m and θ).

This PS PWM strategy is equivalent to the quasi two-state mode PWM strategy presented in [11] for n-level three-leg diode-clamped converters.

IV. Simulation Results

In this section, simulation results are presented to evaluate the performance of the different proposed CB PWM strategies. The simulations have been performed in MATLAB-Simulink.

Fig. 9 shows the total harmonic distortion in the output line-to-line voltages (*THD*) of a three-leg dc-ac converter as a function of the modulation index for all proposed CB PWM strategies and two additional cases for comparison: a space vector modulation (SVM) strategy for a two-level converter and the original (O) PWM strategy presented in [7]. It can be seen that CB1 and CB2 are equivalent to O. CB3 presents a slightly higher *THD* and CB4 presents similar *THD* values as in a two-level converter. Comparing CB2, CB3, and CB4, it can be concluded that there is a tradeoff between the PWM simplicity and the *THD*.

Figs. 11-14 present simulation results corresponding to a five-level five-leg converter, as shown in Fig. 10. It can be seen that the proposed CB PWM strategies perform satisfactorily in multilevel multileg (multiphase) systems, guaranteeing the dc-link capacitor voltage balance in every switching cycle with low dc-link capacitance values. Note the use of all possible voltage levels (nine) in synthesizing the output line-to-line voltages v_{12} and v_{13}.

In real applications, dc-link capacitor voltage unbalances can occur due to several possible causes: high output-current ripple or any other conditions producing high output current derivatives, unequal switching behavior, leakage currents, etc. The proposed CB PWM strategies do not produce any low-frequency distortion in the ac-side line-to-line voltages and currents under unbalanced dc-link capacitor voltages [12]. On the other hand, these unbalances can be corrected by properly modifying the values of $d_{x,y}$ in CB1 (according to the closed-loop control presented in [13]) or the phase-shifts among carriers in CB2, CB3 and CB4.

The good performance of this type of voltage balancing PWM strategies has been experimentally verified in [6], [7], [12], and [13].

V. Conclusion

Four novel CB PWM strategies have been presented to control multilevel multileg diode-clamped converters, particularly in dc-ac conversion applications, guaranteeing the balance of the dc-link capacitor voltages in every

switching cycle for any modulation index and load, provided that the sum of output leg currents is zero and that the leg output currents are approximately constant over the switching cycle. The specific features of these PWM strategies that allow a comprehensive dc-link capacitor voltage balancing have been highlighted with reference to conventional CB PWM schemes. The capacitor voltage balance is obtained without the need of additional hardware but at the expense of increasing the total harmonic distortion at high modulation indexes, compared to other conventional PWM strategies.

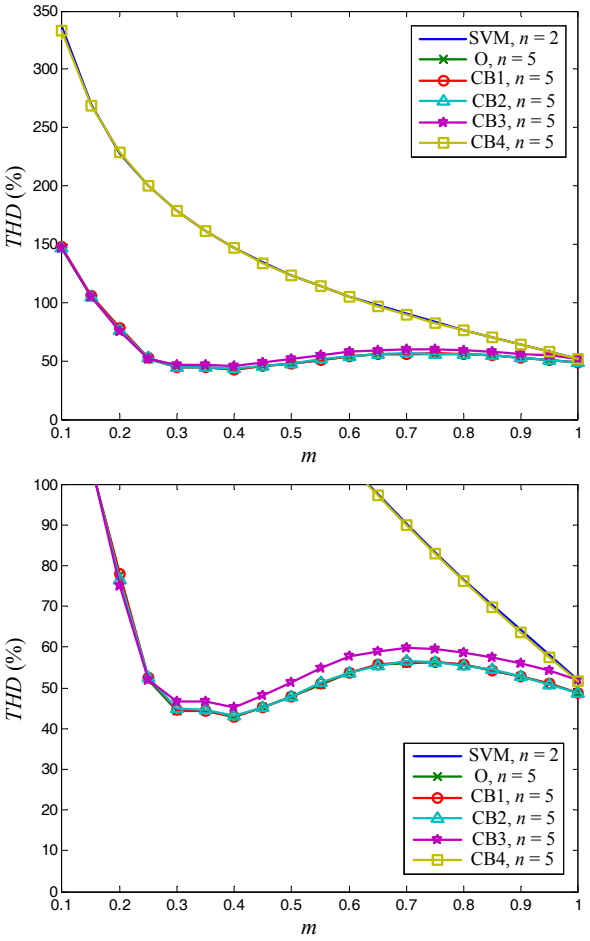

Fig. 9. *THD* as a function of the modulation index *m*. Conditions: $p = 3$, $\varphi_{min} = (0.01/3)\cdot\pi$ (in CB4), $f_s / f_o = 100$ and harmonics considered up to $40 \cdot f_s$.

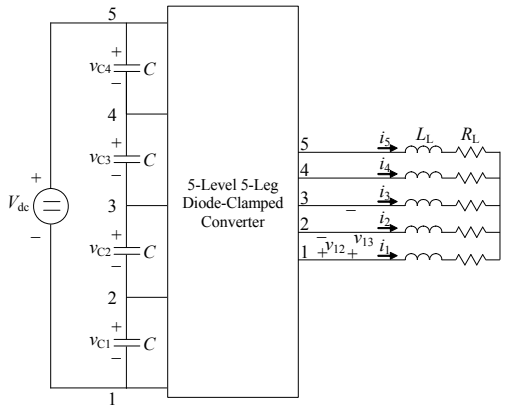

Fig. 10. Five-level five-leg diode-clamped inverter with a five-phase load.

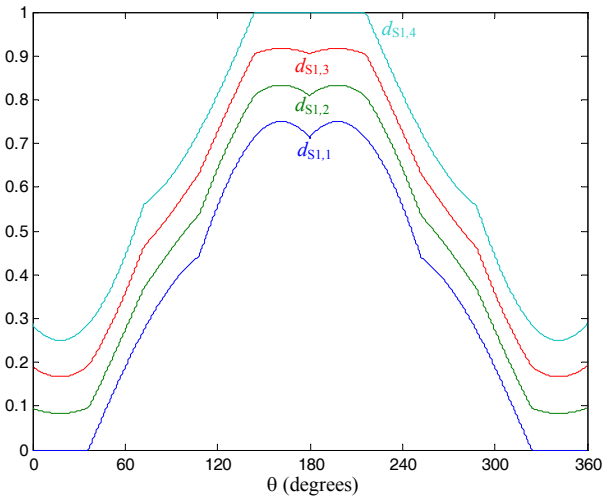

Fig. 11. Modulating waveforms for CB1, $n = 5$, $p = 5$, and $m = 0.75$.

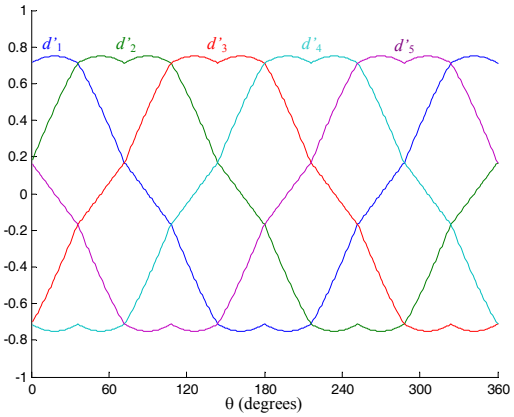

Fig. 12. Modulating waveforms for CB2, CB3, CB4, $p = 5$, and $m = 0.75$.

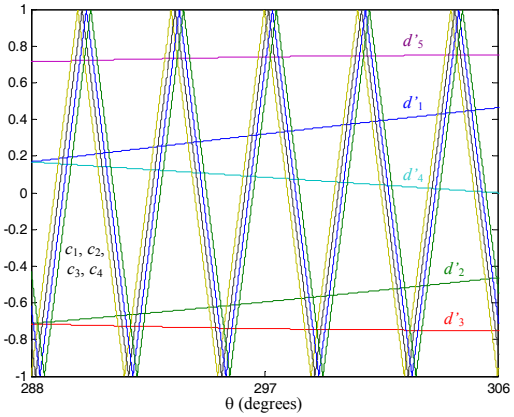

Fig. 13. Detail of the modulating and carrier waveforms for CB2, $n = 5$, $p = 5$, and $m = 0.75$.

The presented CB PWM strategies allow an alternative implementation of other equivalent PWMs already reported in the literature for *n*-level two-leg (single phase) and three-leg (three-phase) diode-clamped converters. Furthermore, the strategies presented here are defined for any number of legs (phases), extending this type of PWMs to converters with more than three ac-side phases.

If a particular switch (e.g., MOSFET), ideally with integrated auxiliary circuitry (gate driver, gate-driver power supply [14], protections…), and a particular diode (e.g., Schottky), both with good performance characteristics, are available; then, multilevel converters of different voltage ratings could be built from these two devices. The extended use of these two devices could bring their cost down enough to make the proposed multilevel topologies competitive with conventional topologies.

Therefore, the proposed PWM strategies enable the use of easily scalable multiphase and compact (small dc-link capacitances) diode-clamped converters in applications such as ac motor drives, with higher efficiency and lower output line-to-line voltage harmonic distortion than conventional two-level converters [6], [7].

REFERENCES

[1] J. Rodríguez, J. Lai, and F. Peng, "Multilevel inverters: a survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, vol. 49, pp. 724-738, Aug. 2002.

[2] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.,* vol. 54, pp. 2930-2945, Dec. 2007.

[3] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Magazine,* vol. 2, pp. 28-39, 2008.

[4] B. A. Welchko, M. B. de Rossiter Correa, and T. A. Lipo, "A three-level MOSFET inverter for low-power drives," *IEEE Trans. Ind. Electron.*, vol. 51, pp. 669-674, June 2004.

[5] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," *IEEE Trans. Ind. Applicat.*, vol. 41, pp. 855-865, May-June 2005.

[6] S. Busquets-Monge, S. Alepuz, J. Rocabert, and J. Bordonau, "Pulsewidth modulations for the comprehensive capacitor voltage balance of *n*-level two-leg diode-clamped converters," *IEEE Trans. Power Electron.*, vol. 24, pp. 1951-1959, Aug. 2009.

[7] S. Busquets-Monge, S. Alepuz, J. Rocabert, and J. Bordonau, "Pulsewidth modulations for the comprehensive capacitor voltage balance of *n*-level three-leg diode-clamped converters," *IEEE Trans. Power Electron.*, vol. 24, pp. 1364-1375, May 2009.

[8] G. Holmes and T. A. Lipo, *Pulse width modulation for power converters. Principles and practice*, IEEE Press, Piscataway, NJ, 2003.

[9] F. Bovolini and H. Pinheiro, "Generalized PWM approach for dc capacitors voltage balancing in diode-clamped multilevel converters," in *Proc. European Conf. on Power Electron. and Appl.*, 2009, pp. 1-12.

[10] W. Yao, H. Hu, and Z. Lu, "Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter," *IEEE Trans. Power Electron.*, vol. 23, pp. 45-51, Jan. 2008.

[11] G. P. Adam, S. J. Finney, A. M. Massoud, and B. W. Williams, "Capacitor balance issues of the diode-clamped multilevel inverter operated in a quasi two-state mode," *IEEE Trans. Ind. Electron.*, vol. 55, pp. 3088-3099, Aug. 2008.

[12] S. Busquets-Monge, J. Rocabert, P. Rodríguez, S. Alepuz, and J. Bordonau, "Multilevel diode-clamped converter for photovoltaic generators with independent voltage control of each solar array," *IEEE Trans. Ind. Electron.*, vol. 55, pp. 2713-2723, July 2008.

[13] S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, "Voltage balancing control of diode-clamped multilevel converters with passive front-ends," *IEEE Trans. Power Electron.*, vol. 23, pp. 1751-1758, July 2008.

[14] S. Busquets-Monge, J. Rocabert, C. Crebier, and J. Peracaula, "Diode-clamped multilevel converters with integrable gate-driver power-supply circuits," in *Proc. European Conf. on Power Electron. and Appl.*, 2009, pp. 1-10.

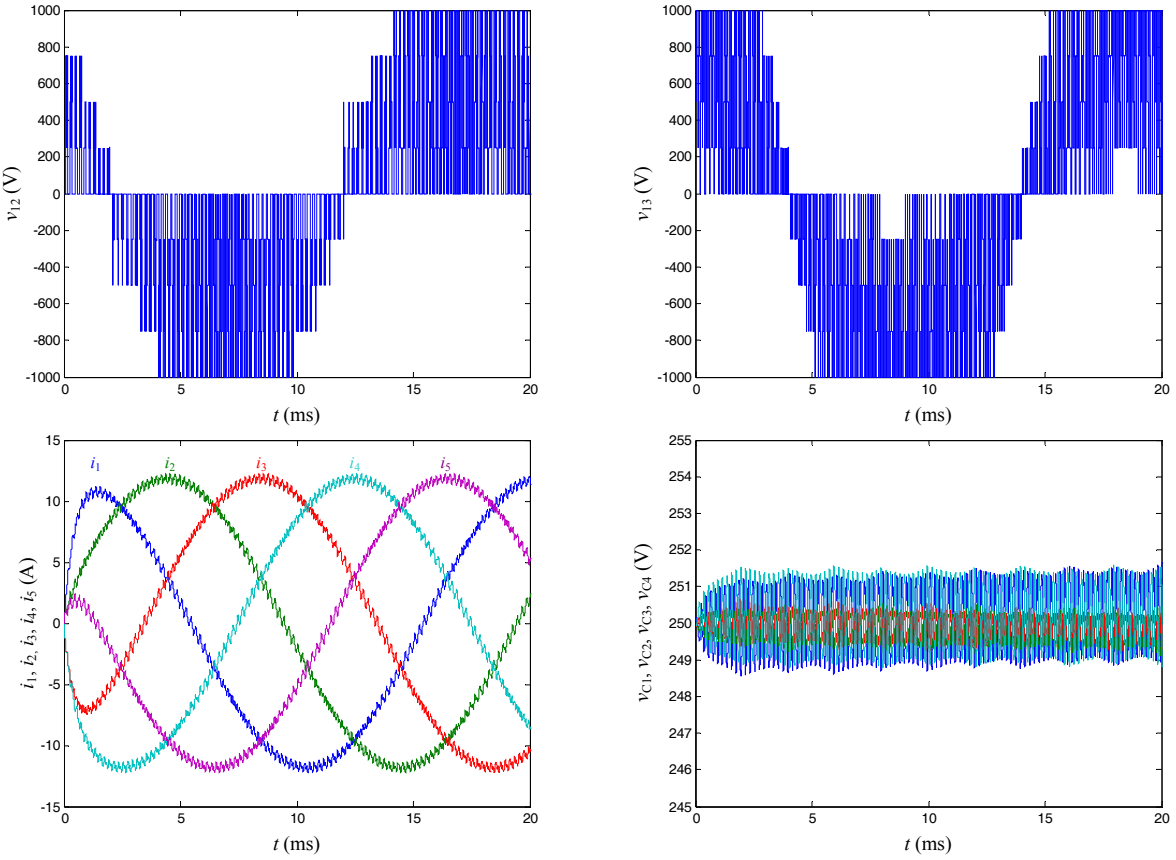

Fig. 14. Simulation results for the two different line-to-line voltages (v_{12}, v_{13}), line currents (i_1, i_2, i_3, i_4, i_5), and dc-link capacitor voltages (v_{C1}, v_{C2}, v_{C3}, v_{C4}) in the following conditions: CB2, $n = 5$, $p = 5$, $m = 0.75$, $V_{dc} = 1000$ V, $f_o = 50$ Hz, $f_s = 5$ kHz, $C = 200$ µF, $R_L = 33$ Ω, and $L_L = 15$ mH.