A Compact Charge Ratio Expression for the Emitter Delay of Polysilicon Emitter Bipolar Transistors

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***Abstract*—A compact solution for the ratio of the excess minority carrier charge stored into the polysilicon to the charge stored in the single crystal part of the emitter of a polysilicon emitter bipolar transistor is derived. The solution is based on an existing comprehensive model which takes into account the interfacial oxide and an arbitrary number of grains in the polysilicon layer. The emitter charge partition in polysilicon and single crystal emitter components is summarized in contour plots for constant values of the ratio.**

I. INTRODUCTION

The large f_T values recently achieved by polysilicon emitter bipolar transistors [1], have come about because of the lateral and vertical dimension reduction along with new isolation techniques. The forward delay time components arising from emitter and base layers become the more significant the more the capacitance terms are reduced. The base component can be reduced by downscaling the base-collector junction depth, whereas the emitter component reduction strongly depends on the feasibility of further reduction of the emitter-base junction depth without compromising the ideality factor of the Gummel plots, and on the morphology of the interface polysilicon-single crystal silicon.

This brief paper presents a compact analytical expression for the ratio of the minority carrier charges stored in the single crystal emitter region and in the polysilicon emitter region extending existing models [2].

II. MODEL

In an earlier work, the ratio between the minority carrier charge stored into the polysilicon to the charge stored in the single crystal part of the emitter was used to calculate the contribution of the polysilicon layer to the total emitter transit time [3]. A simple expression for the charge ratio was derived there assuming that there was not an interfacial oxide layer and the polysilicon was modelled by a box containing a single grain. Such model was not linked to more comprehensive polysilicon emitter contact model.

In this work, a more elaborate solution for the charge ratio between the two parts of the emitter is presented. A geometry, such as depicted in Fig. 1, has been used, in which a polysilicon layer of n grains is supposed to contact a single crystal silicon; an interfacial oxide in between the two layers is considered.

The model described in reference [2] has been followed. According to it, and considering an npn transistor, the ratio of the minority carrier concentration in grain boundary $(i-1)$ to the concentration in grain boundary (i) can be written as shown in Table I. As can be seen three cases are possible: odd and even values of (i) and the last possible value for (i), namely $i = 2n + 2$, where the interfacial oxide is located. In Table I, S_{gb} is the grain boundary recombination velocity, S_I is the recombination velocity at the interfacial oxide-silicon boundary, D_{pg}, τ_{pg}, L_{pg} are the polysilicon grain diffusion constant, lifetime and diffusion length respectively d_g is the polysilicon grain thickness. T_{gb} is a constant which relates the current through a grain boundary to the difference of minority carrier concentration at the two edges of the grain boundary. T_I is the same constant but related to the interfacial oxide and depends on the oxide thickness and on the potential barrier for holes as shown in Table I as taken from [2].

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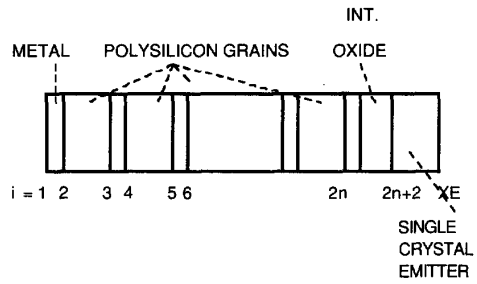

Fig. 1. Geometry used in the model.

TABLE I
SUMMARY OF KEY RELATIONSHIPS BETWEEN CARRIER CONCENTRATIONS AND RECOMBINATION VELOCITIES

	$\frac{p(i-1)}{p(i)}$	$s(i)$
i=odd	$\frac{T_{gb}}{S(i-1)+T_{gb}+S_{gb}}$	$S_{gb}+T_{gb}-\frac{T_{gb}^2}{S(i-1)+S_{gb}+T_{gb}}$
i=even	$\frac{b_g}{S(i-1)+a_g}$	$a_g-\frac{b_g^2}{S(i-1)+a_g}$
i=2n+2	$\frac{T_I}{S(2n+1)+S_I+T_I}$	$S_I+T_I-\frac{T_I^2}{S(2n+1)+S_I+T_I}$

$a_g=\frac{D_{pg}}{L_{pg}}\mathrm{Coth}\frac{d_g}{L_{pg}}$ $\quad b_g=\frac{D_{pg}}{L_{pg}}\mathrm{Sinh}^{-1}\frac{d_g}{L_{pg}}$

$T_I\sqrt{\frac{kT}{2\pi m^*}}\frac{e^{-b_h}}{1-c_hkT}$ $\quad b_h=\frac{4\pi\Delta}{h}\sqrt{2m_h^*X_h}$ $\quad c_h=\frac{2\pi\Delta}{h}\sqrt{\frac{2m_h^*}{X_h}}$

In Table I equations for the parameter $S(i)$ applying to every of the three cases are also shown. $S(i)$ is an effective recombination velocity which relates linearly at each location (i) the current density, $J(i)$ to the minority carrier concentration $p(i)$:

$$J(i) = qS(i)p(i). \tag{1}$$

The excess minority carrier charge, Q_P, stored into the polysilicon can be calculated by integrating the excess carrier distribution $p(x)$:

$$Q_P = q\sum_{\substack{1\\ i=\mathrm{odd}}}^{2n-1}\int_{x(i+1)}^{x(i)} p(x)dx. \tag{2}$$

In (2) the charge stored in the grain boundaries is neglected.

Solving the diffusion equation inside a polysilicon grain and then integrating the minority carrier distribution between grain boundaries it follows that, the stored charge is given by

$$Q_P = \tau_{Pg}\sum_{\substack{2\\ m=\mathrm{even}}}^{2n} J(m) - \sum_{\substack{1\\ i=\mathrm{odd}}}^{2n-1} J(i). \tag{3}$$

The charge stored in the single crystal part of the emitter, Q_s is now required. We have calculated, in a previous work, [3] an analytical solution for Q_s:

$$Q_S = J(2n+2)\left[\frac{N_{\rm ef}(2n+2)}{S(2n+2)}\int_{x(2n+2)}^{x_E}\frac{dx}{N_{\rm ef}(x)} + \int_{x(2n+2)}^{x_E}\frac{dx}{N_{\rm ef}(x)}\int_{x}^{x_E}\frac{N_{\rm ef}(y)}{D(y)}dy\right] \quad (4)$$

where $N_{\rm ef}$ is the effective doping concentration and D is the minority carrier diffusion constant in the single crystal emitter. In the derivation of (4) the quasi-neutral emitter is assumed to be transparent [4].

Dividing now Q_P by Q_S,

$$\frac{Q_P}{Q_S} = \frac{\tau_{\rm Pg}\sum_{\substack{2\\ m=\rm even}}^{2n} J(m) - \sum_{\substack{1\\ i=\rm odd}}^{2n-1} J(i)}{J(2n+2)F(2n+2).} \quad (5)$$

where $F(2n+2)$ is the term inside the brackets in (4).

Applying (1) to $J(i)$, $J(m)$ and $J(2n+2)$ it follows

$$\frac{Q_P}{Q_S} = \frac{\tau_{\rm Pg}}{F(2n+2)}\sum_{\substack{2\\ m=\rm even}}^{2n} S(m)\frac{p(m)}{p(2n+2)} - \sum_{\substack{1\\ i=\rm odd}}^{2n-1} S(i)\frac{p(i)}{p(2n+2).} \quad (6)$$

In (6) the carrier concentration ratios can be easily calculated using the equations summarized in Table I.

The emitter delay time can then be calculated

$$\tau_{\rm E} = \tau_{\rm ES} + \tau_{\rm EP} = \tau_{\rm ES}\left(1+\frac{\tau_{\rm EP}}{\tau_{\rm ES}}\right) = \tau_{\rm ES}\left(1+\frac{Q_P}{Q_S}\right) \quad (7)$$

where $\tau_{\rm ES}$ is the single crystal emitter delay time and $\tau_{\rm EP}$ is the polysilicon emitter delay time.

III. RESULTS

We have used (7) above to compute the values for the charge ratio in a polysilicon emitter bipolar transistor in which the thickness of the interfacial oxide, the number of grains and the thickness of the polysilicon have been varied. A gaussian emitter and base profiles have been used with several junction depths. Bandgap narrowing and mobility values have taken from [5] and [6]. Typical values for the parameters involved in the equations have been taken as follows [7]: $T_{\rm gb} = 5.2 \times 10^5$ cm/s, $S_{\rm gb} = 7.5 \times 10^4$ cm/s, $S_{\rm I} = 1.5 \times 10^3$ cm/s, $T_{\rm I} = 7.9 \times 10^4$ cm/s, $d_{\rm g} = 1000$ Å, $D_{\rm gb} = 3.43$ cm^2/s, $\tau_{\rm gb} = 1.88 \times 10^{-9}$ s, $L_{\rm gb} = 8 \times 10^{-5}$ cm $\chi_{\rm h} = 1$ eV.

In Fig. 2 the effect of varying the single crystal emitter depth and the interfacial oxide thickness is summarised. Polysilicon emitter bipolar transistors with several values for the emitter depth have been simulated assuming the same base-collector junction depth (150 nm) and the same polysilicon thickness (200 nm). The results in Fig. 2 are given as contour plots of constant values for the Ratio QEP/QES ranging from 12 to 0.25, for various interfacial oxide thicknesses (from 0 Å to 6 Å) and various single crystal emitter thicknesses (from 10 nm to 70 nm).

The results shown in Fig. 2 indicate that the charge partition in polysilicon emitters can be quantified and that the ratio of charge stored into the polysilicon to the single crystal emitter can take values ranging from 0.25 for the thicker emitters and the thicker interfacial oxide to 12 for the thinner emitters and the thinner interfacial oxide layers. For the same value of the single crystal emitter layer depth the charge into the polysilicon is drastically reduced as the interfacial oxide thickness is increased. For the same value of the interfacial oxide thickness, the charge into the polysilicon is also reduced as the single crystal emitter depth is increased.

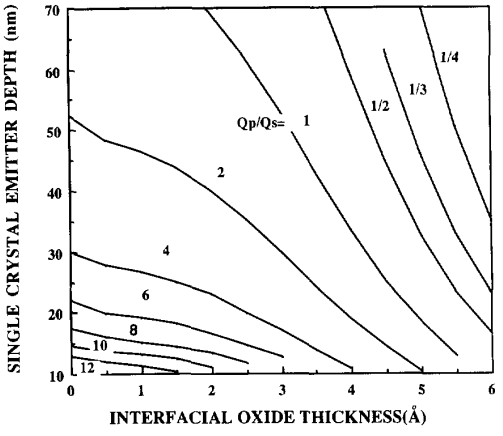

Fig. 2. Contour plots of polysilicon to single crystal silicon charge ratio for different values of single crystal emitter junction depth and interfacial oxide thickness. The collector-base junction depth is 150 nm.

The results shown indicate that the speed of polysilicon emitter bipolar transistors, will be increased not only by downscaling the single crystal emitter depth but also by a careful consideration of the parameters of the polysilicon layer itself.

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