Design and implementation of a power transistor temperature measurement circuit for a multilevel active-clamped power converter

Master Degree in Electronic Engineering

Author: Federico GUOLO

Supervisors: Prof. Josep BORDONAU
Prof. Paolo TENTI
Prof. Sergio BUSQUETS
Dott. Joan NICOLAS
Dott. Àlber FILBA

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by Federico Guolo

Semiconductor power switches are largely considered the most fragile components in power electronic converters. In order to increase the reliability of power devices, it is important to avoid high junction temperatures and high junction temperature fluctuations, which are basically caused by conduction and switching losses in the devices. The purpose of the thesis is to find and implement a robust method to sense the junction temperature of a power switch and deliver this information to the converter controller. The method will be implemented using a circuit that has to be small, cheap and with low-power consumption, since the circuit will be fed by the same power supply used by the gate-driver circuit of the power device. This method is designed to be applied into the multilevel active-clamped converter. One of the main advantages of this topology is its degree of freedom to select the power switch that concentrates the switching losses in the switching-state transitions. By sensing the switches temperatures, it will be possible to always select the coolest transistor to take the switching losses. This will enable a better distribution of the temperature and a lower cost of the cooling system. In addition to this, an improved reliability of the system can be achieved.
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Chapter 1

Introduction

Power converters are used everywhere, from industrial fields to domestic ones. Their application—especially in the industrial field—require stringent demand on reliability. For example, a breakdown in the supply chain of an electronic power converter in a car may lead to severe accidents, while a downtime of a whole system implies high costs for an industry.

A recent survey has shown that the most unreliable components in electronics are the power switches, followed by capacitors and gate drivers. The main problem of these components is due to the fact that most of the times power converters are required to work in a stressful environment with high voltages and high temperatures.

When it comes to reliability of electronic components, the temperature plays an important role since that it increases a lot the rate of failure mechanisms, and this is why it is easier for power components to break respect to the other ones.

Expensive cooling system are integrated inside the package of power converters to reduce their temperature. A way to lower the cost of these systems is to improve the distribution of the power generated by the switching activity inside the power converters; in this way the size of the cooling system can be reduced as well as the costs of the final project.

![Figure 1.1: Power Electronic Plant for HVDC](image)
1.1 Multilevel Active-Clamped converter

A converter topology that allows to achieve this goal is the Multilevel Active-Clamped converter (MAC converter).

The leg of the converter is formed by a pyramidal connection of \( \frac{m(m-1)}{2} \) instances of the basic cell defined in the inset of the figure 1.2. The leg presents one output terminal (o) and m input terminals (ik, k \( \in \{1,2,\ldots,m\} \)), where m is the number of converter levels.

A capacitor or a voltage source is connected across every two adjacent input terminals, with the dc voltage of each of these components being typically the same \( V_{dclink} \). If the converter is operating properly, each device of the basic cell has to withstand a voltage equal to \( V_{dclink} \).

In the functional model of the converter leg, a single-pole m-through switch allows the connection of the output terminal (o) to each of the m possible input terminals (ik).

**Figure 1.2:** Leg of a Multilevel Active-Clamped converter
A set of \( m \) switching states is defined to implement these \( m \) possible connections. The switching states are defined with the aid of \( m - 1 \) independent control variables \( (c_k, k \in 1,2,\ldots, m - 1) \) and their complementary values \( (c_k) \), representing the state (ON: 1, OFF: 0) of the switches.

To connect the output terminal \( (o) \) to the input terminal \( (i_k) \), the control variable values are

\[
\begin{align*}
  c_j &= 0 & \text{for} & & j & < k \\
  c_j &= 1 & \text{for} & & j & \geq k
\end{align*}
\]  

(1.1)

The figures below present these switching states in the particular case of a five-level converter leg. In this figures, the uncircled switches are OFF-state devices, the circled ones are instead in the ON-state.

The solid-line circled switches connect the output terminal to the desired input terminal and conduct the output terminal current \( (i_o) \) while the dotted-line circled ones do not conduct any significant current and simply clamp the blocking voltage of the OFF-state devices to the voltage across adjacent input terminals \( (i_k \text{ and } i_{k+1}) \).

The arrows indicate the direction of the current flow through these switches.
Chapter 1. Introduction

FIGURE 1.5: Switching states of the Multilevel Active-Clamped converter’s leg in the third and the fourth state

FIGURE 1.6: Switching states of the Multilevel Active-Clamped converter’s leg in the fifth state

It can be observed that the connection of the output terminal to the inner input terminals (i_k, k ∈ 2, . . . , m - 1) presents more than one path of m - 1 series-connected On-state switches to conduct the output current. The distribution of these through the different current paths will depend upon the switch characteristics, state, and parasitics. This parallelization greatly reduces the total series resistance -Ron- of the current paths and increases the fault resistance of the converter, since that more than a single path are available.

Moreover, every switching cycle it is possible to choose which transistor will sustain the switching losses of that cycle, from the moment that only one power switch will interrupt the current path -hard switching- and all the other switches will commutate with zero voltage or zero current -soft switching-. Hard-switching means that there is an overlap between voltage \( v_{DS} \) and current \( i_{DS} \) when switching the transistor on and off. This overlap causes energy loss, which makes the transistor to heat up.

This feature can be used to effectively achieve a cost reduction of the total converter, since that a better power distribution can be achieved inside the converter. To do so, the easiest way is to always choose the coolest switch in a current path.
The objective of this thesis is in fact to find and implement a robust method to collect the temperature from the power switches so that in the future this information will be used inside the MAC converter to better distribute the power dissipation between the various switches.

The circuit designed has to be easily integrable inside the circuit, cheap and with low-power consumption, since that it will be supplied by the same power supply used by the gate driver.
Chapter 2

State of the art

In power electronic the junction temperature is usually estimated through analytical calculations to make sure that the maximum temperature that a device can withstand is never reached. The calculations are based on the datasheet values that a manufacturer provides.

![Diagram of junction temperature evolution](image)

**Figure 2.1:** Typical idealised evolution of junction temperature in a power module over time

From the picture above it can be easily seen that the temperature can be decomposed in two temperatures, a slow varying one, that changes with the environment, and a fast-varying one, that changes with the single power cycle. An averaged measurement can be done by using a thermal model without capacitors, and by taking into account a safety margin for the maximum temperature so that the device will work in a safe zone.

The problem of using this method is that the cooling system will cost more than needed and that the ageing of the device will change its thermal model -and that change depends on the single device-, which will be very far from the original one after after some years. From these example it is now clear how the temperature estimation may lead to a wrong estimation after some use of the devices.
In order to avoid this kind of problems, a lot of methods to collect the devices temperature have been developed, each one with advantages and disadvantages. Since that there are a lot of them, some bounds must me kept in mind in order to choose the correct sensing method.

- Accuracy: Some application require precise measurement while some others require just to know if some devices are faulty, in that case a simple sensing on the case of the device would be enough. If instead a control algorithm has to be implemented, a faster method is required.

- Time resolution: Some methods simply cannot track instantaneously the temperature, since they measure an averaged one across various periods.

- Cost-Benefit trade-off: Some methods require to disrupt the power converter operation to measure the junction temperature, while others require to place a sensor inside the case of the power device in order to have a more precise sensed temperature. Both of these two examples may have a higher cost respect to some other forms of sensing.

2.1 Direct Measurements

The easiest way to implement a measurement system -although it is not the cheapest one- is the direct measure of the temperature using an IR sensor. The measurement is done directly on the dye of the semiconductor using an optical fibre to carry the signal to the sensor.()

This method can also be used with high voltages and currents without any particular precautions, since that the measurement system is insulated from the power components.
2.1. Direct Measurements

The main problem of this method is that for each power switch an optical fibre has to be placed. If a lot of switches are present, a lot of fibres will be connected and the system won’t be a feasible solution.

Another fact is also that the insulation has to be removed to allow the measurement of the junction temperature, so that the system will have a security problem.

If the insulation is not removed then the sensed temperature will be related to the case temperature and not to the junction temperature itself, which will be different since power switches are generally encapsulated by power module packages or discrete component packages. By sensing the temperature on the case has also the disadvantage that the cooling systems ruin the collected measurement, since that they are applied to the device packages surface. (R. Wu; F. Blaabjerg, 2013)

At the rated power in fact, the switching semiconductor $T_j$ is higher than the package surface temperature because of the thermal impedance of device package. In transient analysis, the temperature change of package surface is slower compared with the fast power dissipation in the semiconductor chip because of the thermal impedance and heat capacitance of the device package, thus the switching power semiconductor temperature sensing cannot be easily achieved on the surface of the device package.

A better option rather than placing a lot of fibres, is the placement of a sensor inside the package placed near the dye in order to sense the junction temperature.

The most common sensor placed inside the package it is a simple diode. This is due to the fact that the relationship between current and temperature in a diode is well known and linear.

![Diagram of on-chip supplementary temperature sensors](image)

**Figure 2.3:** On-chip supplementary temperature sensors

The main problem with this method is that not all the mosfets have a sensing diode packaged with them, thus if this sensing method is chosen, the cost of the overall project will increase due to this boundary. (R. Wu; F. Blaabjerg, 2013)

Also, because the diode is placed very close to the switching power semiconductor, the noise generated by the switching activity can distort the performance of the sensor.
2.2 Temperature Sensitive Electrical Parameters -TSEPs-

To overcome the need to have external temperature sensors, a different approach is used. This is based on the sensing of some Temperature Sensitive Electrical Parameters (TSEPs) and by knowing these, the junction temperature is estimated.

These are parameters that change with the temperature, and if their relationship with it is known, than they can be used to get the junction temperature. To gather the relationship with the temperature, some measurement of the interested parameter are performed at different temperatures to create a table that maps the value of the parameters to the temperature. (A. Hamidi, 2001)

The main problem found with them is that most of these are hard to use because they either change in time -ageing of the device- or they are not only temperature-dependent but they also vary with some other electrical parameters. By the way in the past years much research has focused on the studying of these parameters, since that it is difficult to sense them inside a power switch without breaking its operations.

Anyway, the methods developed to measure these parameters are the most promising in the field of temperature sensing, since that costs are lower if compared to any external sensors.

A division in 3 categories has been performed to ease the explanation.

- Classical TSEPs: The traditional ones, such as $V_{CE}$, $V_{TH}$ and the saturation current $I_{sat}$.
- Static characteristic: Sensing the device behaviour at high currents.
- Dynamic characteristic: Sensing the transient switching parameters of the device.

2.2.1 Classical TSEPs

Classical TSEPs are the most used parameters among the one exposed above because a lot of techniques have been developed until now to sense them.

$V_{CE}$ at low currents

The first method presented the evaluation of the temperature using the $V_{CE}$ at low current injection. (A. Hamidi, 2001)

This method is easy to understand and to use, since that it uses the characteristic of the $V_{CE}$ to be linear respect to the temperature. This method becomes very useful if an IGBT is used as power switch.

A sensing current of about 1/1000th of the device current rating is imposed to the power device and the voltage drop $V_{CE}$ is measured. The voltage drop is about 2mv and it does change a lot depending on the sensing current, so this means that the current must be strictly the same at each measurement.
2.2. Temperature Sensitive Electrical Parameters -TSEPs-

Figure 2.4: VCE(low) on a Fuji 6MBI100VA-120-50 IGBT measured with a variety of sensing currents

The $V_{CE}$ has been typically used for offline characterization where the sensing current is injected into the devices a short time after the load is removed. In this way $V_{CE}$ is recorded as the device cools down and a graph of $V_{CE}$ - square root of time is used to estimate the temperature when the load is disconnected.

This measurement must be performed only at low currents so that the nature of the PN junction overrides the internal losses due to the resistance of the power module.

That’s the main problem on these parameters, the separation of the effects due to the temperature from those due to electrical reasons. To do so, the only way is to interrupt the operations of the converter and to sense the parameters in a favourable environment.

One of the many methods to sense $V_{CE}$ is when the current reaches a value close to 0. When this happens, the current is diverted into another transistor and the measurement can be done in a few hundred of microseconds - that is an acceptable delay.

Figure 2.5: VCE(low) measurement during inverter operation using supplementary switches
Chapter 2. State of the art

\[ V_{TH} \]

For the \( V_{TH} \) measurement, different approaches can be chosen and they vary in relation to component used.\()

For the MOSFETs, the measurement circuit is implemented with an increased gate resistance to slow down the turn on of the MOSFET when the measure has to be done. The disconnection of the measured switch is always required, since that a fixed low current has to be set.

For IGBTs, the induced voltages over the parasitic inductances of the package is used to trigger a measurement as the IGBT turns on. The voltage sensed is assumed to be \( V_{TH} \). It has to be noticed that the IGBT is not disconnected from the load, so this measurement is less invasive respect to the MOSFET counterpart but it is more affected by any fluctuation in the circuit.

\[ I_{SAT} \]

The last "classical" TSEP is the saturation current \( I_{SAT} \) when the gate-emitter and collector-emitter voltages are set.

The first technique is to partially turn on the device by supplying it with a gate-emitter voltage of 6V for 2\( \mu \)s.

The second one is similar to the previous one, but now a hard switching fault is induced with another switch to measure the peak current. The problem of this measurement is the instantaneous heating of the component, which limits the frequency of the temperature measurement and reduces its lifetime.\()

To measure the current, the breakdown of the normal operations is required and \( I_{SAT} \) has an exponential relationship with the temperature, which makes the calibration process harder.

The measurement of the temperature are possible during the converter operation, but the modifications to the converter’s structure make these option non-suited to the market.

2.2.2 Static Characteristic

It is known that the IV characteristic of all the power devices depends on the temperature. This has been used a lot in the past, since that both the current and the forward voltage of a power switch are easy to collect.\( (\text{Wieman and Hollberg, 2013}) \)

In a MOSFET using this characteristic means to use the \( R_{DS\text{ON}} \) as a TSEP.

Knowing the IV characteristic implies to know bot the voltage and the current of every device.

Just one current sensor is enough for the whole circuit while several measurement circuit have been proposed in the past years to measure \( V_{DS} (V_{CE}) \) in normal operations.\()

The main problem of this method is that the sensing of the voltage \( V_{DS} (V_{CE}) \) is not performed directly onto the dye of the semiconductor but it is measured outside the package. Doing so also implies the measurement of the voltage drop across the interconnections and bond-wires.

These effects become important at high currents and will introduce a large error in the estimated temperature, up to \( \pm 30^\circ \text{C} \). A possible solution to this is to use a correction factor, but this solution only stands for ideal conditions.\( (\text{M. Held, 1997}) \)

Another possible improvement of the method is to measure the \( V_{DS} (V_{CE}) \) twice, at two different gate voltages -15V and 13V- and the difference between the two is
used as a new TSEP. This new parameter will reduce the resistance contribution to zero and will be unaffected by any defects inside the switch.

The need of using a gate driver that can actually provide 2 different stable voltages is what actually makes this option non suitable for the market, due to the too high costs of implementation.

In addition to this, the measured IV characteristic has also some dependencies from other parameters:

The gate voltage dependence depends on the driving circuit, since it is the one who must be able to keep a constant voltage.

The current dependence is instead even more difficult to control, since that a variation of it implies variation of the sensibility of the measurement. This can be a negative dependency at low currents to a positive dependency at high currents, as it can be seen from the pictures below.

![Figure 2.6: Variation of sensibility of the measurement system due to current and gate-voltage variation](image)

The last problem can be the accuracy of the current sensor. From the table below it can be seen that a variation of 0.5% of the current can produce a discrepancy of 4°C in the measure.

<table>
<thead>
<tr>
<th>Current close to 80A</th>
<th>Current close to 100A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current (A)</td>
<td>79.8</td>
</tr>
<tr>
<td>Estimated temperature (°C)</td>
<td>111.2</td>
</tr>
</tbody>
</table>

Data from IFSTTAR, LTN

### 2.2.3 Dynamic Characteristics

The dynamic characteristics are another option of collecting the junction temperature. Three methods have been developed up to now to estimate the temperature of the dye, and these are the turn-on delay, the turn-off delay and the current slope during turn-on. (M. Held, 1997)

All of these measurements require a really fast sensor that must have the sensitivity of at least $\text{ns}/°\text{C}$ or $\text{ps}/°\text{C}$, depending on the power switch used, and this means high costs.

In addition to the high cost, the problem with these is that they are very dependent on a variety of variables, such as temperature, DC voltage, load current, control strategy, and fluctuations in gate driver performance.

These methods are simply not feasible.
2.3 Calibration requirements

Before using an electrical parameter to sense the temperature, it is necessary to know its relationship with the temperature.

The linearity of a TSEP is a good indicator of the time needed to process it. (W. Wu and Birolini, 1995)

If the parameter has a good linearity, it only requires a few points to calibrate the sensor, for example the $V_{CE}$ low varies linearly with the temperature, so the calibration is relatively easy.

Another indicator of the quality of the used TSEP is how the sensibility of it changes from a device to another. In a power converter a lot of devices are used, and it would be really useful to have the same sensitivity for every device. In this way a single calibration would be needed for the whole circuit. This again is the case of $V_{CE}$ low, that has a sensitivity of $-2mV/°C$ with little variation to one device to another.

The problem is that most of TSEPs have variations between devices, like $V_{TH}$ that varies a lot from a device to another, and they don’t remain constant as the devices age. (Fig. 2.7)

These changes in the TSEPs due to other parameters means that periodic calibrations must be done during the lifetime of the devices.

Some of this TSEP vary so much with other variables besides the temperature, that they can also be used as sensors for those variables too, like the failure predicting capability of the $V_{CE}$ or the module’s thermal resistance $R_{TH}$.

2.3.1 Vce as failure-predictive sensor

Repeated thermal cycling leads to stress that results in degradation of the bondwires and eventual lift-off from the semiconductor die itself. The failure of a single or small number of bondwires can alter the current distribution in the module and increase ohmic resistances. (Fig. 2.7)

If operation of the device is not halted before a suitable threshold, catastrophic failure can occur that can manifest itself in a number of ways. This could include melting of the remaining bondwires, thermal runaway in paralleled semiconductors, or triggering of parasitic events that lead to device destruction.
2.3. Calibration requirements

Figure 2.8: Failure mechanism inside a power switch

The failures prediction is then a really interesting field since that a system can be fixed before a breakdown occurs.

An active area of research in power module reliability is the development of condition monitoring systems, in particular the focus has been posed on monitoring electrical parameters that indicate degradation. In particular the collector-emitter voltage ($V_{CE}$) at high current in IGBTs and the evolution a module’s thermal resistance ($R_{th}$) have been studied since the 1990s.(1)

While these parameters readily observe degradation in laboratory conditions, they are ultimately influenced by numerous failure mechanisms. As such, they are difficult to use as a standalone parameter to monitor device degradation.

This is especially true for the $V_{CE}$ at high current, which can be effected by gate oxide integrity, bond-wire fatigue, quality of electrical connections, and surface metallisation reconstruction. This manifests in ageing trends for $V_{CE}$ that are not consistent: increases of 5%, 7% and 20%.

As a result, interpreting parameters of this nature requires a thorough understanding of the relationship between the parameter, health condition, and operational profile.

As a first principle, the degradation parameter can be obtained alongside with an accurate real-time junction temperature. From the variations in time of $V_{CE}$, it is possible to have both the knowledge on the temperature as well as assess which failure mechanism is dominant in the device, or more precisely determine when a degradation parameter signals a critical level of degradation.(1)

The gradual increase of $V_{CE}$ could be due to aluminium reconstruction increasing the ohmic sheet resistance, or degradation in the thermal path contributing to a gradual increase in $T_j$. On the other hand, sharp step increases in the $V_{CE}$ can often be seen when a bond wire lifts off from the IGBT.

Therefore, the $V_{CE}$ can be used as a multi purpose parameter that can indicate both the temperature and the degradation of an electronic device.
Chapter 2. State of the art

Figure 2.9: In the first image an increase of $R_{TH}$ during ageing test with $V_{CE}$ compensation (red) and without the compensation (blue). In the second one $V_{CE}$ during accelerated ageing test can be noticed: step change indicates bondwire lift-off.

2.4 Comparison

<table>
<thead>
<tr>
<th>Method</th>
<th>Device</th>
<th>Dependents</th>
<th>Additional Comments</th>
<th>Comments</th>
<th>Linearity</th>
<th>Required Sensing Resolution</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Short Circuit Current</td>
<td>IGBT</td>
<td>T, V</td>
<td>Induces a Hard Switching Fault to create short circuit.</td>
<td>Very Low</td>
<td>Good Linearity</td>
<td>Depends on device (0.15% of max $I_{max}$ per °C)</td>
<td>[59]</td>
</tr>
<tr>
<td>Saturation Current</td>
<td>MOS Transistors</td>
<td>T, V</td>
<td>Partially turns on the device with a low gate voltage during the off-state</td>
<td>Unknown</td>
<td>Non-Linear (Exponential)</td>
<td>Varies depending on temperature range</td>
<td>[34]</td>
</tr>
<tr>
<td>$V_{TH}$ (TJ)</td>
<td>Transistors and Diodes</td>
<td>T</td>
<td>Requires specific current low current level. Requires interruption to normal load current</td>
<td>Low (when load current comes close to 0A or interrupting operation)</td>
<td>Good Linearity</td>
<td>2mV/°C in silicon devices</td>
<td>[21][50][51][52][53]</td>
</tr>
<tr>
<td>$V_{TH}$ (TJ)</td>
<td>IGBTs, MOSFETs</td>
<td>T</td>
<td>Possible disconnection of the device from power circuit May require increased gate resistor Dependence on load current according to extraction method</td>
<td>Depend on measurement circuit</td>
<td>Good Linearity</td>
<td>May require measurement synchronisatio accuracy in nanoseconds</td>
<td>[54][55][56][57]</td>
</tr>
<tr>
<td>Static characteristics $V_{T(0)}$</td>
<td>IGBTs, MOSFETs</td>
<td>T, I, $V_{GE}$</td>
<td>Requires very accurate current sensors Generally inaccurate temperature measurements</td>
<td>High (each on-state)</td>
<td>Good Linearity</td>
<td>±2-3mV/°C Sensitivity depends on current level and device type</td>
<td>[62][63][64][65][66][67][68]</td>
</tr>
<tr>
<td>IGBT Turn-Off</td>
<td>IGBT</td>
<td>T, I, V, $V_{GE}$</td>
<td>Dependent on a high number of inherent electrical variations</td>
<td>High (Each Switching Cycle)</td>
<td>Good Linearity</td>
<td>ns/ps per °C</td>
<td>[72][73][74][69][75][76][78]</td>
</tr>
<tr>
<td>Turn-On Delay</td>
<td>MOS Transistors</td>
<td>T, V, $V_{GE}$</td>
<td>Closely related to $V_{TH}$ High (Each Switching Cycle)</td>
<td>Good Linearity</td>
<td>ns/ps per °C</td>
<td>[69][70][71]</td>
<td></td>
</tr>
<tr>
<td>Rise-Time</td>
<td>MOS Transistors</td>
<td>T, I, V, $V_{GE}$</td>
<td>Dependent on a high number of inherent electrical variations High (Each Switching Cycle)</td>
<td>Good Linearity</td>
<td>ns/ps per °C</td>
<td>[69][71]</td>
<td></td>
</tr>
</tbody>
</table>
2.5 New method: Peak gate current - $I_{Gpeak}$

The new method that is about to be exposed is called Peak gate current - $I_{Gpeak}$. This method consists of detecting the peak voltage over an external gate resistor during the turn-on delay.

This voltage is then used to calculate the peak current that flows in the circuit, and from the knowledge of that and the gate driver voltage, the total resistance of the current path is known as well as the internal gate one.

The internal gate resistance is the temperature sensitive electrical parameter - TSEP- that will be used in the project. This method has been chosen because it has a lot of advantages respect to the previous ones analysed:

- the measurement circuit can be integrated into a gate driver
- it is immune to load variations
- it has a linear relationship with temperature
- it doesn’t disruption the operations of the power converter

These statements will be compared with the experimental results.

2.5.1 Theoretical recalls

Internal Gate Resistance - $R_{GINT}$

The $R_{GINT}$ is the distributed internal gate resistance of MOSFETs or IGBTs, and its dependence to the temperature is a consequence of the variations in the resistivity of the polysilicon, the material chosen for manufacturing these components. In power MOSFETs, where a single device is composed by a lot of MOSFETs connected in parallel, the resistance is often increased by the manufacturer to improve current sharing and to damp high frequency oscillations.

The problem with this TSEP was that at the beginning a MOSFET with a modified substrate was required in order to sense the resistance. The substrate was modified in order to add another pin to connect a second probe to set a current through the gate resistor. A constant current of 500mA was then applied to the internal gate resistor and the voltage drop across it had the information of the temperature needed for the measurement.
Introduction in switching phases

Since that the cost of a modified power module with 4 terminals is not negligible, another method to sense the internal gate resistance has been found. To understand how the new measurement is performed inside a standard power module (with just 3 terminals), a small introduction in the switching phases in power electronics has to be done.

Taking as a model the buck converter, it can be analysed by focusing on the voltage across the diode that behaves like a square wave generator with a second order filter with a low cut-off frequency at the final stage. Idealizing the filter so that the filtering action is perfect, the output value will be almost constant and of course also the current will be constant as well.

During the MOSFET turn-on, since that transitions are realised in a very short time, the current in the inductor and the voltage across the capacitor remain steady during this time. The inductor can then be approximated to a constant current source (with $I_{ON}$ being the value of the steady state current in the inductor) and the capacitor to a constant voltage source (with $V_O$ being the steady state value of the output voltage).()

The MOSFET is then modelled as the blue parts in the scheme below:

A dependent current generator $i_{DS}$ when it is in saturation and as a resistor $R_{DS_{ON}}$ when it is in the linear region, and the parasitic capacitances between the various terminals.

After applying this approximation to every topology, some manipulations of the circuits lead to a single circuit valid for all the topologies, the model of the simplest hard-switching power converter during a transition.(Due, 2011)
2.5. New method: Peak gate current - \( I_{G_{peak}} \)

In this representation, \( R_{G_{ON}} \) represents the total turn-on resistance of the gate MOSFET, \( R_{G_{OFF}} \) represents the turn-off one and as already explained before, the constant current generator and the constant voltage generator are respectively the inductor and the capacitor of the circuits.

The turn-on of the MOSFET implies that the input capacitances are being charged and the output one has to be discharged.

Note that the capacitors in a MOSFET are not fixed, they change with the drain-source voltage \( V_{DS} \).

The figure below will clarify how they change.

![Diagram of a simple power converter during a hard-switching](image)

**Figure 2.12:** Model of a simple power converter during a hard-switching

![Graph showing Ciss, Coss, and Crss varying with V_{DS}](image)

**Figure 2.13:** Ciss, Coss and Crss varying with the drain-source voltage
Chapter 2. State of the art

The names of the capacitances reported in the graph have the notation used in power electronics, but they can be expressed respect to the normal ones:
- \( CRSS = C_{gd} \) (\( CRSS = \) small signal reverse transfer capacitance)
- \( CISS = C_{gs} + C_{gd} \) (\( CISS = \) small signal input capacitance when drain and source terminals are shorted)
- \( COSS = C_{ds} + C_{gd} \) (\( COSS = \) small signal output capacitance when gate and source terminals are shorted)

To greatly simplify the calculations, an approximation is done:
The capacitors values are considered constant up to a certain \( V_{DS} \) threshold, then they abruptly change to another value when that value has been passed.

![Diagram showing capacitance variation with \( V_{DS} \)]

**Figure 2.14:** Approximation with an abrupt variation of the MOSFET capacitances

Using this approximation it is easier to understand how the turn-on or the turn-off of a MOSFET works, since that the capacitor can be considered as normal ones. The turn on waveforms of the MOSFET during a hard-switching are now reported below
2.5. New method: Peak gate current - $I_{G\text{peak}}$

To have a better understanding of the turn on phase from 0 up to $t_1$ -the only interval needed- the model of the circuit during this time is reported below.

![Diagram](image)

**Figure 2.16**: Model of a power converter during the first stage of a hard-switching turn on

At the beginning of the turn-on, when the switch is still off, the diode is conducting ($I_{\text{DIODE}} = I_{ON}$).

Until the gate-source voltage $v_{GS}$ doesn’t get to $V_{TH}$, the transistor isn’t turned on, so the dependent current generator that models it is off.

Moreover, to turn off the diode the current in the MOSFET $i_{DS}$ has to be greater than $I_{ON}$, in order to carry all the needed current.
Since that the diode is on, ideally the voltage across its terminal is 0 so $V_{OFF}$ is also applied to the capacitance $C_{ds}$. This is why the voltage $v_{DS}$ remains high during this first period.

Since that the drain-source voltage $v_{DS}$ remains steady at the maximum value $V_{OFF}$ during all this period, the approximation of the capacitances is well verified. In addition to this, since that at first the capacitance $C_{gs}$ is discharged ($v_{GS} = 0$), using Kirchhoff leads $C_{gd}$ to be negatively charged at $-V_{OFF}$.

At the beginning, when the voltage is applied to the gate of the transistor, both the capacitors $C_{gs}$ and $C_{gd}$ start to charge with the current supplied by the gate driver. Using Kirchhoff’s current law and the capacitor behaviour brings to

\[
\begin{align*}
\left\{ i_G(t) &= i_{GS}(t) + i_{GD}(t) \\
i_C(t) &= C \frac{dv_C(t)}{dt}
\right.
\end{align*}
\]

(2.1)

And by substituting the second one into the first one, one gets

\[
i_G(t) = i_{C_g}(t) + i_{C_d}(t) = C_{gs} \frac{dv_{GS}(t)}{dt} + C_{gd} \frac{dv_{GD}(t)}{dt}
\]

(2.2)

At last, if Kirchhoff’s voltage law is used

\[-v_{GS}(t) + v_{GD}(t) + v_{DS}(t) = 0
\]

(2.3)

and substituting $v_{GD}(t) = v_{GS}(t) - v_{DS}(t)$

\[
i_G(t) = C_{gs} \frac{dv_{GS}(t)}{dt} + C_{gd} \frac{d(v_{GS}(t) - v_{DS}(t))}{dt}
\]

(2.4)

Since that the voltage $v_{DS}$ is clamped, it means that it isn’t time dependent and so its derivative respect to time is 0. The total gate current is then

\[
i_G(t) = C_{gs} \frac{dv_{GS}(t)}{dt} + C_{gd} \frac{dv_{GS}(t)}{dt} = (C_{gs} + C_{gd}) \frac{dv_{GS}(t)}{dt}
\]

(2.5)

The two capacitors act like they are connected in parallel even though they are not and they are at 2 different voltages. They also start to charge with the same voltage derivative $\frac{dv_{GS}(t)}{dt}$ with the time constant that is $\tau = R_{GON}(C_{gs} + C_{gd})$.

This means that when the transistor is at the very beginning of the turn-on (until $v_{GS} < V_{TH}$), the capacitors $C_{gs}$ and $C_{gd}$ behave like they are connected in parallel.

### 2.5.2 $R_{GINT}$ Measurement on Standard Power Modules

Now that the model of the MOSFET during the very beginning of the turn-on phase is known, the model from the gate side of the transistor has to be obtained.

The MOSFET is still considered in the OFF-state, so from the previous section it is known that the input capacitors can be considered in parallel, so to ease the model, the voltage of the capacitor $C_{GD}$ will be referred to the source as $C_{GS}$.

An external inductance is also added to have a more generic model that can take into account another problem that will be discussed soon.

In addition to this, the total gate resistance $R_{GON}$ is divided in the internal one, inside the MOSFET -$R_{GINT}$-, and the external one -$R_{GINT}$-.

The circuit model obtained now is a simple RLC circuit, so when a sinusoidal waveform at the resonance frequency is injected, the reactance of the series can be neglected and only the total gate resistance is sensed.
2.5. New method: Peak gate current - $I_{G\text{peak}}$

The knowledge on the value of the resistor brings then also the knowledge on the temperature. Since that from the gate side of the transistor the model is the same for both IGBTs and for MOSFETs, this measurement has been recently proposed as a sensing method for an IGBT using a special gate driver.

The driver that will be used to turn on the device has also to be capable of generating a sinusoidal waveform at high frequency when the transistor is in the off state -so the considered model is the same as the one that has just been developed-, in order to sense its temperature through the measurement of the total gate resistance.

The problem is that having such a driver means higher costs for the project. Moreover, measurements performed with some high-end RLC meter requires around 20ms to be completed, and during this time the transistor has to be kept in the off-state; this would be a strict boundary for any project.

The last problem is then that the parasitic gate inductance has to be taken into account in order to select the correct resonance frequency. A random high frequency
won’t be enough, since that it has to be really close to the resonant frequency of the circuit in order to sense the resistance correctly, so this method also requires specific calibration for every device used.

The need of having a specialized gate driver circuit capable of generating a sinusoid at a specific high frequency when it is in the off-state removes the advantages of having a standard transistor rather than the one with the modified substrate.
2.6 \( I_{\text{Gpeak}} \) Measurement Principle

To overcome the previous problems, a new approach has been developed to sense the internal gate resistance based on the same RLC circuit that has been explained, but simplifying the gate inductance under proper conditions.

The conditions can be obtained by the analysis of the impedance transfer function of the system:

\[
Z(s) = R + sL + \frac{1}{sC} = \frac{1 + sRC + s^2 LC}{sC} = \frac{1 + \frac{2\xi}{\omega_0} s + \frac{s^2}{\omega_0^2}}{sC} \tag{2.6}
\]

with \( \omega_0 \) and \( \xi \) being the angular frequency and the damping factor of the transfer function.

The system can be approximated into a first order circuit if the poles of the system are not conjugates but divided and far away from each other. This implies that the damping factor has to be big, with the module much greater than 1 -that is the value at which the 2 poles are joint but not conjugates.

\[
\xi = \frac{R}{2} \sqrt{\frac{C}{L}} \gg 1 \quad \Rightarrow \quad L \ll C \frac{R^2}{4} \tag{2.7}
\]

That means that if the gate inductance is kept low, the response from the gate side of the system can be simplified into a first order one with just the resistors and the capacitors.

This is the final model of the circuit that will be used to sense the MOSFET temperature.
Chapter 2. State of the art

The external gate resistance is assumed to have insignificant temperature dependence and in any case the temperature of it won’t reach high values, since that just the gate current would flow through it.

The gate capacitances are considered stable until $v_{DS} = V_{OFF}$ (that happens when $i_{DS}(t) \geq I_{ON}$ - the steady state value of current in the inductor -); even if they were to change with the temperature, the $I_{GPEAK}$ shouldn’t change since that it is theoretically independent from the capacitors values.

Finally, under the condition that the gate driver delivers a fixed step voltage, any fluctuations of the initial peak of the gate current would be caused just by variations of $R_{GINT}$ with the temperature.

An increase of this resistance due to temperature will reduce the magnitude of $I_{GPEAK}$, therefore it provides a suitable observation point for the temperature dependent variation of $R_{GINT}$.

The response of the current in this RC circuit to a step input voltage is then described by the equation

$$I_G(t) = \frac{V_{GS}}{R_{GON}} e^{-\frac{t}{R_{GON}C}}$$

(2.9)

And this is the exact behaviour that can easily be seen from the graph of the turn on phase of the transistor, in which the peak of the gate current $I_{GPEAK}$ obtained when the time approaches 0,

$$I_{GPEAK} = I_G(t \Rightarrow 0) = \frac{V_{GS}}{R_{GON}}$$

(2.10)

depends just from the gate voltage and the total gate resistance $R_{GON}$ (the internal one inside the MOSFET $-R_{GINT}$, plus the external one $-R_{GEXT}$).

This method has already been tested in the lab with high power IGBT devices, showing a consistency in the method, but it has never been tried using MOSFETs nor in a real switching converter.

Moreover the circuit used to sense it was not a feasible solution to be implemented for each transistor in a power converter.

The objective of the thesis is now to use this method to gain the information of the temperature inside a MOSFET in a switching environment.
Chapter 3

Design

Detecting the $I_{G_{PEAK}}$ while being in line with the design specification (the sensing circuit that has to be small, cheap, with low-power consumption) has been the focus of the design.

Since that voltage across the resistor $R_{G_{EXT}}$ isn’t sensed respect to the reference, a differential amplifier configuration will be used in order to sense it.

After the differential circuit, a peak detector circuit will be used. The circuit will sense the output voltage of the amplifier and will store the peak of it inside a capacitor.

The signal stored inside the capacitor will then be sent to an optoisolator that will transfer this information to a Vumeter that will visually give the information regarding the temperature.

The circuit will be implemented inside a basic cell of the MAC Converter, that will constitute the final project.

To test the whole circuit, the basic cell will be used in a Buck configuration using the second transistor as a diode that will be turned on during the off interval of the first one. In this way 2 different measurements of gate current peaks can be performed on the same board.

Each block of the logic scheme will now be explained.
3.1 Control circuit

The first block that will be analysed is the control one.

As it has just been explained, this circuit has to switch on and off the two power mosfets of the circuit board without causing a short-circuit in the powerline, in order to being able to take two different measurements at the same time.

To control the 2 gate driver circuits of the power mosfets, the integrated Regulating Pulse-Width Modulators SG2524 has been chosen.

![Logic scheme of SG2524](image)

From the logic scheme of the SG2524 is it possible to see that it has a lot of functions to control the output voltage. Most of them were exaggerated for the purpose of the temperature measurements, infact that a lot of the pins have been grounded or disconnected, for example the current limiting feature of the device or the internal comparator to regulate the output voltage haven’t been used for this project.

The duty cycle of the circuit is selected by a direct connection of the output of the internal error amplifier (pin 9) to a voltage divider. In this way the voltage level of the internal comparator is externally decided and is fixed by the value chosen by the user. Since that the internal digital logic is supplied with 5V, also the voltage divider must be connected to the same power supply by connecting it to the REF OUT pin (16) of the integrated circuit. This is the output pin of the internal voltage regulator to which a 10kΩ trimmer will be connected. In this way it will be possible to vary the duty cycle of the system. To stabilize this voltage, a capacitor is added in parallel to the comparator pin.

The frequency of the switching activity and the blanking time between the turn-off of a transistor and the turn-on of the other are instead decided by the values of the resistor Rt and the capacitor Ct, using the tables below. In order to work properly, both the resistor and the capacitor will be connected to the ground plane of the board.
3.1. Control circuit

The switching frequency has been chosen from 25kHz down to 2.5kHz, with 1µs of blanking time. To accomplish so, the values chosen for the components have been $C_t = 10nF$ and $R_t = 50k\Omega$. To vary the resistor, a trimmer has been used together with the resistance.

The final control circuit is the following one

This integrated circuit alternatively turns on one of the 2 internal BJTs that will be used as control signal for a following stage, equal to the first one, that is used to invert the control logic. Both the internal and the external transistors have the source connected to ground, and the collector connected to 5V through a pull-up resistor. In this way when the first internal transistor is on the "HIGH" logic state, it is turned on. But this means that the collector voltage of the internal transistor is grounded, so on the "LOW" logic state. This behaviour is not acceptable, since that in this way -with the inverted logic- a short circuit between the power transistors will surely occur. To avoid this the second stage equal to the previous one is added to invert the logic again. The output of this last stage is then sent as a control signal to the gate driver.
3.2 Gate driver

The second circuit is then the Gate driver.

This circuit uses a Gate Drive Optocoupler HCPL-316J, an integrated circuit with the control part optically insulated from the high voltage one.

![Diagram of Gate Drive Optocoupler HCPL-316J](image)

This IC is divided in two insulated parts: the low voltage control one is from pin 1 up to pin 8, while all the other pins are at high voltage.

To describe how this IC works, the pins of the lower voltage part are now described:

- $V_{CC1}$ and $GND1$ are the power supply pins.
- At the $V_{IN+}$ pin of the circuit, the control signal will be connected. Since that the board is thought to be used as a basic cell of the MAC converter, also the possibility to add an external control through a jumper is added.
- The $V_{IN-}$ pin is instead connected to the ground plane, to have a correct negative reference that will be compared with $V_{IN+}$.
- Also this pin could be used together with the previous control circuit without adding another stage at the output of it, making things easier. The point is that this board is mainly thought to work as a MAC cell rather than being used as a buck converter, so if the external control is added in the positive pin, this would maintain the logic of that control.
- The pin $V_{LED1-}$ is connected to ground in order to switch on the LED diode that will be used to transmit the turn on information to the high voltage part of the circuit.
- The pin $V_{LED1+}$ is left disconnected since an external control is not used.
- The reset and fault pins are instead respectively an input that resets the gate driver if it is in a faulty state, and an output that can be connected to a led to have a visual information about the state of the HCPL-316J.

The high voltage side pins of the gate driver are instead as follows:
3.2. Gate driver

$V_{CC2}$ and $V_{EE}$ are the power supply pins.

The pins $V_E$ is connected to $V_{EE}$ in order to have the Under Voltage Lock-Out protection. This is a protection useful when the power supply of the high voltage part is not capable of supplying the high current spikes needed to turn on the power MOSFET, so the voltage at the end is lowered too much respect to the nominal value. If the circuit detects that $V_{CC2} - V_E < UVLO$, then an under voltage in the power supply voltage is happening and the output of the gate driver is prevented from supplying the gate of the driver.

$V_C$ is the terminal from which the power to supply the gate of the transistor is taken. It is connected together with $V_{CC2}$.

The DESAT pin in instead a pin useful when an IGBT is used. It checks if the IGBT is working in saturation and stops the circuit in order not to damage the power device.

At the end, the pin $V_{LED2+}$ is left unconnected since that no external fault conditions have to be set.

The following figure is the final gate driver circuit

![Gate driver circuit](image)

The following figure is the final gate driver circuit

The remaining part of this circuit that is still to be explained is the power supply of the high voltage part of the circuit, on the right side of the circuit.

The working principle of this circuit is easy.

The $V_{DRAIN}$ yellow port is the actual connection to the drain of the transistor, while the $REF1$ is the connection to the source. $VCC1$ is the voltage of the capacitor $C_{56}$ refer to the source, used to power up all the circuit.

The zener diode, polarized through the R16 resistor, provides the voltage to the gate of the charging transistor Q3.

When this happens, the transistor starts to conduct the current needed to charge the capacitor C56 until the voltage on the source of the transistor is equal to $V_{ZENER} - V_{TH} - 2V_{DIODE}$. When this happens, the MOSFET stops conducting and the capacitor is charged. The current cannot flow in the opposite way because of the reverse polarity of the two diodes.

A thing to notice is that the current that flows through the circuit is absolutely non constant since that the circuit can charge the capacitor only when the power transistor is in the off-state. The resistor between the drain and the source is there just to clamp the voltage of the nodes when the device is in the off state.

Now, with the power supply circuit explained, the next circuit to be designed is the temperature measurement one.
3.3 Temperature measurement

3.3.1 $R_{G\text{INT}}$ Laboratory Measurements

The first thing that is useful to understand before starting to design the circuit is to understand the order of magnitude of the internal gate resistor $R_{G\text{INT}}$ of the used mosfets and how it varies from a device to another.

To do so, six power MOSFETs -the ones that were already used in the MAC converter- have been tested in the lab and their result have been used to design the remaining part of the circuit.

![FDPF3860T N-Channel PowerTrench® MOSFET](image)

To perform the measurements, a Solartron SI 1260A Impedance / Gain-Phase Analyzer is used.

This instrument can reach a frequency up to 32MHz and it gives information regarding the amplitude and the phase of an analysed impedance. The user has just to provide the model of the connected impedance (series connection of a resistor and an inductor, or a parallel combination of a resistor and a capacitor) and the instrument will provide the values in a format module/phase or resistance/capacitance-inductance.

To measure the value of $R_{G\text{INT}}$, the drain and the source of the MOSFETs have been shorted in order to have the parallel combination of the capacitors equal to the one used in the model obtained.

The main difference of this circuit respect to model used is that the capacitances have higher values (Figure 2.14), since that $V_{DS}$ is now 0 and not $V_{OFF}$. By the way, the values of the capacitances don’t influence the internal gate resistance, but just the resonant frequency of the circuit.
3.3. Temperature measurement

However, to reduce at the minimum the possible measurement error of the Impedance Analyser, the chosen starting frequency has always been close to the resonance one (for all the devices it was close to 6MHz).

To heat up the component at the proper temperature, the soldering station MBT 250-SDT have been used, since that is has an optimum temperature regulator.

At the end, to know the temperature of the MOSFETs, 2 Multimeter Meterman 33XR have been connected to their thermocouples. The 2 have been used to sense the temperature at the gate pin of the transistor and at the pointer of the soldering station, to have the same resolution of measurements and to evaluate the thermal resistance of the package.

The measurements have been collected for both the heating phase and the cooling one. A discrepancy between the results can be noticed due to the fact that the measurement on the gate pin of the MOSFET is not perfect since that it has still some thermal resistance from the junction temperature to the output connector.

The results of the measurements are in the images below.

The average sensitivity found with this method is of $32 \, \text{m}\Omega / ^\circ\text{C}$, with a variance that in the worst case is of $7 \, \text{m}\Omega / ^\circ\text{C}$. This means that, as an average, $R_{G_{\text{INT}}}$ will have a variation of $0.32 \, \Omega$ for $100 \, ^\circ\text{C}$ of temperature excursion and that the variance of the gain could induce an error up to $20 \, ^\circ\text{C}$, if it is not calibrated for each device.

Taking into account just the devices FDPF3860T, the variance is reduced to $2 \, \text{m}\Omega / ^\circ\text{C}$. Such a small variance is not enough to require the calibration of all the sensing circuits that are present in a converter, but the point is that since that only 3 transistor have been tested, this cannot be considered valid for a proper statistic. The circuit will then require a potentiometer to vary the gain of it, in order to change the slope of the temperature respect to the resistance.

The shifting value also requires calibration in order to use this method as a measurement for the temperature, since that a low value of resistance for a transistor could be a high value for another one.

The last important thing that is visible from the graphs is that the $R_{G_{\text{INT}}}$ increase its value as the temperature increases. By sensing the current, since that the total resistance of the current path will increase, the final sensed peak will lower down as the temperature increases.
Figure 3.8: $R_{GINT}$ measured for 3 different transistors respect to the temperature, for both the heating phase and the cooling one.
3.3. Temperature measurement

Figure 3.9: $R_{G\text{INT}}$ measured for 3 different transistors respect to the temperature, for both the heating phase and the cooling one.
3.3.2 Differential Amplifier

Now that the value of the internal gate resistor is known, the Differential Amplifier can be designed.

External gate resistor

The first thing of the differential structure that will be chosen now is the value of the external gate resistor, \( R_{\text{GEXT}} \).

The peak of the voltage measured across its terminals is

\[
V_{R_{\text{GEXT}}} = V_{\text{DRIVER}} \frac{R_{\text{GEXT}}}{R_{\text{GEXT}} + R_{\text{GIN}}} \tag{3.1}
\]

From this formula is easy to understand how a small value of the voltage of \( R_{\text{GEXT}} \) would be useful to increase the resolution of the measurement, even though too low one would break the power switch due to high gate currents. The chosen value for this resistor at the end has been a compromise between the two needs, 10\( \Omega \).

In addition to this, the resistance has been chosen to be really stable in temperature, so that it won’t affect the measurements.

Operational Amplifier

After the external gate resistor, the operational amplifier is the next component that is designed.

The best configuration that could be used to sense a voltage between two nodes at a different potential would be an Instrumentation Amplifier.

The problem with this structure is that since it is composed by a cascade of two op-amps, the total bandwidth is limited due to stability reasons, so a normal operational amplifier is the preferred choice.

By the way the focus points for the selection of the amplifier have been the supply voltage, the slew rate and the bandwidth.

For the supply voltage, since that the circuit will be supplied by the power supply circuit explained before, it was already fixed to a single supply voltage of 18 volts.

After this, the slew rate was the next parameter.

It was not possible to obtain this parameter from any data sheet, since that it is the non-idealization of the formula

\[
I_G(t) = \frac{V_{GS}}{R_{\text{GON}}} e^{-\frac{t}{R_{\text{GON}}C}} \tag{3.2}
\]

when real components are used. The point is that the current cannot be discontinuous and jumping from 0 up to the value \( \frac{V_{GS}}{R_{\text{GON}}} \) at the time 0, but it has still to be continued, no matter how fast is the signal to rise.

The only available document to estimate this parameter was from the IGBT’s measurement performed in the PHD thesis from which this thesis is based on, where the minimum slew rate seen from the graphs to perform correctly the measure was of 1.5\( kV/\mu s \).

The bandwidth of the system has instead been estimated using a famous thumb rule that from the rise time of the input waveform, which was of about 100\( ns \), could obtain the minimum required bandwidth of the system to correctly sense the signal. The thumb rule is the following
3.3. Temperature measurement

\[ BW = \frac{0.35}{100_{\text{Hz}}} = 3.5\text{MHz} \quad (3.3) \]

A good trade off between benefits and costs of the final project has been the choice of an operational amplifier with a bandwidth of 100MHz of GBW, the LM6172.

![LM6172 Data Sheet](image)

**Figure 3.10**: Data sheet of the integrated circuit LM6172

**Differential structure**

Now that the OP AMP is decided, the gain of the differential structure has to be fixed.

Since that every power switch has a different internal resistance from the others, to have a starting reference the circuit will be designed tailored on the MOS2 of the figure 3.8, so that the minimum \( R_{G\text{INT}} \) is 1.7\(\Omega \) and the maximum is 2.0\(\Omega \).

Then, when \( R_{G\text{INT}} \) is minimum, the voltage over the external gate resistor is

\[ V_{R_{G\text{EXT}m}} = V_{\text{DRIVER}} \frac{R_{\text{GEXT}}}{R_{\text{GEXT}} + R_{G\text{INT}m}} = 15 \frac{10}{10 + 1.7} = 12.82V \quad (3.4) \]

On the other hand, when \( R_{G\text{INT}} \) is maximum, the voltage is

\[ V_{R_{G\text{EXT}m}} = V_{\text{DRIVER}} \frac{R_{\text{GEXT}}}{R_{\text{GEXT}} + R_{G\text{INT}M}} = 15 \frac{10}{10 + 2} = 12.5V \quad (3.5) \]

At the end the peak variation from the \( R_{G\text{INT}m} \) to the \( R_{G\text{INT}M} \) is

\[ V_{R_{G\text{EXT}m}} - V_{R_{G\text{EXT}m}} = 12.82 - 12.5 = 320mV \quad (3.6) \]
This will be the signal that will bring the information regarding the temperature inside the power switch.

In order to use it, an amplification of this signal is required. To have \( V_O = 15V \) at the output when the input is \( V_I = 320mV \), a gain of 37.5 is needed.

Now a consideration regarding the bandwidth of the chosen OP AMP has to be made. The point of this is that maybe the amplifier won’t have enough bandwidth to sustain a high gain (37.5) for high frequencies, and so it won’t sense the peak perfectly. Actually, to keep the final costs of the project low, even a high distortion caused by a low gain for high frequencies wouldn’t be a problem since that at most the peak would be lower than expected.

Anyway with such a gain if the output of the op amp wouldn’t saturate at the output of the differential structure there would be a voltage of

\[
V_{O_{R_{G_{EXTm}}} = GV_{R_{G_{EXTm}}} = 585V}
\]

when the internal gate resistor is minimum, and

\[
V_{O_{R_{G_{EXTM}}} = GV_{R_{G_{EXTM}}} = 600V}
\]

when the external gate resistor is maximum.

So, to avoid the saturation of this first stage, an offset of 585V is required in order to have the output signal from 0 up to 15V. Of course this high value will be accomplished by selecting a high gain for a lower constant signal at the input, that will be calibrated correctly to produce the desired high output offset.

After the gain and the offset, the following step has been to choose the structure of the differential amplifier, in order to have in a single stage both the gain and the shift of the waveforms.

![Figure 3.11: The differential amplifier at the input stage of the circuit](image)
3.3. Temperature measurement

The circuit above has to be carefully designed in order to be able of subtracting and amplifying in the same way the signals $V_1$ and $V_2$, while the signal $V_3$ is then used to have the offset to shift up or down the final waveforms.

The point is that a differential amplifier needs to have exactly the same gain for both $V_1$ and $V_2$, in order to make the correct difference and amplification between the two.

The condition that has to be satisfied is that

$$\frac{V_o}{V_1} = \frac{R_1/\sqrt{R_3} + R_2}{R_1/\sqrt{R_3} + R_B} = \frac{R_2}{R_1} \quad (3.9)$$

By equating the second term with the third one and leaving just $R_B$ on the left side, one gets

$$\frac{R_B}{R_A + R_B} = \frac{R_2}{R_1} \frac{1}{\sqrt{R_3} + \frac{R_1}{\sqrt{R_3}}} = \frac{1}{R_1 + \left(\frac{R_1}{R_3}\right)} = \frac{1}{R_1 + \left(\frac{R_1 + R_3}{R_1}\right)} \quad (3.10)$$

Now, by inverting both the terms, the following formula is obtained

$$\frac{R_A + R_B}{R_B} = \frac{R_1}{R_2} + \left(\frac{R_1 + R_3}{R_3}\right) = \frac{R_1}{R_2} + \frac{R_1}{R_3} + 1 \quad \rightarrow \quad R_A = R_B \left(\frac{R_1}{R_2} + \frac{R_1}{R_3}\right) = R_B \left(\frac{R_1}{R_2/\sqrt{R_3}}\right) \quad (3.11)$$

From this last equation, the value of $R_A$ and $R_B$ are found

$$\frac{R_A}{R_B} = \frac{R_1}{R_2/\sqrt{R_3}} \quad (3.12)$$

Now that all the proportion between the resistors are known, the gain needed for the circuit can be provided directly by the subtractor by setting the gain $G$ equal to

$$G = \frac{R_2}{R_1} = 37.5 \quad (3.13)$$

To accomplish that, the chosen values of the resistor are $R_1 = 18k\Omega$ and $R_2 = 680k\Omega$.

The same gain is also chosen for $V_3$, so that an input signal of 12.5V is required to have 585V at the output. This constant voltage is obtained with a voltage divider connecting it to the circuit power supply.

At the end, this is the circuit designed as a first stage of the sensing circuit.
This circuit has been simulated varying the $R_{G_{INT}}$ from 1.7Ω up to 2.0Ω, and the output is has been plotted in the graph below. In the graph it can be seen both the voltage across the external gate resistor and the output voltage of the differential amplifier (the high peak at the beginning).

From the figure above it is clear how the circuit works and it is interesting to see also how the negative peak exists due to the current to discharge the gate of the device but that it doesn’t affect the principle of the circuit, since that the offset is too low and the op amp is supplied just with the positive voltage.

By zooming in the peak region, the result is that as the temperature increases, the output voltage decreases.
3.3. Temperature measurement

The next stage after the differential amplifier is the peak detector.

To design this circuit, a lot of small improvements to a basic circuit have brought to the final one.

The first schematics has been the basic peak detector consisting of a simple diode, a capacitor and a resistor to discharge the capacitor.

![Simplest Peak Detector Diagram](image)

The resistor to discharge the capacitor is fundamental in this circuit since that the maximum temperature corresponds to the minimum peak, if it isn’t added then the capacitor cannot be discharged -not ideally at least- and the transistor would always be cold for the sensing circuit, even if the temperature in increasing.

The simulation output of this is circuit is the following
In this graph the green line is the input voltage and the blue line is the output of the peak detector.

As it can be seen, the output of the circuit slowly goes to the peak, because as the current in the diode lowers down, as well the voltage across it lowers down.

But still this diode is nearly an ideal one, a real diode would have a non negligible turn on time that wouldn’t manage to be that fast.

The first improvements done to the circuit are then to remove the voltage drop of the diode by adding an operational amplifier to it, and to decouple the output of the circuit from the capacitor, in order to preserve the charge if the capacitor voltage is sensed.

The circuit is then the following

![Figure 3.17: First improvement of the peak detector](image)

By adding the first op amp, the circuit has been completely disconnected from the input and then the voltage drop of the diode is now ideally reduced to 0, since that the output of the op amp will be high -and saturated actually- until $V_+ = V_-$. In this way a fast charge of the capacitor will be achieved, since that now the voltage will be higher.

The second op amp then prevents the capacitor from being discharged by other thing that are not the parallel resistor.

This is the output of the simulation
In this figure the blue line is the input voltage, the red line is the output of the first op amp, and the green one is the output of the peak detector.

As it is clear, now the output of the op amp goes immediately in saturation as the input voltage is higher than the capacitor one. The point is that normally the op amp cannot be so fast to be turned on instantaneously and then turned off in no time again.

A final improvement is then necessary in order to prevent saturation, but first it is mandatory to understand why the saturation occurs.

The saturation occurs due when the condition $V_- > V_+$ is verified. In this case the output of the OP AMP goes immediately to 0 (it is basically saturating to the negative power supply) since that the diode doesn’t allow any current to flow in the opposite direction and acts as an open circuit, so the circuit in this case is basically without feedback.

To change this, the diode and the OP AMP have to be disconnected from the circuit and analysed separately.

If the diode is now flipped, the op amp can now also have intermediate stable voltages, since that if $V_- > V_+$, the output of the amplifier will decrease until the condition $V_- = V_+$ is verified again and so it can reach another stable state. Of course this is valid just if the diode is conducting, so for this solution the back of the diode must be connected to something to keep it polarized.

The point is that now the opposite problem occurs, since that the condition $-V_+ > V_-$ is now an open loop system, due to the fact that the diode conducts no more.

The improvement is to connect the output of the first OP AMP to the cathode of another diode, that will be connected to the capacitor of the peak detector.

Then, to have the feedback in the case $V_+ > V_-$, the final output of the peak detector has to be connected to the negative input of the first OP AMP through a resistor. The purpose of the resistor is to limit the current that will flow through the circuit when the first op amp presents the condition $V_- > V_+$.

The final circuit designed is then this one
And the simulation result is

With the blue line that is the input voltage, the green one that is the output of the first amplifier and the red one that is the output voltage of the peak detector. As it can be clearly seen, the saturation occurs no more. This will be the final circuit that will be used as peak detector.

Now that the circuit has been selected, the components have now to be chosen. As OP AMP the ones already selected for the differential amplifier are still good, since that the input waveform is still the fast one seen before. The other important matter are the diodes. For the circuit some really fast Schottky diodes have been selected (turn on time < 1ns), in order to be able to turn them on fast, since that when the capacitor is almost charged, the time available to charge the capacitor is really tiny.

The last one is the discharge time constant of the circuit. Since that the purpose of the project is not to have an instantaneous temperature sensing -at least not for the moment- but an averaged one, even a time constant of seconds is good for the purpose of the project. The point is that since that there will be a lot of noise due to switching activity in the circuit, having a big capacitor prevents the information to be degraded.
3.3. Temperature measurement

Optocoupler

The information contained in the peak detector has now to be sent to a digital controller or to any other circuits that are at a voltage different that the source voltage of the power transistor.

To accomplish such a purpose, an analogue or digital optocoupler is needed. For this circuit the analogue version is the preferred one, and the linear optocoupler IL300 is the selected component.

![Figure 3.21: Linear Optocoupler IL300](image)

This optocoupler inside its package presents an LED diode that highlights two identical photodiodes connected in a reverse polarization.

In this way the current that flows through the diodes is no more dependent from the reverse voltage applied, since that theoretically it should just be the constant reverse current $I_a$, but it varies just with the temperature and the light.

The two photodiodes are identical, in order to use one of them as a feedback branch.

This circuit is then used as indicated in the application note.
In the application note the LED inside the package is driven by a current generator. The current generator is stable when $V_a = V_b$. $V_b$ is also the voltage across the resistor $R_1$ ($V_b = R_1I_{P1}$), in which the current $I_{P1}$ is flowing. $I_{P1}$ is also the current that flows through the photodiode.

To choose the value of the resistor $R_1$, the relationship between $I_F$ (the LED current) and $I_{P1}$ (the photodiode one) has to be read from the table below.

From this table, it is clear to see that the optocoupler is more linear if used at high values of $I_F$ rather than low ones.
At this point, a minimum voltage is then required in order to have a linear behaviour of the system while the temperature is varying.

The op amp used are actually not rail to rail, so at the output of the peak detector the value will never be 0, but it will be at least one volt.

Anyway the minimum output voltage will then be set at a voltage higher than 0, in order to always work with a good linearity, but being careful of not draining too much current, since that that current is the one drained from the power supply circuit.

In order to drain not too much power (to the cost of losing linearity), the maximum current $I_F$ has been chosen equal to $20mA$.

From the table, the value of the current $I_{P1}$ is selected to be $150\mu A$.

The remaining thing is now to choose the value of the resistor $R_1$

$$R_1 = \frac{15}{150\mu} = 100\Omega$$

After the resistor $R_1$, the resistor $R_3$ is the next.

This resistor is actually calibrated to limit the maximum current that flows into the diode, in order not to break the system in the case of faulty conditions. The maximum current is actually the one that has just been set, so $20mA$.

$$R_3 = \frac{15}{20m} = 750\Omega$$

To have a slight margin in the current, the chosen value of the resistor will be of $680\Omega$ ($22mA$).

The last missing resistor $R_2$ is the one that actually modifies the gain of the whole circuit.

The principle behind this second part of the optoisolator is to have the same behaviour as the first part, since that the current $I_{P2}$ will flow through the resistor $R_2$, obtaining the voltage $V_C$. This voltage will then be sent to the output thanks to the voltage follower.

By modifying the the value of $R_2$, the value of $V_C$ (and so of $V_{OUT}$) can be chosen.

With the optoisolator the last block of the measurement circuit is completed, and the final sensing circuit is this

![Figure 3.24: Data sheet of the LM3914](image)
3.3.3 Vu meter

The last circuit that has still to be explained is the Vu meter.

The Vu meter is a component that incorporates inside of its package all the needed circuitry to drive a digital output given an analogue signal as input.

The chosen circuit to do so is the LM3914, a circuit that can drive up to 10 LEDs, lighting them up accordingly to the input voltage. To do so, internally this circuit has a resistive network that divides the voltage across the series 10 times, in order to have a different reference for each LED diode.

The maximum input voltage is 12.5V, so the resistor $R_2$ of the previous circuit has to be set accordingly to have this as maximum output value from the optocoupler.

![Data sheet of the LM3914](image1)

**Figure 3.25:** Data sheet of the LM3914

The two resistors in the circuit are the ones used to controls the led brightness and the level of the internal reference.

![Data sheet of the LM3914](image2)

**Figure 3.26:** Data sheet of the LM3914
3.3. Temperature measurement

The principle to select the resistor is quite easy: 1.25V is always present between the REF OUT and the REF ADJ, for whatever resistance value connected through them. It must be noticed that the led brightness is fixed by selecting the value of the led current, which is the current that flows through the resistor $R_1$ increased by a factor of 10.

Then, when a second resistor is added in series to the first one, since that the current is already set by the first resistor (which is $\frac{1.25}{R_1}$), the voltage on the reference is also set.

So, starting from the LED current, the value of the resistor $R_1$ can be selected.

$$R_1 = \frac{1.25 \times 10}{12.5m} = 1k\Omega$$

After this resistor, the other one is the last one.
Its value is instead chosen based on the formula

$$REFOUT = 1.25(1 + \frac{R_2}{R_1}) = 12.5V$$

So the value of the resistor $R_2$ is chosen to be 9kΩ.

This voltage has now to be set as the voltage across the resistor network inside the circuit. To do so, it’s enough to connect the pin REF OUT to $R_{HI}$, and $R_{LO}$ to the ground plane.

The final vu meter circuit is then

![Vu meter circuit](image)

**Figure 3.27: Vu meter circuit**
3.3.4 Layout

The final schematic, with each one of the blocks explained before connected together is reported below

![Schematics of the final board](image1)

The only block that hasn’t been explained is actually the block with a voltage regulator, that as the name suggests is actually a simple LM7805 with just its filtering capacitances.

Now that the whole schematics is ready, the layout of the circuit has been the next design step.

![Layout of the final board](image2)

Connecting all the components in the proper way while making some EMC considerations has been challenging.

The first challenge has been to have all the interfaces easily accessible to be used, may these be the jumpers or the cables to connect. Also a lot of probes have been put in the bord, in order to easily sense all the signals easily.
3.3. Temperature measurement

The second one has been to reduce the parasitic inductances of the circuit as much as it was possible -by increasing the width of the tracks-. This has been especially true with the power supply circuit of the gate driver, since that it is really susceptible to parasitic inductances, since that it charges only with current spikes. So it has been mandatory to connect that circuit as close as possible to the power transistor in order to reduce at minimum the tracks length. It has been mandatory as well to connect the differential amplifier as close as possible to the external gate resistance, in order to always reduce the parasitic inductances to the minimum.

The third one is actually another EMC consideration, that is to consider the huge current spikes that comes with the charging of gate capacitance, and to reduce the current loop of these to the minimum in order to avoid too much noise due to the switching activity.

The fourth consideration was related to the ground planes.

As is it possible so see from the figure above, in the circuit there are 3 different ground planes at 3 different references.

The longest one, that embraces the whole board, is the real ground plane, connected to ground. The other 2 are planes connected to the source of the 2 power mosfets.

A lot of effort has been done in order to cut it as little as it was possible, in order to have as few antennas as possible, since that every time that a current path that is flowing through the ground plane encounters a cut, in that point a small antenna is present. For the design of this circuit this parameter has been important.

Also the fact of dividing the signal and turn on/off currents that flows through the ground plane from the high currents due to the high loads that flow in the big track that is at the top of the circuit.

At the end the effort on the powerlines has been to try to have them as big as possible, in order to reduce the ohmic losses due to the supply currents in the circuit.
Chapter 4

Experimental results

4.1 Measurements

The last step of the project was the actual implementation of it on a real board. In the image below the realized prototype can be seen

![Prototype of the project](image)

**Figure 4.1:** Prototype of the project

After that the project has been built, the testing phase started by checking the 2 controls signals of the gate drivers, verifying that it could never happen that both of the gate signal would be up at the same time
Chapter 4. Experimental results

Figure 4.2: Test of the gate signals

The testing results were as expected, so that a short circuit condition could never happen because of the gate control signals.

After this verification, the next tests have been the frequency and the duty cycle variations in the control circuit, both of which worked as expected.

In the image below it is possible to see that both the duty cycle and the frequency of the converter have been changed respect to the previous case.

Figure 4.3: Test of the gate signals with modified frequency and duty cycle

After the gate control signals, the gate driver ones were the ones to test. Both of the circuit worked properly, but for a tidier view just one gate driver signal is represented here.
As it is clear from the image below, it works as expected.

![Figure 4.4: Test of the gate driver circuit](image)

Now that it is assured that everything works fine, the focus will be set on the current spikes measured through the external gate resistor. As it can be seen, they last a really short time respect to the total switching period.

![Figure 4.5: Current spikes measured across the external gate resistor](image)

A zoom will clarify the actual slope of the signals.
FIGURE 4.6: Zoom of the previous current spikes

From this picture, an unexpected thing is actually noticed: the rise time of the waveforms of the used power MOSFET is not of 100ns, but it is actually decreased by a factor 10, since that is is 10ns.

This means that the bandwidth calculated previously needs to be increased at least by 10 times, so it is now 35MHz.

The operational amplifiers chosen before had a GBW of 100MHz, which wouldn’t be enough even for an input signal of 3.5MHz of bandwidth, but taking into account a small distortion wouldn’t have been a trouble.

The point is that now the bandwidth is for sure not enough to sense correctly the input signal, but the circuit will still be tested.
As it can be easily seen the output voltage has decrease as the temperature increased, but not of the expected value.

The point is that not even the input signal has actually changed its shape from the beginning of testing.

To find the solution to this problem, the problem has been found in the actual formula of $V_{RG_{EXT}}$. 
Chapter 4. Experimental results

\[ V_{R_{EXT}} = V_{\text{DRIVER}} \frac{R_{G_{EXT}}}{R_{G_{EXT}} + R_{G_{INT}}} \]  \hspace{1cm} (4.1)

The initial hypothesis was that the only parameter that could vary in temperature was \( R_{G_{INT}} \).

The problem is that the zener diode, used to provide the constant reference to the power supply, is actually located near the power mosfet as well as all the other component of the power supply circuit.

The point is that its reference voltage varies a lot depending on the temperature, as the images below suggest.

**Figure 4.9:** Power supply voltage at 26°C

**Figure 4.10:** Power supply voltage at 80°C
As it is clear from the graphs above, the power supply voltage isn’t constant respect to the temperature, that’s why the output voltage doesn’t vary as expected -or at least with a similar behaviour-.

By removing the power supply circuit and supplying the circuit externally, the behaviour of the system is now as predicted, except for the gain that can’t be as high as needed, due to the low bandwidth of the op amp.

**Figure 4.11**: Blue: \( V_{RG_{EXT}} \), Azure: Output of the differential amplifier, Purple: Peak Detector Output at 26°C, externally supplied

**Figure 4.12**: Blue: \( V_{RG_{EXT}} \), Azure: Output of the differential amplifier, Purple: Peak Detector Output at 100°C, externally supplied
As it can be seen, the actual gain of the subtractor is not high enough at high frequencies to allow a large voltage swing of the peak detector.

To further prove the correct behaviour of the system, the device has been heated up fast from a temperature of already 50°C, up to 120°C in a fast way. Then in another graph it is shown a slow cool down of the device, always accordingly to the predicted behaviour.

**Figure 4.13:** Peak Detector Output vs time while heating the device from 50°C up to 120°C

**Figure 4.14:** Peak Detector Output vs time while cooling down the device from 120°C up to 26°C
After these tests, the circuit has been tested with abrupt load variation, to see how it reacts.

Theoretically these variations shouldn’t affect the measurement, but the results are actually different.

To check the behaviour of the system, the output of the peak detector is plotted.

![Figure 4.15: Peak Detector Output vs time while cooling down the device, step changes indicate a load variation](image)

From the graph above it is clear to see how the theoretical expectation doesn’t match with the reality.

At the beginning, the circuit works as expected, sensing the temperature of the device as it cools down.

The first positive step variation indicates that the input voltage has been connected to the circuit.

At this point, the circuit is already not working as it should, since that the value shouldn’t change respect to any changes in \( V_{DS} \).

The following small negative one is due to the first connection of a light load (0.56 A).

This variation actually does not bothers too much the temperature measurement, since that the variation in the temperature read is just a few degrees.

The next one, the big one, is instead due to the insertion of a medium load connection (0.98 A). Then a third and a fourth loads (up to 1.68 A) are added, but almost no changes in the gate current can be seen. Then the loads are gradually removed and then the circuits returns to work properly.

The huge variation that the insertion of the load has provoked at the output of the converter at the end makes this system unsuitable for medium or high loads connections.

This behaviour could be due to the fact that when a high current passes through the transistor, it actually changes the distribution of the electric field in a difficult way to predict, so that the current distribution of the gate are changed as well.

Moreover, since that the bandwidth of the system is not suitable for this measurement, another solution for the temperature circuit has been explored.
### 4.2 Second circuit

Since that the previous approach to the problem seemed to have some problems, another one has been tried.

Instead on focusing on getting the perfect voltage waveform on the external gate resistor, to amplify and to shift it, and just at the end to store the value of the peak, the order of the components has been changed.

Since that the real problem was that all the operational amplifiers had to withstand a lot of fast voltage spikes, if the peak is set as first block of the circuit, then all the other block will work with a DC signal, since that the output will be actually a DC voltage.

The point is that there is no low cost, small, active component that could achieve such a high bandwidth to be put as first stage of the circuit.

The solution has been found by looking at figure 3.16. From that figure (the waveforms of a simple passive peak detector) it is clear that even thou a capacitor isn’t fully charged in a single turn-on instant, after some pulses it will actually be charged. The charge will never reach level higher than $V_{R_{INT}}$, since that the max voltage is clamped by the voltage divider provided by that resistance with $R_{GINT}$.

Using the very fast Schottky diodes used in the previous peak detector scheme, achieve this goal without active components look like a possible solution.

In this way sensing the voltage would be easy and low cost, since that any OP AMP will serve the purpose of being used in a differential configuration with a high input impedance.

The only thing of using a circuit like this is that at the output there will be some noise due to the switching activity.

This noise can be filtered out by adding a capacitor in the feedback loop of the amplifier, together with the resistances, in order to add a pole at a low frequency, to filter the input switching noise.

After this stage, another one is added just to adjust the gain and the proper offset.

This hasn’t been implemented directly on the subtractor because it is not convenient nor easy to change 2 resistor at the same time to modify the gain or the offset, in order to keep the subtractor balanced. With this other stage, since that it has to sense a single ended voltage, it is possible to easily invert the logic of the circuit and to have a higher peak when the temperature actually increases.

![Figure 4.16: New temperature circuit](image)

In the following graphs there will be represented the voltage across the capacitor in blue and at the output of the optoisolator in azure, varying with the temperature.
As it can be clearly seen, now the temperature variation provides a sensible output variation of 5V, much better than the previous one.

The point is that also this measurement is still affected by load variation, as it is clearly visible in the graph below.

![Graph 1](image1)

**Figure 4.17:** Blue: Capacitor Voltage, Azure: Optocoupler Output

It is clear how the load changes affect also this measurement in a way that makes the temperature measurement circuit useless if it isn’t performed with a fixed load.

But this is not a feasible solution, since that the converter will always be affected by load changes.

![Graph 2](image2)

**Figure 4.18:** Blue: Capacitor Voltage, Azure: Optocoupler Output
4.3 Conclusions

Both of the designed circuit versions presented some troubles when the converter was connected to heavy loads, maybe due to a different distribution of the gate charge.

The load changes actually implied really small changes to the input peak, but since that the gain was really high, even a small variation of an input parameter at the output would be seen as a huge one.

However, at the end the project specifications regarding the area of the circuit, the cost and the power consumption have been achieved, the missing point is the immunity to load variations.

Some points to work as a future project would be to actually change the used device and trying with bigger ones, since that maybe in those the temperature measurements won’t be influenced by load variations.
Appendix A

Economical review

A.1 Component cost

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**FIGURE A.1:** Cost of the first list of components
### A.2 Total cost of the Project

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#### First Component list
- [ ] First Component List

#### Second Component list
- [ ] Second Component List

**TOTAL**
- **€27,366.58**

**FIGURE A.2:** Cost of the second list of components

**FIGURE A.3:** Cost of the board
Appendix B

Environmental Impact

Nowadays the environmental impact is an important aspect of a project that is seen just as a background aspect by the common PCBs designer, since that if a project works, then the objective is achieved.

By wasting a lot of energy the pollution is increased day by day, even thou some important steps have been taken in those field where a limit could be applied by law. Nowadays for example there is a law called RoHs that limit the use of lead, a really toxic substance, as enrichment of the electronic components.

However this project can actually give a minimal environmental benefit to minimize the energy waste.

The final objective of this project is to use it as a temperature sensor for the power switches used in the MAC converter.

If this circuit is taken into account in the control scheme, then there will be no more a single device that will be heated up much more than the others, but the controls will be designed in order to guarantee a better power distribution between all the devices.

This will imply an energy saving from the point of view of the cooling system, since that all the temperature peaks will be lowered down.

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