June 7th, 2017

Instruction sets want to be free

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Abstract

The most important interface in a computer system is the instruction set architecture (ISA) as it connects software to hardware. So, given the prevalence of open standards for almost all other important interfaces, why is the ISA still proprietary? We argue that a free ISA is a necessary precursor to future hardware innovation, and there is no good technical reason not to have free, open ISAs just as we have free, open networking standards and free, open operating systems.

The free and open RISC-V ISA began development at UC Berkeley in 2010, with the frozen base user ISA standard released in May 2014, and has since then seen rapid uptake around the globe, including the first commercial shipments. This talk will cover the technical features of the RISC-V ISA design, which has the goals of scaling from the tiniest implementations for IoT up to the largest warehouse-scale computers, with support for extensive customization. We will also describe industry-competitive open-source cores developed at UC Berkeley, all written in Chisel, a productive new open-source hardware design language. Finally, we will describe the uptake of RISC-V and the development of the RISC-V ecosystem, including the RISC-V Foundation.

Short Bio

Krste Asanović is a Professor in the EECS Department at the University of California, Berkeley. He received a PhD in Computer Science from UC Berkeley in 1998 then joined the faculty at MIT, receiving tenure in 2005. He returned to join the faculty at Berkeley in 2007, where he co-founded the Berkeley Parallel Computing Laboratory ("Par Lab").

His main research areas are computer architecture, VLSI design, parallel programming and operating system design. He is currently Director of the Berkeley ASPIRE lab tackling the challenge of improving computational efficiency now that transistor scaling is ending. He leads the free RISC-V ISA project, is Chairman of the RISC-V Foundation, and has recently co-founded SiFive Inc. to support commercial use of RISC-V processors. He is also an Associate Director at the Berkeley Wireless Research Center, and holds a joint appointment with the Lawrence Berkeley National Laboratory. He received the NSF CAREER award, and he is an ACM Distinguished Scientist and an IEEE Fellow.