FPGA Implementation of an LMS-based Real-Time Adaptive Predistorter for Power Amplifiers

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***Abstract* - This paper presents an adaptive Digital Predistorter (DPD) for Power Amplifier (PA) linearization whose implementation and real time adaptation have been fully performed in a Field Programmable Gate Array (FPGA) device responsible for the co-processing tasks. The predistortion function is carried out in a Basic Predistortion Cell (BPC) containing a Look-up Table (LUT). One of the main advantages of this DPD configuration is that adaptation is performed in a hot manner and therefore, it is not necessary to switch the DPD into a training mode in order to estimate the LUT contents. Results showing the linearization capabilities of this adaptive DPD are here provided.**

I. INTRODUCTION

The spectrally efficient modulation formats are very sensitive to the Intermodulation Distortion (IMD) that mainly results from nonlinearities intrinsic of the PA. Hence, significant back-off (BO) levels of operation are required to achieve linearity, thus penalizing power efficiency in the PA. The wider bandwidths, often scalable, and the adaptive modulation process imposed in modern communications standards increased PAPR (peak to average power ratio) figures so then aggravating the linearity *vs.* efficiency problem. A recognized solution to avoid the power inefficient operation without enlarging the spectral regrowth is the use of PA linearizers, being Digital Predistortion (DPD) of the most important linearization techniques due to the current availability of faster Digital Signal Processing (DSP) hardware.

Due to aspects such as aging, heating or load impedance variations, the PA is a long-term time-variant nonlinear system, Therefore, the PA behavior needs to be periodically monitored in order to eventually adapt the Digital Predistorter (DPD) to counteract possible changes in its behavior or in its mode of operation.

Therefore, the PA behavior needs to be periodically monitored in order to eventually adapt the Digital Predistorter (DPD) to counteract possible changes in its behavior or in its mode of operation. Unlike in [1], there is no need to stop the transmission and switch into a training mode, because the DPD adaptation can be enabled/disabled by the user in a hot manner. It is thus possible to simultaneously transmit and adapt the DPD thanks to the real-time parallel processing performed by the Field Programmable Gate Array (FPGA) device. This architecture improves the DPD configuration in [2], where the predistortion function was already implemented in a FPGA device by means of a set of Basic Predistortion Cells (BPCs), but the update of the contents of these BPCs (complex gains stored in look-up tables) was performed in a host PC. Following the same principles explained in [3], the adaptation of the DPD is carried out using the Least Mean Square (LMS) algorithm to update all single complex gains that fill a BPC.

This paper is an extended version of a work presented in the Topical Symposium on Power Amplifiers for Wireless Communications (San Diego, 2009).

II. ARCHITECTURE OF THE ADAPTIVE REAL-TIME DIGITAL PREDISTORTER

A block scheme of the adaptive LMS-based DPD is depicted in Fig. 1. First of all and in order to ensure a good functioning of the DPD+PA system it is necessary pre-equalize the return path (from the PA output at RF to baseband), that is, to perform an amplitude and phase correction of the received baseband signal (*Rx_Data* in Fig.) with the PA acting as a linear device. One of the main critical issues regarding the design of adaptive DPDs is to ensure that the return path (from the PA output at RF to baseband) does not introduce additional nonlinearities, otherwise the DPD would be compensating for nonlinearities that don't belong to the PA and the overall linearity in the transmitter would be compromised. Additionally it also necessary to include an offset cancellation block and a time-alignment block, in order to remove I-Q offsets and to have the transmitted (*Tx_Data*), the predistorted (*Tx_DPD*) and the received (*Rx_Data*) signals aligned, synchronized.

The predistortion function is carried out as in [2] and [3] by means of BPCs. Here, for simplicity, we have just considered 1 BPC for testing the functioning of the real-time adaptation and thus the DPD is memoryless. However, the introduction of memory compensation capabilities to the existing DPD just relies on the addition of several replicas of the same BPC structure, considering delayed samples of the input and/or the output to address their corresponding LUTs (see [3]). In order to perform the real-time adaptation it is necessary to use Dual Port RAM (DPR) memory blocks. A DPR memory block has two independent sets of ports for simultaneous reading and writing. Independent address, data, and write enable ports allow shared access to a single memory space.

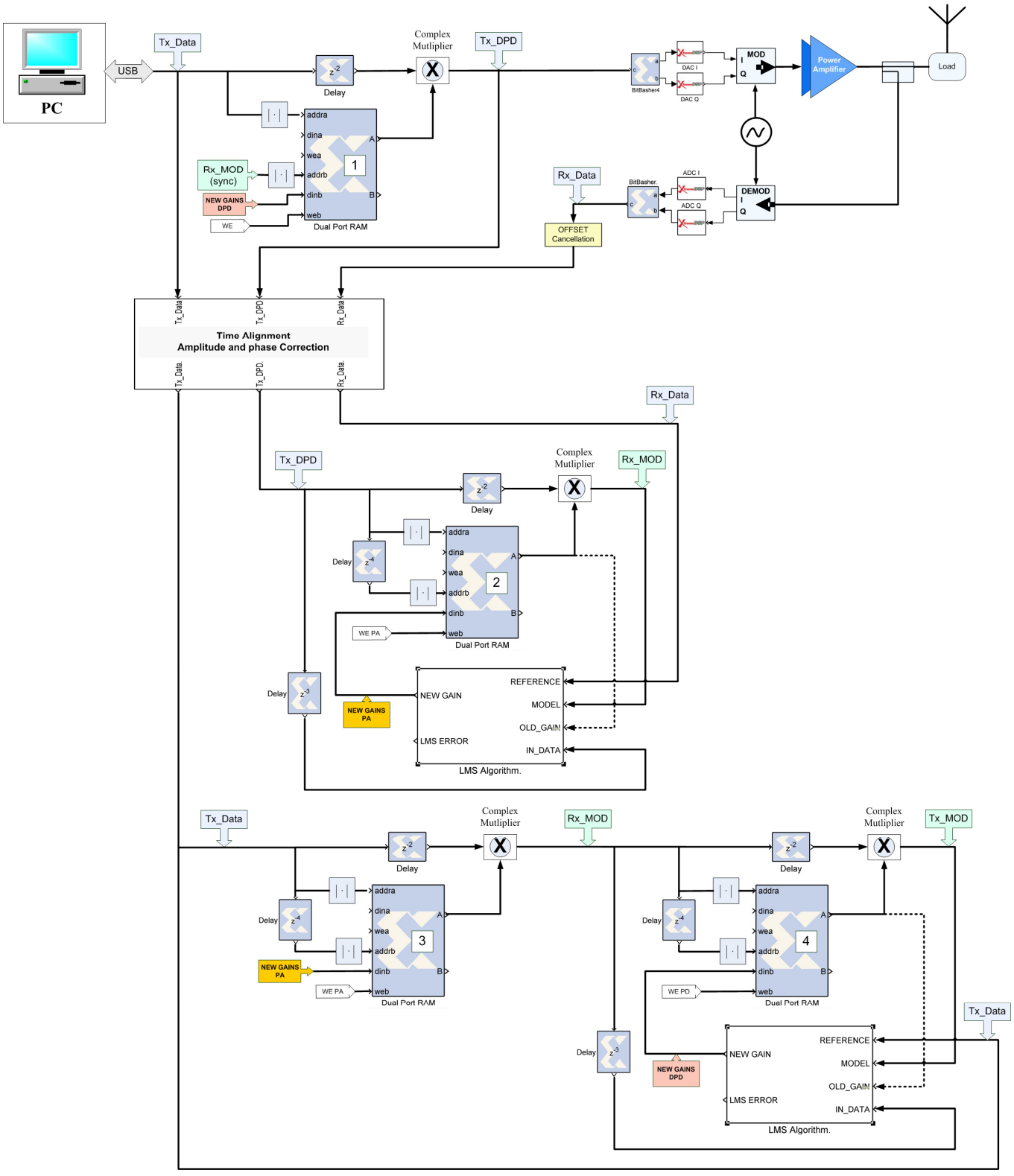

Fig. 1. Block scheme of the adaptive LMS-based digital Predistorter

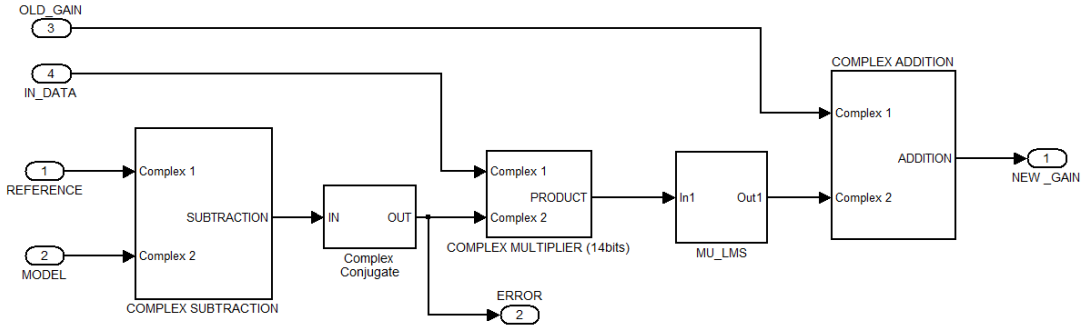

Fig. 2. Block scheme of LMS block

The whole adaptive predistorter subsystem is composed by the following blocks running in parallel: PA identification block (BPC#2+LMS and BPC#3), Postdistortion block (BPC#4) and Predistortion block (BPC#1). The PA identification block is composed by the BPC#2 + LMS block (see Fig. 1). In here, both *Tx_DPD* and *Rx_Data* signals are continuously monitored to extract the complex gains (NEW GAINS PA) defining the PA static behavioral model (AM-AM and AM-PM characteristics). These gains are used to fill BPC#3, which is excited with the input signal to be transmitted (*Tx_Data*) to obtain the estimated output signal of the PA, *Rx_MOD*.

The postdistortion block is composed by the BPC#4 + LMS block, and is responsible for inverting the PA characteristic. This block is exited with the estimated output of the PA (*Rx_MOD*) obtained before. The complex gains (*NEW GAINS DPD*) estimated in the BPC#4 + LMS block are continuously being copied in BPC#1 to perform predistortion.

Finally, the predistortion of the signal to be transmitted (*Tx_Data*) is performed in BPC#1, obtaining the predistorted data (*Tx_DPD*) to be upconverted and fed to the PA.

This closed loop system allows real-time adaptation of the DPD without interrupting the data transmission.

Using a generic notation ($x(k)$ being a generic input and $\hat{y}(k)$ being a generic estimated output), the input-output relation in a BPC is defined in eq. (2) while the LMS algorithm is defined in eq.(3).

$$\hat{y}(k) = x(k) \cdot G^{*}_{LUT}(|x(k)|) \qquad (2)$$

$$G^{(new)}_{LUT}(|x(k)|) = G^{(old)}_{LUT}(|x(k)|) + \mu \cdot x(k) \cdot e^{*}(k) \qquad (3)$$

Now, if we particularize the notation for the BPC#2, the variable *x(k)* is *Tx_DPD*, while $\hat{y}(k)$ is *Rx_MOD* and the LMS error is defined as: *e(k)= Rx_Data - Rx_MOD*. Analogously, particularizing for the BPC#4, the variable *x(k)* is *Rx_MOD*, while $\hat{y}(k)$ is *Tx_MOD* and the LMS error is defined as: *e(k)= Tx_Data - Tx_MOD*. The block scheme of implementation of the LMS algorithm in the FPGA is depicted in Fig. 2.

III. Results

Results were obtained considering a memoryless behavioral model for the RF subsystem (PA + converters). The complete adaptive DPD architecture was implemented in a Xilinx Virtex-IV FPGA device. The test signal used to obtain these results is a typical 16-QAM modulated signal, being experimented two different bandwidths in order to consider the PA designed to cope with new standards allowing scalable bandwidths.

Some preliminary results are depicted in Fig. 3, Fig. 4 and Fig. 5. Fig. 3 shows both linearized and unlinearized output power spectra. The out-of-band distortion that appears as spectral regrowth (that according to communications standards has to respect certain spectrum masks) is compensated by the memoryless DPD in both transmission bandwidths.

Fig. 4 shows again both linearized and unlinearized AM-AM characteristics. Note that the linearized AM-AM shows a linear characteristic but at the price of losing gain in comparison to the unlinearized one.

Finally Fig. 5 shows the demodulated 16-QAM constellation for both cases, when the DPD is active and when DPD is not functioning. The in-band distortion can be seen in the demodulated signal as a compression and phase rotation of its constellation points. The use of the memoryless DPD allows compensate for this phase rotation and compression.

IV. Conclusion

The presented DPD architecture is capable to perform real-time adaptation without interrupting the data transmission Preliminary results have shown that this architecture is capable to compensate for both in-band and out-of-band nonlinear distortion. Future work will be aimed at implementing the Nonlinear Auto-Regressive Moving Average (NARMA) based predistorter by adding parallel BPCs that will allow the DPD compensate also for the memory effects. In addition, to reduce power consumption, it will be also interesting to introduce a control mechanism to automatically enable/disable adaptation according to the DPD+PA linearity requirements.

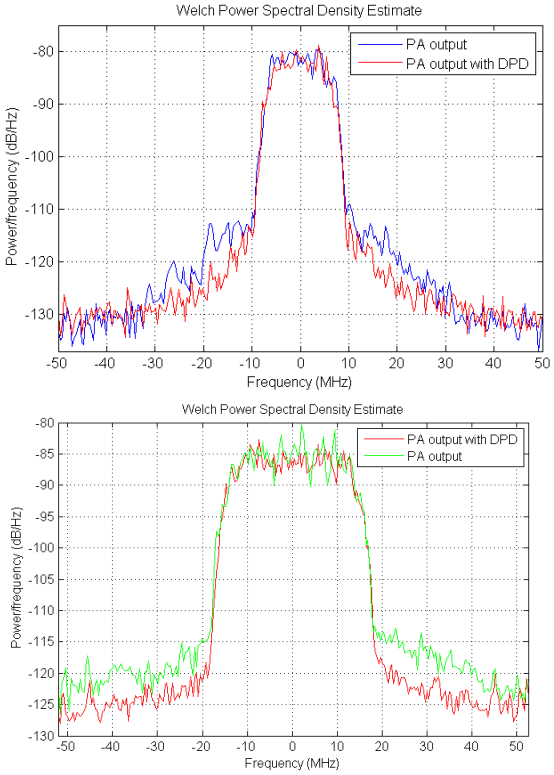

Fig. 3. Output power spectra (scalable bandwidths)

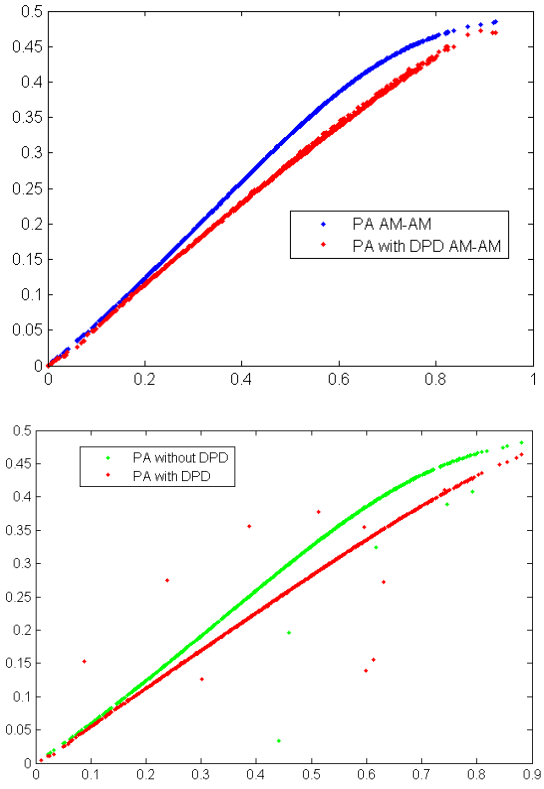

Fig. 4. AM-AM characteristic (scalable bandwidths of Fig. 3)

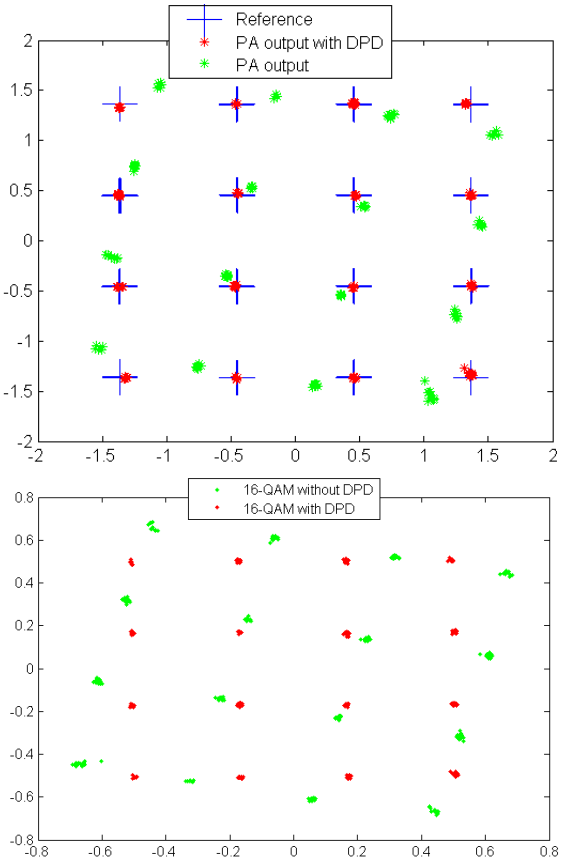

Fig. 5. 16-QAM constellation (scalable bandwidths of Fig.3)

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