3-Port Frequency-Selective Absorptive Limiter*

Alberto Hueltes, Eduard Rocas, *IEEE Senior Member,* Carlos Collado, *IEEE Senior Member*, Jordi Mateu, *IEEE Senior Member*, Nathan Orloff, James C. Booth, David Garcia-Pastor, Rafael Perea-Robles

***Abstract*— This paper describes a novel 3-port absorptive limiter for frequency selective circuits based on a configuration similar to a conventional 90º hybrid coupler. This circuit uses the switching behavior of common diodes to change between the non-limiting and absorptive limiting states. Theoretical descriptions and designs are presented along with prototypes based on PIN diodes. Measurements of the limiting performance of the devices at approximately 2 GHz as a function of power demonstrate the viability of the concept.**

***Index Terms*— Absorptive limiter, diode limiter, frequency selective limiter.**

I. Introduction

FREQUENCY-selective limiters are usually required to prevent large-amplitude incident signals from blocking the reception of smaller-amplitude signals at other frequencies. They are commonly used as part of broadband receivers in electronic warfare systems, where a very high-power jamming signal can significantly de-sensitize the receiver.

Typically, it is advantageous to have a fast transition from the non-limiting to the limiting state, in order to suppress the effects of short-duration, pulsed RF jamming signals. The time response is usually set by the device used as the limiting element, which is the diode element here. In this case, the diodes may be implemented in one or more stages, and they are inherently reflective, which means that high power signals are reflected in the limiting state [1]. This paper proposes a novel concept for an absorptive limiter that provides good return losses, both during the limiting state and during the all-pass state. This concept is used to design and implement a diode-based absorptive frequency-selective limiter.

Other frequency selective limiters have been proposed in the literature. The work in [2] describes band-stop filters consisting of series resonators loaded with diodes, which present high out-of-band impedance regardless of power level. Although effective, this solution has the disadvantage that the design of the filter is dependent on the specific diode used.

References [3] and [4] show an absorptive limiter realized by loading a 90º hybrid coupler with identical PIN diodes, which were used as power dependent impedances whose magnitude decreases down to 50 Ω as the input power increases, resulting in a power-dependent reflection coefficient. In that case, the large signal power must be dissipated within the limiting device (PIN diodes + biasing circuit). The configuration presented in the current work is similar to that proposed in [5]; the main difference is that in the later work open stubs are cascaded with the diodes in order to change the phase of the reflection coefficient between states. The signal, whose phase is power dependent, is then either added in-phase or cancelled at the protected receiver port.

The design introduced here has some similarities with the work in [5] in the way it takes advantage of the phase dependence as a function of power and also the ability to redirect the large jamming signal to a different port/load where it can be dissipated. Despite the similarities, this new design represents a significant improvement, offering similar performance in a simpler and more compact circuit. This new concept has been validated with the design, fabrication, and power-dependent characterization of a prototype based on PIN diodes.

II. Proposed Architecture

A. General Concept

The concept of this new limiter is based on cancellation of signals of opposite phases, where the phases of the signals are governed by the signal power itself. Figure 1(a) shows the circuit implementing this approach, where the input signal is driven through Port 1, the low-power output signal is on Port 2, and Port 3 is the output for the high-power signal to be dissipated. As depicted in Fig.1(a), the input signal (Port 1) is initially divided into two paths. One path reaches Port 2 after a $\lambda/4$ transmission line section, i.e., with a 90 degree phase shift. Port 2 is connected to Port 3 through another $\lambda/4$ section, providing a power-independent 90 degree phase shift between Port 1 and Port 2, and 180 degree phase shift between Port 1 and Port 3, along this path.

The second path for the incident signal travels through a limiting section, realized by a PIN diode, followed by a $\lambda/4$ transmission line section, which connects to a second limiting section, also realized by a PIN diode. Finally, the signal is delivered to Port 3 by means of a $\lambda/4$ transmission line section. In the low power case, this path behaves as an open-circuit (diodes OFF) and the input power flows to Port 2 (all-pass state) as shown in Fig 1(b).

When the input power exceeds a given threshold, enough to

Automatically generated dates of receipt and acceptance will be placed here; This work was partially supported by the Generalitat de Catalunya under Grant 2014 SGR 1551, by the Cluster of Application and Technology Research in Europe on Nanoelectronics under the CORTIF CA116-Coexistence of Radio Frequency Transmission in the Future.

A. Hueltes, E. Rocas, C. Collado, J. Mateu, D. Garcia-Pastor, R. Perea-Robles are with the Signal Theory and Communication Dept. from Universitat Politecnica de Catalunya, Castelldefels, Barcelona, Spain. N. Orloff, J.C. Booth, are with the CTL at the NIST, Boulder, CO 80305 USA.

*Work partially supported by US Government, not subject to US copyright.

switch both diodes to the ON state, this path adds a phase shift of 180 degrees to the signal before it reaches Port 3 and an additional 90 degrees, for a total of 270 (or -90) degrees, before it reaches Port 2. This means that when the two signals are combined, at both ports 2 and 3, and due to their phase difference, they are cancelled at the receiver port to be protected (limiting state), with the resulting power flowing to Port 3. In this design, the limiting state occurs when both diodes are ON, while the all-pass state occurs when the diodes are OFF.

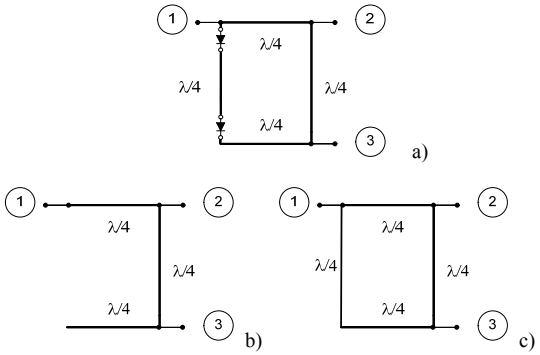

Fig. 1.a) General concept of the proposed absorptive limiter; b) non-limiting state; c) limiting state.

B. *Non-limiting State Analysis*

In the non-limiting case, representing a low power signal, the diodes are in OFF state and the equivalent circuit is depicted in Fig. 1(b). From this, it is straightforward to conclude that, at the operating frequency, Port 3 it is loaded by a λ/4 open stub, resulting in short circuit at Port 3, which in turn results in an open circuit at Port 2, yielding a through-line response between Port 1 (input) and Port 2 (output).

C. *Limiting State Analysis.*

In the limiting case, representing high power signals, the diodes are in ON state and ideally behave as a short circuit, resulting in the equivalent circuit of Fig. 1(c). This circuit can now be analyzed as a conventional branch-line coupler, by use of an even- and odd-mode analysis approach. To accomplish this, an additional port, Port 4, has been included to obtain a plane of symmetry as shown in Fig. 2(a). This port should be considered as an open circuit for the current analysis. Note as well that all transmission lines forming the circuits have equal characteristic impedance, normalized to one for this analysis. The even and odd mode circuits are then formulated as in Fig. 2(b).

In the even- and odd-mode analysis, the normalized amplitude of the incident waves are set to $\pm 1/2$ and the amplitudes of the emerging waves, b_i, at each port of the branch-line hybrid can be expressed as:

$$b_1 = \frac{1}{2}\Gamma_e + \frac{1}{2}\Gamma_o \qquad b_2 = \frac{1}{2}T_e + \frac{1}{2}T_o \quad , \tag{1}$$

$$b_3 = \frac{1}{2}T_e - \frac{1}{2}T_o \qquad b_4 = \frac{1}{2}\Gamma_e - \frac{1}{2}\Gamma_o \quad .$$

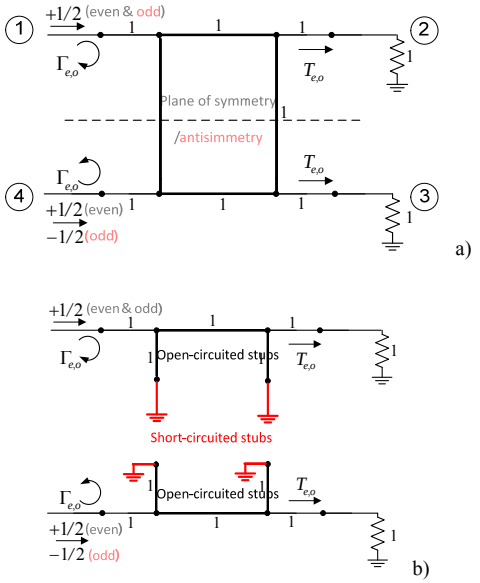

Fig. 2.a) Even & odd-mode analysis. Plane of symmetry (even-mode) and anti-symmetry (odd-mode). b) Open-circuited stubs correspond to an even-mode analysis and red short-circuited stubs correspond to an odd-mode analysis.

The terms, Γ_e, T_e and Γ_o, T_o are calculated by means of conventional microwave circuit analysis of the corresponding circuits for the even and odd modes, respectively. The resulting scattering parameters are:

$$[S] = \frac{1}{5}\begin{bmatrix} 1 & -2j & -4 & -2j \\ -2j & 1 & -2j & -4 \\ -4 & -2j & 1 & -2j \\ -2j & -4 & -2j & 1 \end{bmatrix} \quad . \tag{2}$$

Applying the condition that Port 4 is in open circuit (absence of Port 4), this corresponds to a_4=b_4 in (2) and we obtain:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = [S]\begin{bmatrix} a_1 \\ a_2 \\ a_3 \\ -\frac{j}{2}a_1 - a_2 - \frac{j}{2}a_3 \end{bmatrix} \quad . \tag{4}$$

Now the system has only three linearly independent equations and the previous [S] matrix can be reduced to an equivalent 3-port network with

$$[S] = \begin{bmatrix} 0 & 0 & -1 \\ 0 & 1 & 0 \\ -1 & 0 & 0 \end{bmatrix} \quad . \tag{5}$$

This result leads to the conclusion that Port 1 is matched, with the signal transmitted to Port 3, and no signal is transmitted to Port 2 (which is the protected port of the receiver).

III. Prototype and Measurements

Figure 3 shows the prototype that was fabricated and

measured. It was designed with a RO3010 substrate of 0.635 mm thickness, with 35 μm thick copper conductors, for operation at 2.24 GHz, with 50 Ω input and output ports. This results in transmission lines of 0.51 mm width and 12.28 mm length, which corresponds to λ/4 at the operating frequency.

Simulations were performed to obtain the [S] parameters along with the output power (P_{out}) and input power (P_{in}) dependence. The design uses PIN diodes [6] having a junction capacitance (C_j) value of 0.12 pF, which was included in the simulations. Note that the effect of C_j needs to be considered for the non-limiting state when the diodes are non-conducting. In the limiting state, the diodes conduct and are assumed to behave as perfect through lines.

From the layout point of view, the inclusion of the diodes into the design reduces the space to fit the quarter wavelength transmission line between the diodes. As depicted in Fig.3, this is solved by bending the transmission line. Although the design considers the effects of the bends, we observe that they have a small effect on the calculated [S] parameters.

Although large-signal circuit models of the specific diodes used in the design were not available, we used large signal models of other PIN diodes with similar properties in order to simulate the transition between states using harmonic balance analysis. Figure 4 shows the details of a full characterization of the device performance as a function of the input power, displaying both measured and simulated results. The characterization consists of measuring the output power at each output port, while the other is terminated with a matched load (see the legend in Fig.4), as a function of the input power at Port 1. Measurements and simulations of the reflected power at Port 1, when Ports 2 and 3 are matched, are also included. Note that measured and simulated results are in qualitative agreement; discrepancies are likely due to inaccuracies in the large-signal models of the diodes.

Figure 5 presents both simulated and measured [S]-parameters for an input power of P_{in}=-7 dBm, also showing good agreement. The device shows low insertion loss for both states (limiting and all-pass states), a threshold power around 6 dBm, and isolation of 12 dB at the highest measured input power (30 dBm).

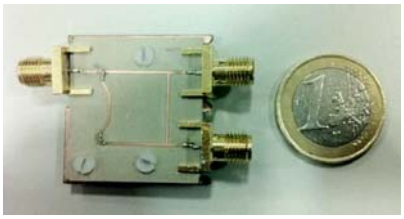

Fig. 3. Photograph of the prototype 3-port limiter.

IV. Conclusion

This work has demonstrated the concept of a compact, absorptive, frequency selective limiter. A prototype using PIN diodes has been designed, implemented, and measured. Measurements demonstrate good agreement with the expected results. Although no time response measurements have been performed, the switching speed would be set by the switching time of the diodes themselves, which is expected for any limiting device implemented with the same limiting elements.

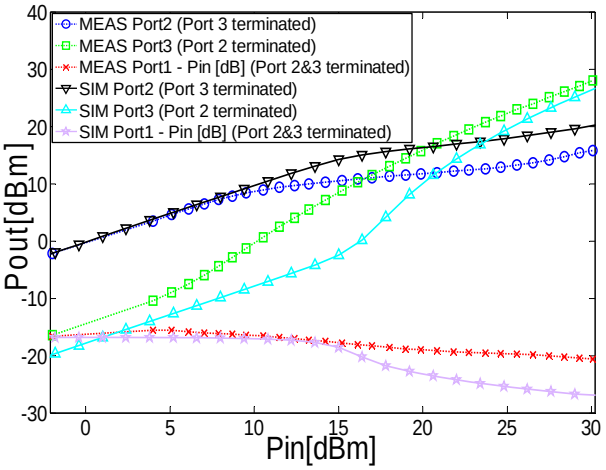

Fig. 4. Measurements and simulations of P_{out} (dBm) vs P_{in} (dBm) of a prototype for both Port 2 and Port 3. This figure also plots P_{out}-P_{in} (dB) at Port 1 vs P_{in} (dBm).

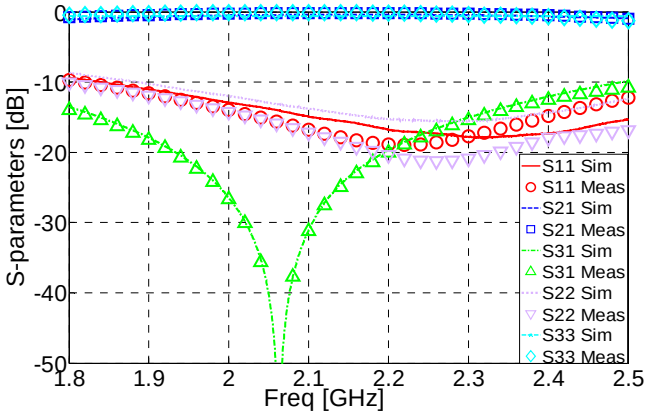

Fig. 5. [S]-Parameters in the all-pass state (P_{in} = -7 dBm). Simulations (continuous/dashed lines and no markers) and measurements (markers).

References

[1] N.J. Brown, "Design Concepts for High-Power PIN Diode Limiting", IEEE Trans. on Microwave Theory and Techniques, Volume 15, Issue 12, Dec 1967, Page(s):732 - 742

[2] P. Phudpong and I.C. Hunter," Frequency-Selective Limiters Using Nonlinear Bandstop Filters", IEEE Trans. on Microwave Theory and Techniques, Volume 57, Issue 1, Jan 2009, Page(s):157 - 164

[3] M.J. Rodriguez, D.A Weissman, "Microwave Power Limiter", IEEE Trans. on Microwave Theory and Techniques, Volume 10, Issue 3, May 1962, Page(s) 219 – 220.

[4] D. Lopez, J.-F. Villemazet, D. Geffroy, J.-L. Cazaux, G. Mouchon, J. Maynard, M. Perrel, M. Amarouali, "Ka Band Power Limiter For Satellite Channel Amplifier", Microwave and Optoelectronics Conference (IMOC), 2009 SBMO/IEEE MTT-S International, Page(s) 200 – 203.

[5] C. Collado, A. Hueltes, E. Rocas, J. Mateu, J.C. Booth, J.M. O'Callaghan, J. Verdú, "Absorptive Limiter for Frequency-Selective Circuits", IEEE Microwave and Wireless Components Letters, Volume 24, Issue 6, June 2014, Page(s) 415 – 417.

[6] The diodes used in this design are MICROSEMI GC4732-150A. The use of specific equipment, instruments, or materials identified in this paper does not imply recommendation or endorsement by the National Institute of Standards and Technology, but are provided to adequately describe the experimental procedures.