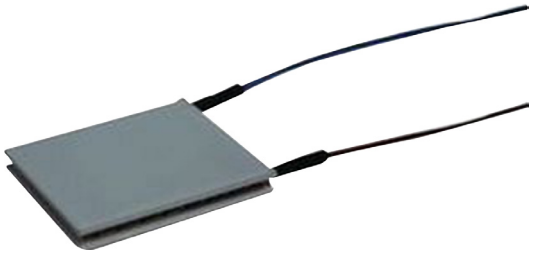
ANNEX 2

En aquest annex hi trobem els datasheets dels components següents en aquest ordre:

1. Cel·la Peltier
2. Sensor de temperatura NTC
3. Integrat LTC3108 pel circuit condicionador
4. Transformador pel circuit condicionador
5. Microcontrolador MSP430G2553
6. Led IR: TSAL6100
7. Receptor IR
8. Relé
9. Arduino Nano.

Peltier Cooler



Scope:

- This specification is applied to Multicomp thermoelectric modules
- Revision of these specifications is carried out after consent

Specification:

1. Parameters

Parameters			Remarks
Internal resistance	1.59Ω ± 10%		Note-1
Imax.	8.5A		Note-2
Vmax.	15.7V		Note-3
	Th=25°C		
Qmax.	79W		Note-4
ΔTmax.	70°C		Note-5
Solder melting point	232°C		Note-6
Max. Compress	1MPa		Note-7

Note-1 Measured by AC 4-terminal method at 25°C.

Note-2 Maximum current at ΔTmax.

Note-3 Maximum voltage at ΔTmax.

Note-4 Maximum cooling capacity at Imax.,Vmax. and ΔT = 0°C.

Note-5 Maximum temperature difference at Imax.,Vmax. and Q = 0W.
(Maximum parameters are measured in a vacuum 1.3P)

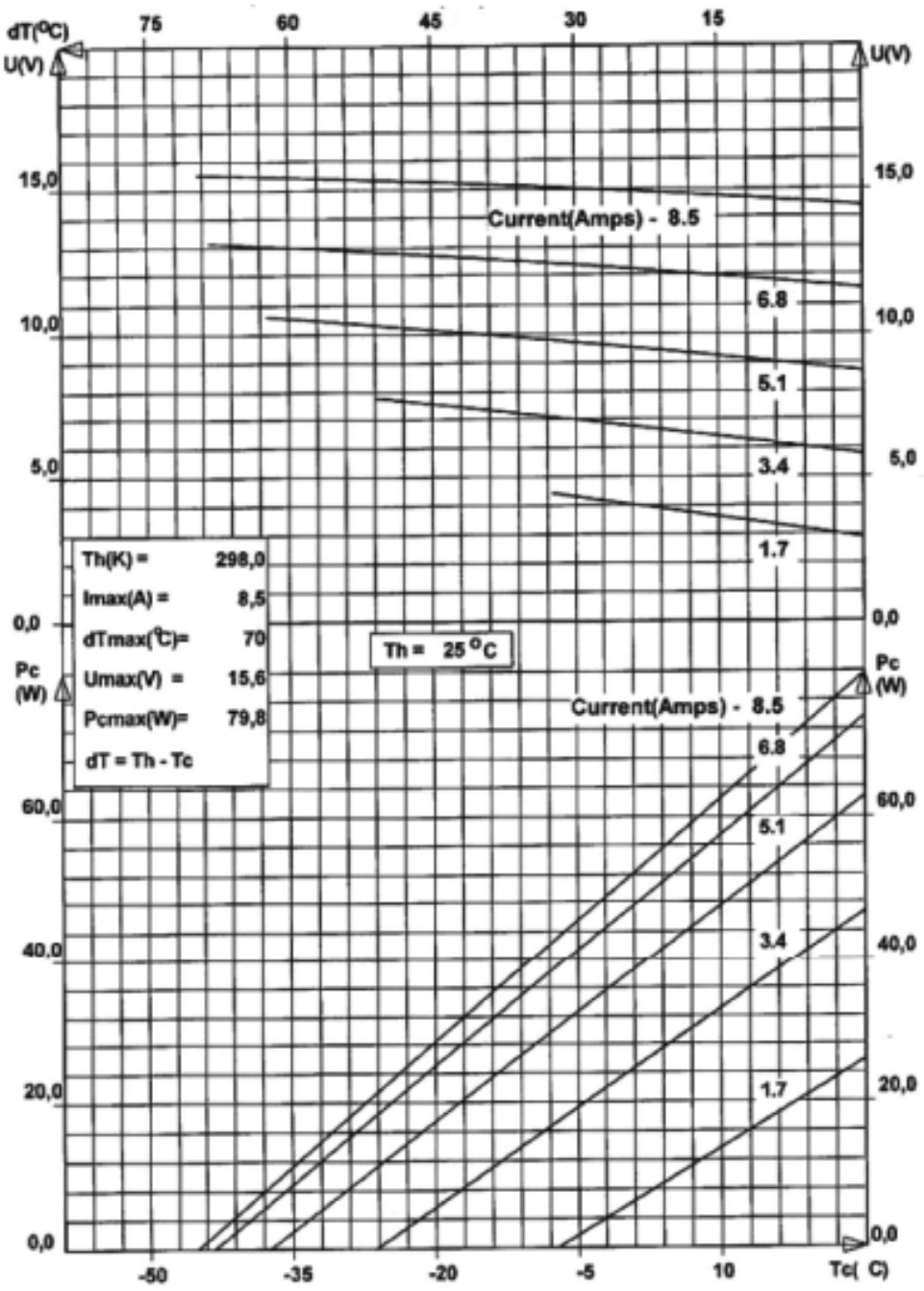
Note-6 The solder melting point of thermoelectric module.

Note-7 Recommended maximum compression (not destruction limit).

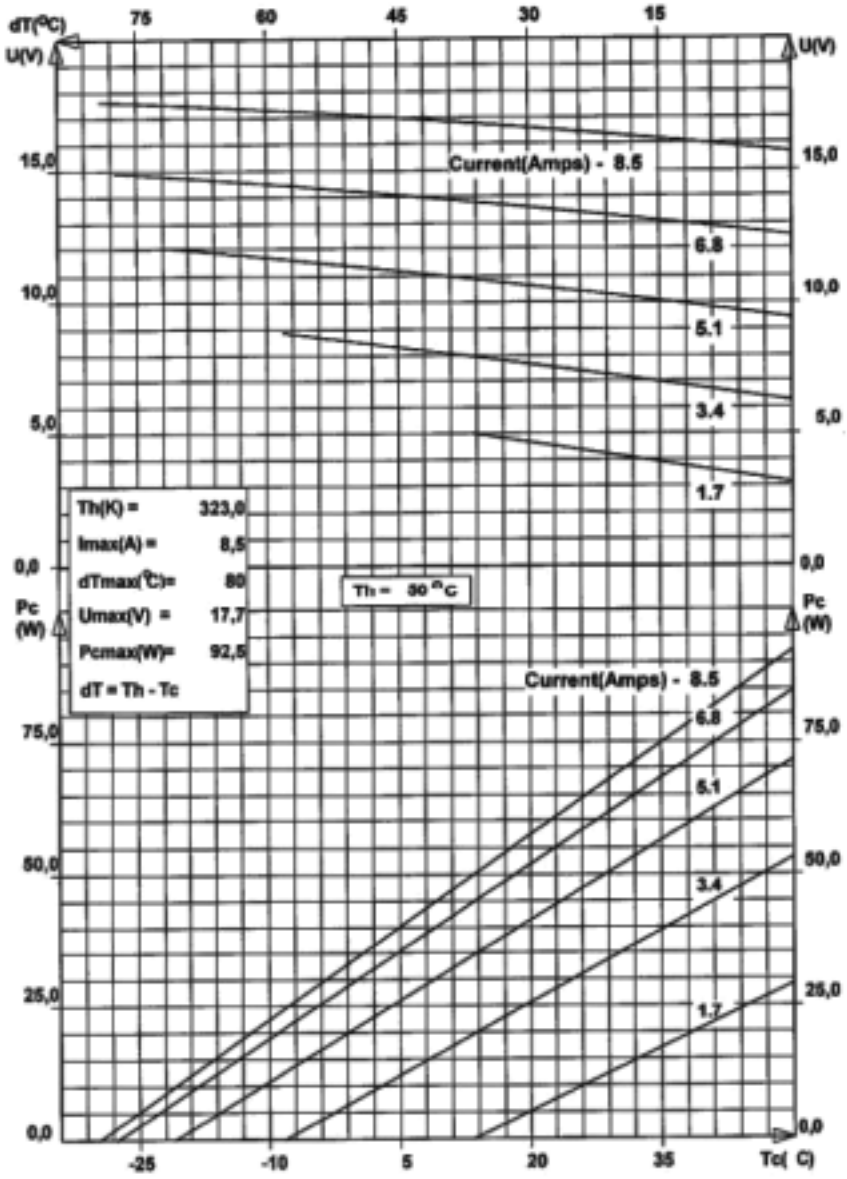
2. Recommendations

- Maximum temperature for short time: 200 °C
- Operation temperature up to 150°C for long lifetime;
- Long lifetime in power cycling mode with polarity change
- Recommended operation current not higher than 0.7 of Imax
- Preferable application; thermal management / cycling at high temperatures

3. Performance Graph



Peltier Cooler



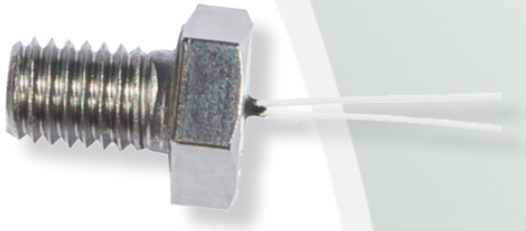
Part Number Table

Description	Part Number
Peltier Cooler, 79W	MCPF-127-14-11-E

Temperature sensor

Hex Bolt Sensor ETP-SP-

- Temperature range -40 to +125°C
- Miniature design with M8 hexagonal bolt
- Resistance values from 2.2 - 100 kΩ
- Custom designs available
- Higher temperature range available
- Versatile temperature probe with screw body



Applications

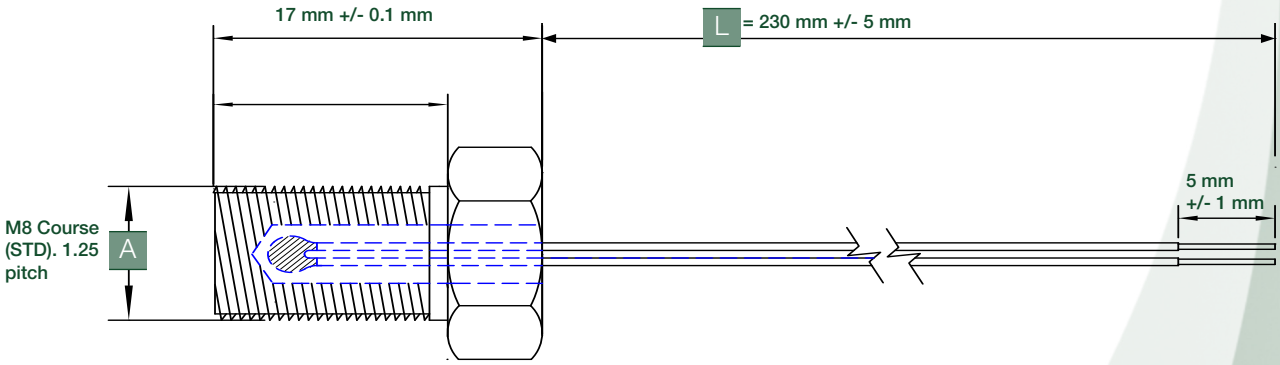
- Heating / cooling systems
- Automaotive
- Laboratory
- Industrial process
- Energy
- HVAC
- Drilling

Ordering information for standard stock model:

Stock model number: ETP - SP - 8 - 23 - 10K3A1B

A L T

- Thermistor type
- Probe cable length
- Probe thread size



Technical parameters for stock model

	Unit	Value
Nominal resistance at +25°C	Ohms	10,000
Resistance tolerance from 0..70°C	°C	+/- 0.2
Beta value 25/85	K	3976
Tolerance on Beta value 25/85	%	+/- 0.5
Dissipation constant in still air	mW/°C	2
Operating temperature	°C	-40 to +125
Epoxy thermal conductivity	W/(m.K)	1.7

Materials

Leads and insulation	28AWG Solid silver plated copper leads with white Kynar insulation
Probe material	Stainless steel

Features

- **Cost effective - off the shelf model**
- Solid tin plated lead wires
- Stock model - reduced lead times
- Improved potting epoxy has outstanding thermal conductivity for faster response times

Ordering information for custom designs:

Use the information below to build up a custom probe design.

A	Probe thread size					
	Order Code A =	5	6	7	8	x
	Thread size in mm	M5	M6	M7	M8	Optional thread size

L	Probe cable length										
	Order Code L =	5	10	15	20	23	25	30	35	40	45	x
	Length in mm +/- 5 mm	50	100	150	200	230	250	300	350	400	450	Custom length

T	Thermistor type	
	Order Code T =	All thermistor types available: Insert details as required

VARIOHM
EUROSENSOR

Resistance v. temperature table for 10K3A1B Thermistor

Temp. °C	Ohms
-40	336,052
-39	314,512
-38	294,487
-37	275,863
-36	258,533
-35	242,399
-34	227,373
-33	213,371
-32	200,318
-31	188,144
-30	176,786
-29	166,183
-28	156,280
-27	147,029
-26	138,382
-25	130,296
-24	122,732
-23	115,653
-22	109,025
-21	102,817
-20	97,000
-19	91,547
-18	86,433
-17	81,636
-16	77,134
-15	72,907
-14	68,937
-13	65,206
-12	61,700
-11	58,403
-10	55,301
-9	52,383
-8	49,636
-7	47,049
-6	44,612
-5	42,315
-4	40,150
-3	38,109
-2	36,183
-1	34,366
0	32650
1	31,030
2	29,500

Temp. °C	Ohms
3	28,054
4	26,687
5	25,395
6	24,172
7	23,016
8	21,921
9	20,884
10	19,903
11	18,973
12	18,092
13	17,257
14	16,465
15	15,714
16	15,001
17	14,324
18	13,682
19	13,073
20	12,493
21	11,943
22	11,420
23	10,923
24	10,450
25	10,000
26	9,572.0
27	9,164.7
28	8,777.0
29	8,407.8
30	8,056.1
31	7,721.0
32	7,401.7
33	7,097.3
34	6,807.1
35	6,530.3
36	6,266.3
37	6,014.3
38	5,773.8
39	5,544.3
40	5,325.0
41	5,115.7
42	4,915.6
43	4,724.5
44	4,541.7
45	4,367.1

Temp. °C	Ohms
46	4,200.0
47	4,040.2
48	3,887.4
49	3,741.1
50	3,601.1
51	3,467.1
52	3,338.7
53	3,215.8
54	3,098.0
55	2,985.2
56	2,877.0
57	2,773.3
58	2,673.9
59	2,578.6
60	2,487.1
61	2,399.4
62	2,315.2
63	2,234.4
64	2,156.8
65	2,082.3
66	2,010.8
67	1,942.1
68	1,876.0
69	1,812.6
70	1751.6
71	1,693.0
72	1,636.6
73	1,582.4
74	1,530.2
75	1,480.1
76	1,431.8
77	1,385.3
78	1,340.6
79	1,297.5
80	1,256.1
81	1,216.1
82	1,177.7
83	1,140.6
84	1,104.9
85	1,070.4
86	1,037.3
87	1,005.3
88	974.4

Temp. °C	Ohms
89	944.7
90	916.0
91	888.3
92	861.5
93	835.7
94	810.8
95	786.8
96	763.6
97	741.2
98	719.5
99	698.6
100	678.4
101	658.9
102	640.0
103	621.8
104	604.1
105	587.1
106	570.6
107	554.6
108	539.2
109	524.3
110	509.8
111	495.8
112	482.3
113	469.2
114	456.5
115	444.2
116	432.3
117	420.8
118	409.6
119	398.8
120	388.3
121	378.2
122	368.3
123	358.8
124	349.5
125	340.6

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ETP-SP - English - 08/12

LTC3108

Ultralow Voltage Step-Up Converter and Power Manager

FEATURES

- **Operates from Inputs of 20mV**
- **Complete Energy Harvesting Power Management System**
  - **Selectable V_{OUT} of 2.35V, 3.3V, 4.1V or 5V**
  - **LDO: 2.2V at 3mA**
  - **Logic Controlled Output**
  - **Reserve Energy Output**
- **Power Good Indicator**
- Uses Compact Step-Up Transformers
- Small 12-Lead (3mm × 4mm) DFN or 16-Lead SSOP Packages

APPLICATIONS

- Remote Sensors and Radio Power
- Surplus Heat Energy Harvesting
- HVAC Systems
- Industrial Wireless Sensing
- Automatic Metering
- Building Automation
- Predictive Maintenance

DESCRIPTION

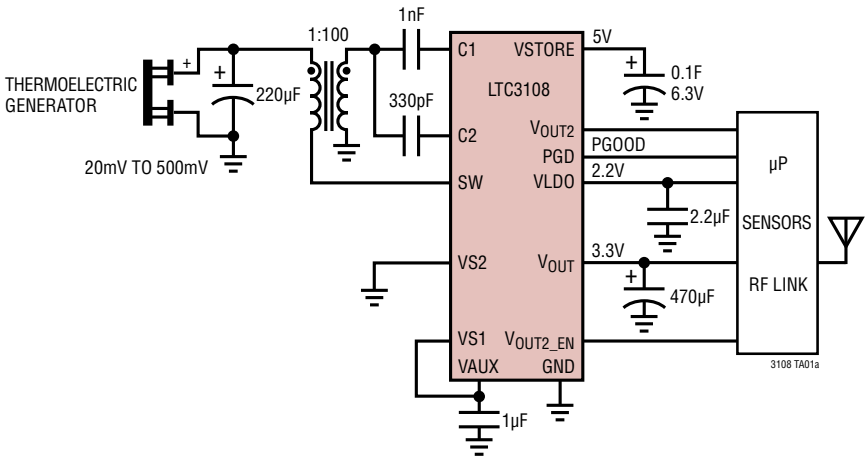
The LTC®3108 is a highly integrated DC/DC converter ideal for harvesting and managing surplus energy from extremely low input voltage sources such as TEGs (thermoelectric generators), thermopiles and small solar cells. The step-up topology operates from input voltages as low as 20mV. The LTC3108 is functionally equivalent to the LTC3108-1 except for its unique fixed V_{OUT} options.

Using a small step-up transformer, the LTC3108 provides a complete power management solution for wireless sensing and data acquisition. The 2.2V LDO powers an external microprocessor, while the main output is programmed to one of four fixed voltages to power a wireless transmitter or sensors. The power good indicator signals that the main output voltage is within regulation. A second output can be enabled by the host. A storage capacitor provides power when the input voltage source is unavailable. Extremely low quiescent current and high efficiency design ensure the fastest possible charge times of the output reservoir capacitor.

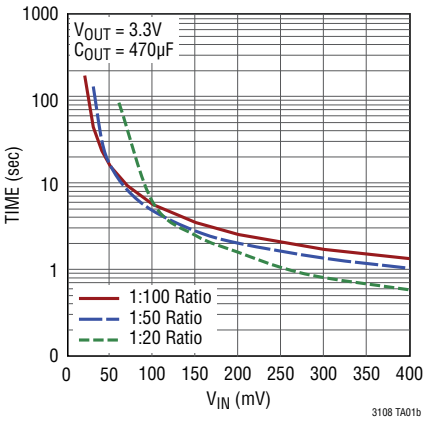
The LTC3108 is available in a small, thermally enhanced 12-lead (3mm × 4mm) DFN package and a 16-lead SSOP package.

TYPICAL APPLICATION

Wireless Remote Sensor Application Powered From a Peltier Cell



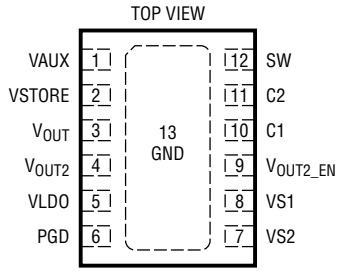
V_{OUT} Charge Time



ABSOLUTE MAXIMUM RATINGS (Note 1)

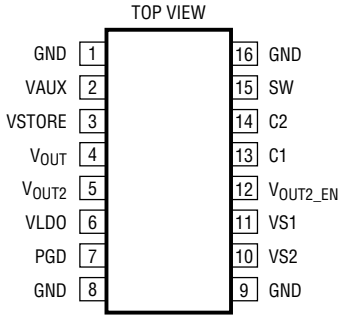
SW Voltage .....–0.3V to 2V
C1 Voltage.....–0.3V to 6V
C2 Voltage (Note 5).....–8V to 8V
V_{OUT2}, V_{OUT2_EN}.....–0.3V to 6V
VAUX.....15mA into VAUX
VS1, VS2, VAUX, V_{OUT}, PGD.....–0.3V to 6V
VLDO, VSTORE .....–0.3V to 6V
Operating Junction Temperature Range
(Note 2)..... –40°C to 125°C
Storage Temperature Range..... –65°C to 125°C

PIN CONFIGURATION



DE PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB (NOTE 4)



GN PACKAGE
16-LEAD PLASTIC SSOP NARROW

T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3108EDE#PBF	LTC3108EDE#TRPBF	3108	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3108IDE#PBF	LTC3108IDE#TRPBF	3108	12-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC3108EGN#PBF	LTC3108EGN#TRPBF	3108	16-Lead Plastic SSOP	–40°C to 125°C
LTC3108IGN#PBF	LTC3108IGN#TRPBF	3108	16-Lead Plastic SSOP	–40°C to 125°C

Consult LTC Marketing for parts specified for other fixed output voltages or wider operating temperature ranges.
*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are for T_A = 25°C (Note 2). VAUX = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Start-Up Voltage	Using 1:100 Transformer Turns Ratio, VAUX = 0V			20	50	mV
No-Load Input Current	Using 1:100 Transformer Turns Ratio; V_{IN} = 20mV, V_{OUT2_EN} = 0V; All Outputs Charged and in Regulation			3		mA
Input Voltage Range	Using 1:100 Transformer Turns Ratio	●	$V_{STARTUP}$		500	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are for T_A = 25°C (Note 2). VAUX = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	VS1 = VS2 = GND VS1 = VAUX, VS2 = GND VS1 = GND, VS2 = VAUX VS1 = VS2 = VAUX	● ● ● ●	2.30 3.234 4.018 4.90	2.350 3.300 4.100 5.000	2.40 3.366 4.182 5.10	V V V V
V_{OUT} Quiescent Current	V_{OUT} = 3.3V, V_{OUT2_EN} = 0V			0.2		µA
VAUX Quiescent Current	No Load, All Outputs Charged			6	9	µA
LDO Output Voltage	0.5mA Load	●	2.134	2.2	2.266	V
LDO Load Regulation	For 0mA to 2mA Load			0.5	1	%
LDO Line Regulation	For VAUX from 2.5V to 5V			0.05	0.2	%
LDO Dropout Voltage	I_{LDO} = 2mA	●		100	200	mV
LDO Current Limit	V_{LDO} = 0V	●	4	11		mA
V_{OUT} Current Limit	V_{OUT} = 0V	●	2.8	4.5	7	mA
VSTORE Current Limit	VSTORE = 0V	●	2.8	4.5	7	mA
VAUX Clamp Voltage	Current into VAUX = 5mA	●	5	5.25	5.55	V
VSTORE Leakage Current	VSTORE = 5V			0.1	0.3	µA
V_{OUT2} Leakage Current	V_{OUT2} = 0V, V_{OUT2_EN} = 0V			0.1		µA
VS1, VS2 Threshold Voltage		●	0.4	0.85	1.2	V
VS1, VS2 Input Current	VS1 = VS2 = 5V			0.01	0.1	µA
PGOOD Threshold (Rising)	Measured Relative to the V_{OUT} Voltage			–7.5		%
PGOOD Threshold (Falling)	Measured Relative to the V_{OUT} Voltage			–9		%
PGOOD V_{OL}	Sink Current = 100µA			0.15	0.3	V
PGOOD V_{OH}	Source Current = 0		2.1	2.2	2.3	V
PGOOD Pull-Up Resistance				1		MΩ
V_{OUT2_EN} Threshold Voltage	V_{OUT2_EN} Rising	●	0.4	1	1.3	V
V_{OUT2_EN} Pull-Down Resistance				5		MΩ
V_{OUT2} Turn-On Time				5		µs
V_{OUT2} Turn-Off Time	(Note 3)			0.15		µs
V_{OUT2} Current Limit	V_{OUT} = 3.3V	●	0.15	0.3	0.45	A
V_{OUT2} Current Limit Response Time	(Note 3)			350		ns
V_{OUT2} P-Channel MOSFET On-Resistance	V_{OUT} = 3.3V (Note 3)			1.3		Ω
N-Channel MOSFET On-Resistance	C2 = 5V (Note 3)			0.5		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3108 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3108E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3108I is guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated thermal package thermal resistance and other environmental factors. The junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$, where θ_{JA} is the package thermal impedance.

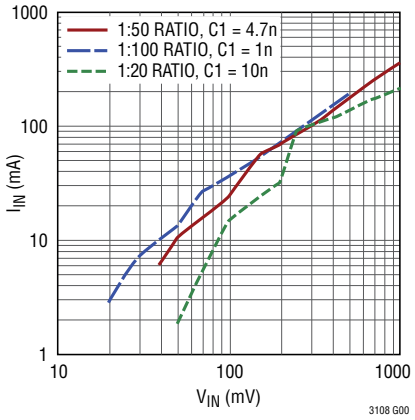
Note 3: Specification is guaranteed by design and not 100% tested in production.

Note 4: Failure to solder the exposed backside of the package to the PC board ground plane will result in a thermal resistance much higher than 43°C/W.

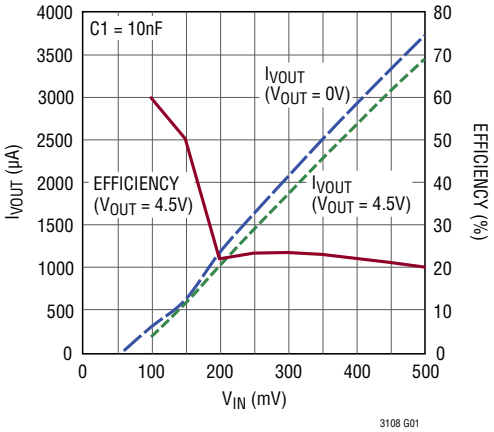
Note 5: The absolute maximum rating is a DC rating. Under certain conditions in the applications shown, the peak AC voltage on the C2 pin may exceed ±8V. This behavior is normal and acceptable because the current into the pin is limited by the impedance of the coupling capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

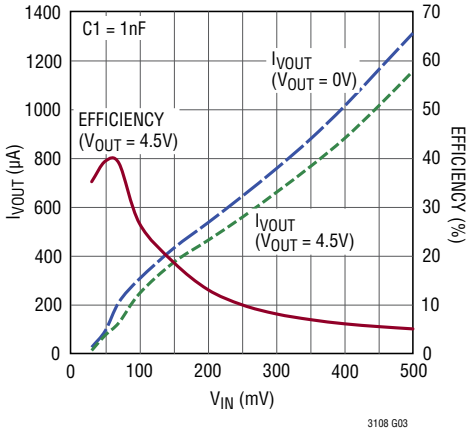
I_{IN} vs V_{IN}, (V_{OUT} = 0V)



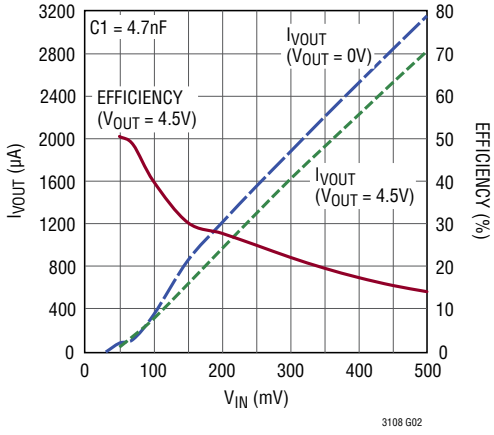
I_{VOUT} and Efficiency vs V_{IN}, 1:20 Ratio Transformer



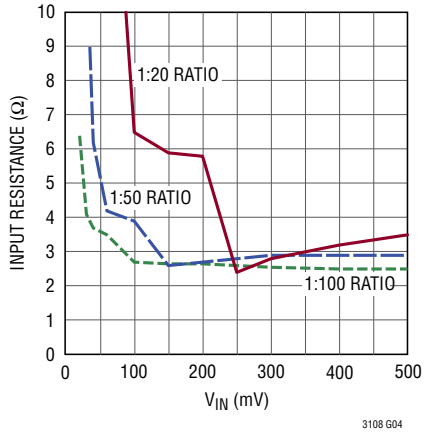
I_{VOUT} and Efficiency vs V_{IN}, 1:100 Ratio Transformer



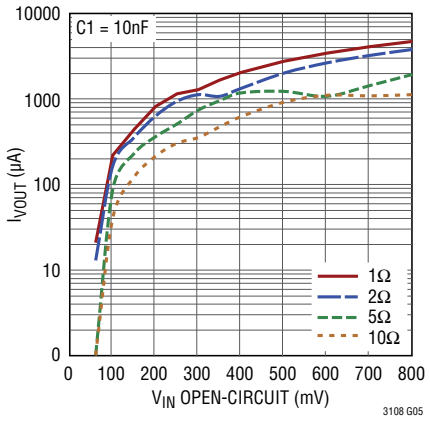
I_{VOUT} and Efficiency vs V_{IN}, 1:50 Ratio Transformer



Input Resistance vs V_{IN} (V_{OUT} Charging)

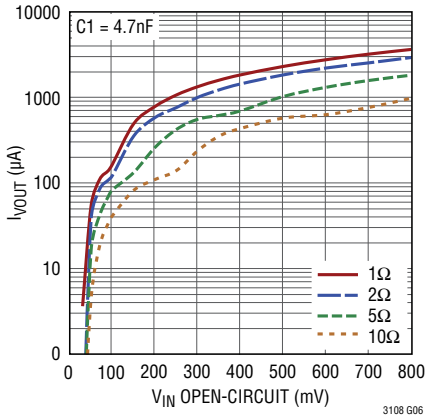


I_{VOUT} vs V_{IN} and Source Resistance, 1:20 Ratio

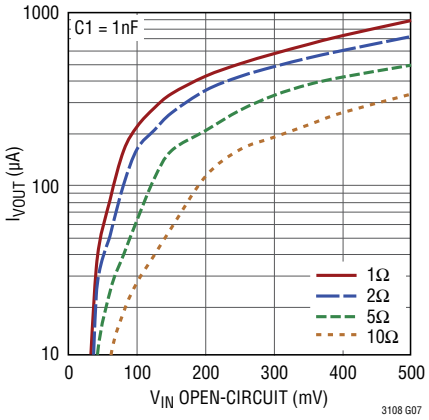


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

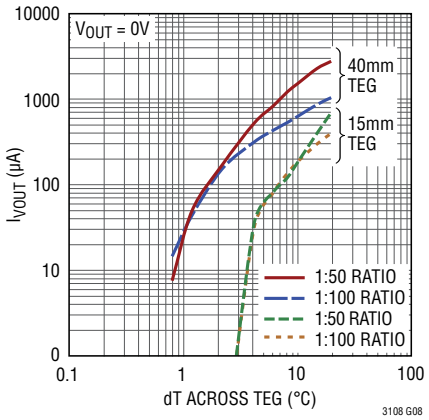
I_{VOUT} vs V_{IN} and Source Resistance, 1:50 Ratio



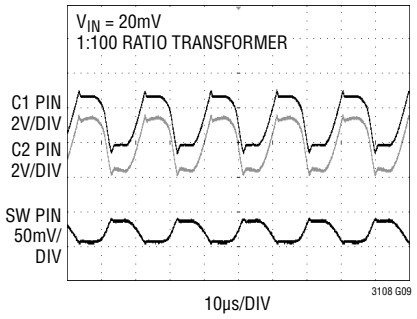
I_{VOUT} vs V_{IN} and Source Resistance, 1:100 Ratio



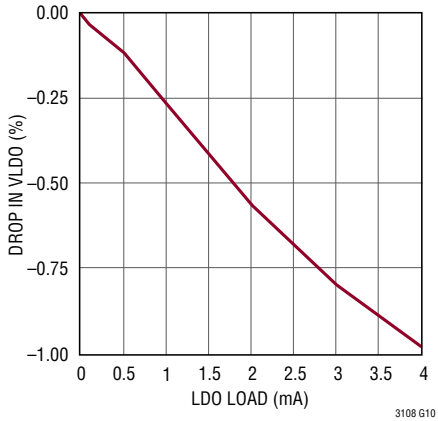
I_{VOUT} vs dT and TEG Size, 1:100 Ratio



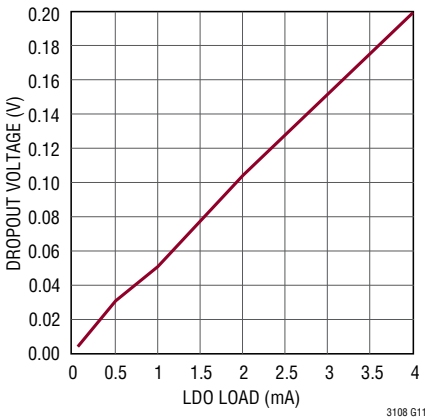
Resonant Switching Waveforms



LDO Load Regulation

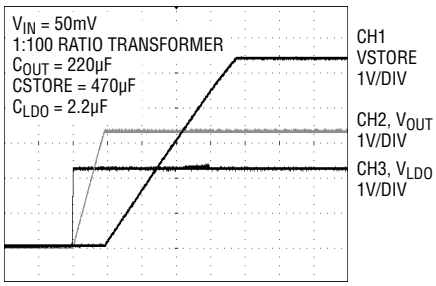


LDO Dropout Voltage

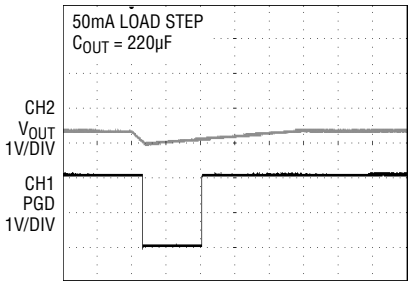


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

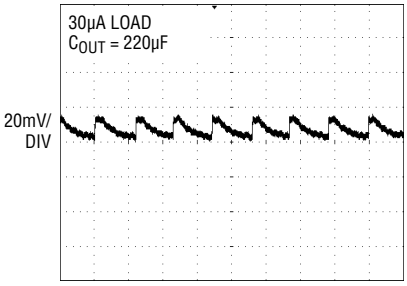
Start-Up Voltage Sequencing



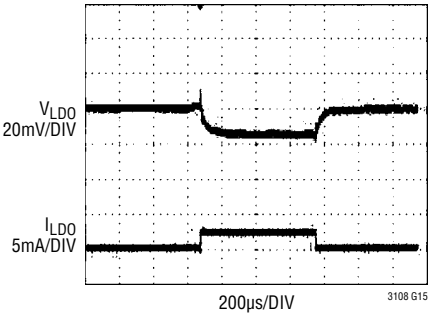
V_{OUT} and PGD Response During a Step Load



V_{OUT} Ripple

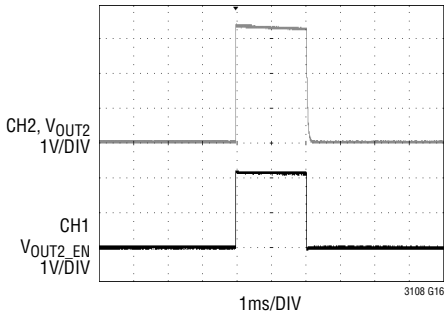


LDO Step Load Response



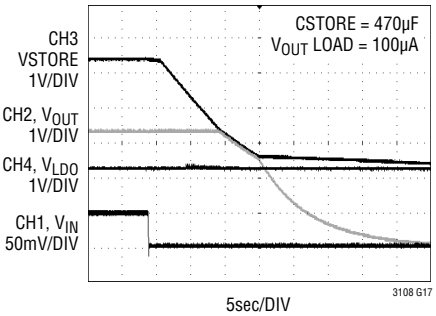
0mA TO 3mA LOAD STEP
C_{LDO} = 2.2µF

Enable Input and V_{OUT2}



10mA LOAD ON V_{OUT2}
C_{OUT} = 220µF

Running on Storage Capacitor



PIN FUNCTIONS (DFN/SSOP)

VAUX (Pin 1/Pin 2): Output of the Internal Rectifier Circuit and V_{CC} for the IC. Bypass VAUX with at least 1µF of capacitance. An active shunt regulator clamps VAUX to 5.25V (typical).

VSTORE (Pin 2/Pin 3): Output for the Storage Capacitor or Battery. A large capacitor may be connected from this pin to GND for powering the system in the event the input voltage is lost. It will be charged up to the maximum VAUX clamp voltage. If not used, this pin should be left open or tied to VAUX.

V_{OUT} (Pin 3/Pin 4): Main Output of the Converter. The voltage at this pin is regulated to the voltage selected by VS1 and VS2 (see Table 1). Connect this pin to an energy storage capacitor or to a rechargeable battery.

V_{OUT2} (Pin 4/Pin 5): Switched Output of the Converter. Connect this pin to a switched load. This output is open until V_{OUT2_EN} is driven high, then it is connected to V_{OUT} through a 1.3Ω P-channel switch. If not used, this pin should be left open or tied to V_{OUT}. The peak current in this output is limited to 0.3A typical.

VLDO (Pin 5/Pin 6): Output of the 2.2V LDO. Connect a 2.2µF or larger ceramic capacitor from this pin to GND. If not used, this pin should be tied to VAUX.

PGD (Pin 6/Pin 7): Power Good Output. When V_{OUT} is within 7.5% of its programmed value, PGD will be pulled up to VLDO through a 1MΩ resistor. If V_{OUT} drops 9% below its programmed value PGD will go low. This pin can sink up to 100µA.

VS2 (Pin 7/Pin 10): V_{OUT} Select Pin 2. Connect this pin to ground or VAUX to program the output voltage (see Table 1).

VS1 (Pin 8/Pin 11): V_{OUT} Select Pin 1. Connect this pin to ground or VAUX to program the output voltage (see Table 1).

V_{OUT2_EN} (Pin 9/Pin 12): Enable Input for V_{OUT2}. V_{OUT2} will be enabled when this pin is driven high. There is an internal 5M pull-down resistor on this pin. If not used, this pin can be left open or grounded.

C1 (Pin 10/Pin 13): Input to the Charge Pump and Rectifier Circuit. Connect a capacitor from this pin to the secondary winding of the step-up transformer.

C2 (Pin 11/Pin 14): Input to the N-Channel Gate Drive Circuit. Connect a capacitor from this pin to the secondary winding of the step-up transformer.

SW (Pin 12/Pin 15): Drain of the Internal N-Channel Switch. Connect this pin to the primary winding of the transformer.

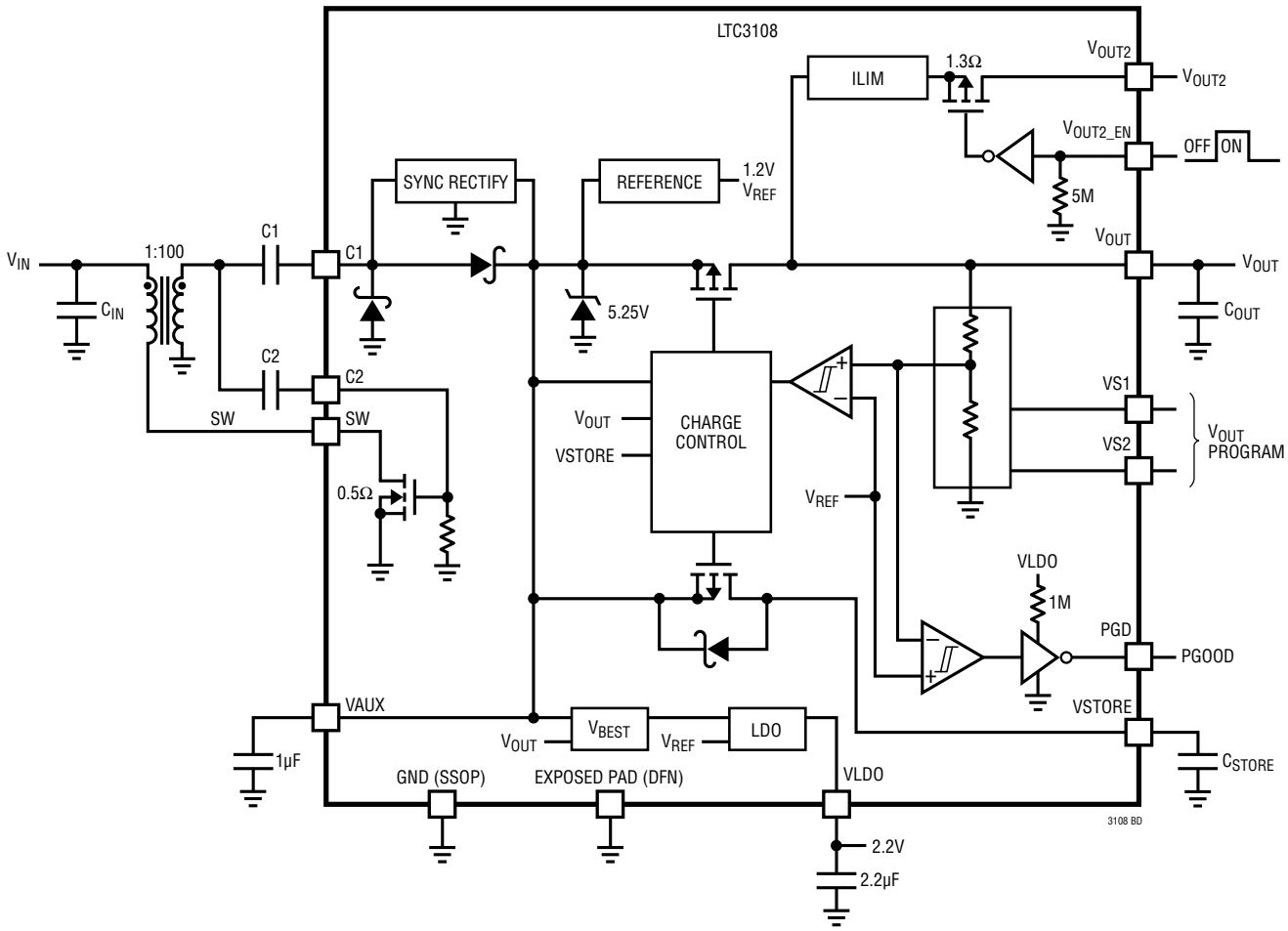
GND (Pins 1, 8, 9, 16) SSOP Only: Ground

GND (Exposed Pad Pin 13) DFN Only: Ground. The DFN exposed pad must be soldered to the PCB ground plane. It serves as the ground connection, and as a means of conducting heat away from the die.

Table 1. Regulated Voltage Using Pins VS1 and VS2

VS2	VS1	V_{OUT}
GND	GND	2.35V
GND	VAUX	3.3V
VAUX	GND	4.1V
VAUX	VAUX	5V

BLOCK DIAGRAM



OPERATION (Refer to the Block Diagram)

The LTC3108 is designed to use a small external step-up transformer to create an ultralow input voltage step-up DC/DC converter and power manager. It is ideally suited for low power wireless sensors and other applications in which surplus energy harvesting is used to generate system power because traditional battery power is inconvenient or impractical.

The LTC3108 is designed to manage the charging and regulation of multiple outputs in a system in which the average power draw is very low, but there may be periodic pulses of higher load current required. This is typical of wireless sensor applications, where the quiescent power draw is extremely low most of the time, except for transmit bursts when circuitry is powered up to make measurements and transmit data.

The LTC3108 can also be used to trickle charge a standard capacitor, supercapacitor or rechargeable battery, using energy harvested from a Peltier or photovoltaic cell.

OPERATION

Oscillator

The LTC3108 utilizes a MOSFET switch to form a resonant step-up oscillator using an external step-up transformer and a small coupling capacitor. This allows it to boost input voltages as low as 20mV high enough to provide multiple regulated output voltages for powering other circuits. The frequency of oscillation is determined by the inductance of the transformer secondary winding and is typically in the range of 10kHz to 100kHz. For input voltages as low as 20mV, a primary-secondary turns ratio of about 1:100 is recommended. For higher input voltages, this ratio can be lower. See the Applications Information section for more information on selecting the transformer.

Charge Pump and Rectifier

The AC voltage produced on the secondary winding of the transformer is boosted and rectified using an external charge pump capacitor (from the secondary winding to pin C1) and the rectifiers internal to the LTC3108. The rectifier circuit feeds current into the VAUX pin, providing charge to the external VAUX capacitor and the other outputs.

VAUX

The active circuits within the LTC3108 are powered from VAUX, which should be bypassed with a 1µF capacitor. Larger capacitor values are recommended when using turns ratios of 1:50 or 1:20 (refer to the Typical Application examples). Once VAUX exceeds 2.5V, the main V_{OUT} is allowed to start charging.

An internal shunt regulator limits the maximum voltage on VAUX to 5.25V typical. It shunts to GND any excess current into VAUX when there is no load on the converter or the input source is generating more power than is required by the load.

Voltage Reference

The LTC3108 includes a precision, micropower reference, for accurate regulated output voltages. This reference becomes active as soon as VAUX exceeds 2V.

Synchronous Rectifiers

Once VAUX exceeds 2V, synchronous rectifiers in parallel with each of the internal diodes take over the job of rectifying the input voltage, improving efficiency.

Low Dropout Linear Regulator (LDO)

The LTC3108 includes a low current LDO to provide a regulated 2.2V output for powering low power processors or other low power ICs. The LDO is powered by the higher of VAUX or V_{OUT}. This enables it to become active as soon as VAUX has charged to 2.3V, while the V_{OUT} storage capacitor is still charging. In the event of a step load on the LDO output, current can come from the main V_{OUT} capacitor if VAUX drops below V_{OUT}. The LDO requires a 2.2µF ceramic capacitor for stability. Larger capacitor values can be used without limitation, but will increase the time it takes for all the outputs to charge up. The LDO output is current limited to 4mA minimum.

V_{OUT}

The main output voltage on V_{OUT} is charged from the VAUX supply, and is user programmed to one of four regulated voltages using the voltage select pins VS1 and VS2, according to Table 2. Although the logic threshold voltage for VS1 and VS2 is 0.85V typical, it is recommended that they be tied to ground or VAUX.

Table 2. Regulated Voltage Using Pins VS1 and VS2

VS2	VS1	V_{OUT}
GND	GND	2.35V
GND	VAUX	3.3V
VAUX	GND	4.1V
VAUX	VAUX	5V

When the output voltage drops slightly below the regulated value, the charging current will be enabled as long as VAUX is greater than 2.5V. Once V_{OUT} has reached the proper value, the charging current is turned off.

The internal programmable resistor divider sets V_{OUT}, eliminating the need for very high value external resistors that are susceptible to board leakage.

OPERATION

In a typical application, a storage capacitor (typically a few hundred microfarads) is connected to V_{OUT}. As soon as VAUX exceeds 2.5V, the V_{OUT} capacitor will be allowed to charge up to its regulated voltage. The current available to charge the capacitor will depend on the input voltage and transformer turns ratio, but is limited to about 4.5mA typical.

PGOOD

A power good comparator monitors the V_{OUT} voltage. The PGD pin is an open-drain output with a weak pull-up (1MΩ) to the LDO voltage. Once V_{OUT} has charged to within 7.5% of its regulated voltage, the PGD output will go high. If V_{OUT} drops more than 9% from its regulated voltage, PGD will go low. The PGD output is designed to drive a microprocessor or other chip I/O and is not intended to drive a higher current load such as an LED. Pulling PGD up externally to a voltage greater than VLDO will cause a small current to be sourced into VLDO. PGD can be pulled low in a wire-OR configuration with other circuitry.

V_{OUT2}

V_{OUT2} is an output that can be turned on and off by the host, using the V_{OUT2_EN} pin. When enabled, V_{OUT2} is connected to V_{OUT} through a 1.3Ω P-channel MOSFET switch. This output, controlled by a host processor, can be used to power external circuits such as sensors and amplifiers, that do not have a low power sleep or shutdown capability. V_{OUT2} can be used to power these circuits only when they are needed.

Minimizing the amount of decoupling capacitance on V_{OUT2} will allow it to be switched on and off faster, allowing shorter burst times and, therefore, smaller duty cycles in pulsed applications such as a wireless sensor/transmitter. A small V_{OUT2} capacitor will also minimize the energy that will be wasted in charging the capacitor every time V_{OUT2} is enabled.

V_{OUT2} has a soft-start time of about 5µs to limit capacitor charging current and minimize glitching of the main output when V_{OUT2} is enabled. It also has a current limiting circuit that limits the peak current to 0.3A typical.

The V_{OUT2} enable input has a typical threshold of 1V with 100mV of hysteresis, making it logic-compatible. If V_{OUT2_EN} (which has an internal pull-down resistor) is low, V_{OUT2} will be off. Driving V_{OUT2_EN} high will turn on the V_{OUT2} output.

Note that while V_{OUT2_EN} is high, the current limiting circuitry for V_{OUT2} draws an extra 8µA of quiescent current from V_{OUT}. This added current draw has a negligible effect on the application and capacitor sizing, since the load on the V_{OUT2} output, when enabled, is likely to be orders of magnitude higher than 8µA.

VSTORE

The VSTORE output can be used to charge a large storage capacitor or rechargeable battery after V_{OUT} has reached regulation. Once V_{OUT} has reached regulation, the VSTORE output will be allowed to charge up to the VAUX voltage. The storage element on VSTORE can be used to power the system in the event that the input source is lost, or is unable to provide the current demanded by the V_{OUT}, V_{OUT2} and LDO outputs. If VAUX drops below VSTORE, the LTC3108 will automatically draw current from the storage element. Note that it may take a long time to charge a large capacitor, depending on the input energy available and the loading on V_{OUT} and VLDO.

Since the maximum current from VSTORE is limited to a few milliamps, it can safely be used to trickle-charge NiCd or NiMH rechargeable batteries for energy storage when the input voltage is lost. Note that the VSTORE capacitor cannot supply large pulse currents to V_{OUT}. Any pulse load on V_{OUT} must be handled by the V_{OUT} capacitor.

Short-Circuit Protection

All outputs of the LTC3108 are current limited to protect against short-circuits to ground.

Output Voltage Sequencing

A timing diagram showing the typical charging and voltage sequencing of the outputs is shown in Figure 1. Note: time not to scale.

OPERATION

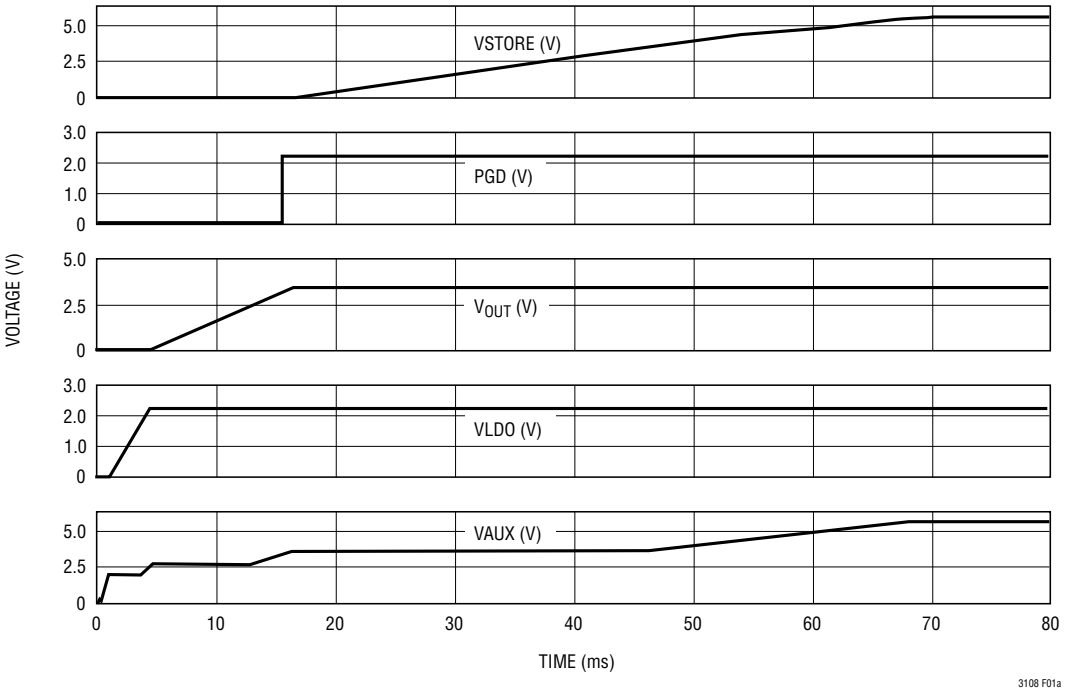


Figure 1. Output Voltage Sequencing with V_{OUT} Programmed for 3.3V (Time Not to Scale)

APPLICATIONS INFORMATION

Introduction

The LTC3108 is designed to gather energy from very low input voltage sources and convert it to usable output voltages to power microprocessors, wireless transmitters and analog sensors. Such applications typically require much more peak power, and at higher voltages, than the input voltage source can produce. The LTC3108 is designed to accumulate and manage energy over a long period of time to enable short power bursts for acquiring and transmitting data. The bursts must occur at a low enough duty cycle such that the total output energy during the burst does not exceed the average source power integrated over the accumulation time between bursts. For many applications, this time between bursts could be seconds, minutes or hours.

The PGD signal can be used to enable a sleeping microprocessor or other circuitry when V_{OUT} reaches regulation, indicating that enough energy is available for a burst.

Input Voltage Sources

The LTC3108 can operate from a number of low input voltage sources, such as Peltier cells, photovoltaic cells or thermopile generators. The minimum input voltage required for a given application will depend on the transformer turns ratio, the load power required, and the internal DC resistance (ESR) of the voltage source. Lower ESR will allow the use of lower input voltages, and provide higher output power capability.

Refer to the I_{IN} vs V_{IN} curves in the Typical Performance Characteristics section to see what input current is required from the source for a given input voltage.

For a given transformer turns ratio, there is a maximum recommended input voltage to avoid excessively high secondary voltages and power dissipation in the shunt regulator. It is recommended that the maximum input voltage times the turns ratio be less than 50.

Note that a low ESR bulk decoupling capacitor will usually be required across the input source to prevent large voltage droop and ripple caused by the source's ESR and the peak primary switching current (which can reach hundreds of milliamps). The time constant of the filter capacitor and the ESR of the voltage source should be much longer than the period of the resonant switching frequency.

Peltier Cell (Thermoelectric Generator)

A Peltier cell (also known as a thermoelectric cooler) is made up of a large number of series-connected P-N junctions, sandwiched between two parallel ceramic plates. Although Peltier cells are often used as coolers by applying a DC voltage to their inputs, they will also generate a DC output voltage, using the Seebeck effect, when the two plates are at different temperatures. The polarity of the output voltage will depend on the polarity of the temperature differential between the plates. The magnitude of the output voltage is proportional to the magnitude of the temperature differential between the plates. When used in

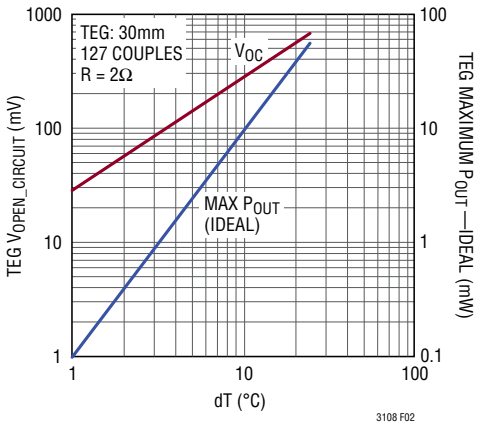


Figure 2. Typical Performance of a Peltier Cell Acting as a Thermoelectric Generator

APPLICATIONS INFORMATION

this manner, a Peltier cell is referred to as a thermoelectric generator (TEG).

The low voltage capability of the LTC3108 design allows it to operate from a TEG with temperature differentials as low as 1°C, making it ideal for harvesting energy in applications in which a temperature difference exists between two surfaces or between a surface and the ambient temperature. The internal resistance (ESR) of most cells is in the range of 1Ω to 5Ω, allowing for reasonable power transfer. The curves in Figure 2 show the open-circuit output voltage and maximum power transfer for a typical Peltier cell (with an ESR of 2Ω) over a 20°C range of temperature differential.

TEG Load Matching

The LTC3108 was designed to present a minimum input resistance (load) in the range of 2Ω to 10Ω, depending on input voltage and transformer turns ratio (as shown in the Typical Performance Characteristics curves). For a given turns ratio, as the input voltage drops, the input resistance increases. This feature allows the LTC3108 to optimize power transfer from sources with a few ohms of source resistance, such as a typical TEG. Note that a lower source resistance will always provide more output current capability by providing a higher input voltage under load.

Peltier Cell (TEG) Suppliers

Peltier cells are available in a wide range of sizes and power capabilities, from less than 10mm square to over 50mm square. They are typically 2mm to 5mm in height. A list of Peltier cell manufacturers is given in Table 3.

Table 3. Peltier Cell Manufacturers

CUI, Inc. www.cui.com (Distributor)
Fujitaka www.fujitaka.com/pub/peltier/english/thermoelectric_power.html
Ferrotec www.ferrotec.com/products/thermal/modules
Kryotherm www.kryothermusa.com
Laird Technologies www.lairdtech.com
Marlow Industries www.marlow.com
Micropelt www.micropelt.com
Nextreme www.nextreme.com
TE Technology www.tetech.com/Peltier-Thermoelectric-Cooler-Modules.html
Tellurex www.tellurex.com

Table 4. Recommended TEG Part Numbers by Size

MANUFACTURER	15mm × 15mm	20mm × 20mm	30mm × 30mm	40mm × 40mm
CUI Inc. (Distributor)	CP60133	CP60233	CP60333	CP85438
Ferrotec	9501/031/030 B	9501/071/040 B	9500/097/090 B	9500/127/100 B
Fujitaka	FPH13106NC	FPH17106NC	FPH17108AC	FPH112708AC
Kryotherm			TGM-127-1.0-0.8	LCB-127-1.4-1.15
Laird Technology			PT6.7.F2.3030.W6	PT8.12.F2.4040.TA.W6
Marlow Industries		RC3-8-01	RC6-6-01	RC12-8-01LS
Tellurex	C2-15-0405	C2-20-0409	C2-30-1505	C2-40-1509
TE Technology	TE-31-1.0-1.3	TE-31-1.4-1.15	TE-71-1.4-1.15	TE-127-1.4-1.05

APPLICATIONS INFORMATION

Thermopile Generator

Thermopile generators (also called powerpile generators) are made up of a number of series-connected thermocouples enclosed in a metal tube. They are commonly used in gas burner applications to generate a DC output of hundreds of millivolts when exposed to the high temperature of a flame. Typical examples are the Honeywell CQ200 and Q313. These devices have an internal series resistance of less than 3Ω, and can generate as much as 750mV open-circuit at their highest rated temperature. For applications in which the temperature rise is too high for a solid-state thermoelectric device, a thermopile can be used as an energy source to power the LTC3108. Because of the higher output voltages possible with a thermopile generator, a lower transformer turns ratio can be used (typically 1:20, depending on the application).

Photovoltaic Cell

The LTC3108 converter can also operate from a single photovoltaic cell (also known as a PV or solar cell) at light levels too low for other low input voltage boost converters to operate. However, many variables will affect the performance in these applications. Light levels can vary over several orders of magnitude and depend on lighting conditions (the type of lighting and indoor versus outdoor). Different types of light (sunlight, incandescent, fluorescent) also have different color spectra, and will produce different output power levels depending on which type of photovoltaic cell is being used (monocrystalline, polycrystalline or thin-film). Therefore, the photovoltaic cell must be chosen for the type and amount of light available. Note that the short-circuit output current from the cell must be at least a few milliamps in order to power the LTC3108 converter

Non-Boost Applications

The LTC3108 can also be used as an energy harvester and power manager for input sources that do not require boosting. In these applications the step-up transformer can be eliminated.

Any source whose peak voltage exceeds 2.5V AC or 5V DC can be connected to the C1 input through a current-limiting resistor where it will be rectified/peak detected. In these applications the C2 and SW pins are not used and can be grounded or left open.

Examples of such input sources would be piezoelectric transducers, vibration energy harvesters, low current generators, a stack of low current solar cells or a 60Hz AC input.

A series resistance of at least 100Ω/V should be used to limit the maximum current into the VAUX shunt regulator.

COMPONENT SELECTION

Step-Up Transformer

The step-up transformer turns ratio will determine how low the input voltage can be for the converter to start. Using a 1:100 ratio can yield start-up voltages as low as 20mV. Other factors that affect performance are the DC resistance of the transformer windings and the inductance of the windings. Higher DC resistance will result in lower efficiency. The secondary winding inductance will determine the resonant frequency of the oscillator, according to the following formula.

$$\text{Frequency} = \frac{1}{2 \bullet \pi \bullet \sqrt{L(\text{sec}) \bullet C}} \text{ Hz}$$

Where L is the inductance of the transformer secondary winding and C is the load capacitance on the secondary winding. This is comprised of the input capacitance at pin C2, typically 30pF, in parallel with the transformer secondary winding's shunt capacitance. The recommended resonant frequency is in the range of 10kHz to 100kHz. See Table 5 for some recommended transformers.

Table 5. Recommended Transformers

VENDOR	PART NUMBER
Coilcraft www.coilcraft.com	LPR6235-752SML (1:100 Ratio) LPR6235-253PML (1:20 Ratio) LPR6235-123QML (1:50 Ratio)
Würth www.we-online	74488540070 (1:100 Ratio) 74488540120 (1:50 Ratio) 74488540250 (1:20 Ratio)

APPLICATIONS INFORMATION

C1 Capacitor

The charge pump capacitor that is connected from the transformer's secondary winding to the C1 pin has an effect on converter input resistance and maximum output current capability. Generally, a minimum value of 1nF is recommended when operating from very low input voltages using a transformer with a ratio of 1:100. Too large a capacitor value can compromise performance when operating at low input voltage or with high resistance sources. For higher input voltages and lower turns ratios, the value of the C1 capacitor can be increased for higher output current capability. Refer to the Typical Applications schematic examples for the recommended value for a given turns ratio.

Squegging

Certain types of oscillators, including transformer-coupled oscillators such as the resonant oscillator of the LTC3108, can exhibit a phenomenon called squegging. This term refers to a condition that can occur which blocks or stops the oscillation for a period of time much longer than the period of oscillation, resulting in bursts of oscillation. An example of this is the blocking oscillator, which is designed to squegg to produce bursts of oscillation. Squegging is also encountered in RF oscillators and regenerative receivers.

In the case of the LTC3108, squegging can occur when a charge builds up on the C2 gate coupling capacitor, such that the DC bias point shifts and oscillation is extinguished for a certain period of time, until the charge on the capacitor bleeds off, allowing oscillation to resume. It is difficult to predict when and if squegging will occur in a given application. While squegging is not harmful, it reduces the average output current capability of the LTC3108.

Squegging can easily be avoided by the addition of a bleeder resistor in parallel with the coupling capacitor on the C2 pin. Resistor values in the range of 100k to 1MΩ are sufficient to eliminate squegging without having any negative impact on performance. For the 330pF capacitor used for C2 in most applications, a 499k bleeder resistor is recommended. See the Typical Applications schematics for an example.

Using External Charge Pump Rectifiers

The synchronous charge pump rectifiers in the LTC3108 (connected to the C1 pin) are optimized for operation from very low input voltage sources, using typical transformer step-up ratios between 1:100 and 1:50, and typical C1 charge pump capacitor values less than 10nF.

Operation from higher input voltage sources (typically 250mV or greater, under load), allows the use of lower transformer step-up ratios (such as 1:20 and 1:10) and larger C1 capacitor values to provide higher output current capability from the LTC3108. However, due to the resulting increase in rectifier currents and resonant oscillator frequency in these applications, the use of external charge pump rectifiers is recommended for optimal performance.

In applications where the step-up ratio is 1:20 or less, and the C1 capacitor is 10nF or greater, the C1 pin should be grounded and two external rectifiers (such as 1N4148 or 1N914 diodes) should be used. These are available as dual diodes in a single package. Avoid the use of Schottky rectifiers, as their lower forward voltage drop increases the minimum start-up voltage. See the Typical Applications schematics for an example.

V_{OUT} and VSTORE Capacitor

For pulsed load applications, the V_{OUT} capacitor should be sized to provide the necessary current when the load is pulsed on. The capacitor value required will be dictated by the load current, the duration of the load pulse, and the amount of voltage droop the circuit can tolerate. The capacitor must be rated for whatever voltage has been selected for V_{OUT} by VS1 and VS2.

$$C_{OUT}(\mu F) \geq \frac{I_{LOAD}(mA) \bullet t_{PULSE}(ms)}{V_{OUT}(V)}$$

Note that there must be enough energy available from the input voltage source for V_{OUT} to recharge the capacitor during the interval between load pulses (to be discussed in the next example). Reducing the duty cycle of the load pulse will allow operation with less input energy.

APPLICATIONS INFORMATION

The VSTORE capacitor may be of very large value (thousands of microfarads or even Farads), to provide holdup at times when the input power may be lost. Note that this capacitor can charge all the way to 5.25V (regardless of the settings for V_{OUT}), so ensure that the holdup capacitor has a working voltage rating of at least 5.5V at the temperature for which it will be used. The VSTORE capacitor can be sized using the following:

$$C_{STORE} \geq \frac{[6\mu A + I_Q + I_{LDO} + (I_{BURST} \bullet t \bullet f)] \bullet TSTORE}{5.25 - V_{OUT}}$$

Where 6µA is the quiescent current of the LTC3108, I_Q is the load on V_{OUT} in between bursts, I_{LDO} is the load on the LDO between bursts, I_{BURST} is the total load during the burst, t is the duration of the burst, f is the frequency of the bursts, TSTORE is the storage time required and V_{OUT} is the output voltage required. Note that for a programmed output voltage of 5V, the VSTORE capacitor cannot provide any beneficial storage time.

To minimize losses and capacitor charge time, all capacitors used for V_{OUT} and VSTORE should be low leakage. See Table 6 for recommended storage capacitors.

Table 6. Recommended Storage Capacitors

VENDOR	PART NUMBER/SERIES
AVX www.avx.com	BestCap Series TAJ and TPS Series Tantalum
Cap-XX www.cap-xx.com	GZ Series
Cooper/Bussmann www.bussmann.com/3/PowerStor.html	KR Series P Series
Vishay/Sprague www.vishay.com/capacitors	Tantamount 592D 595D Tantalum 150CRZ/153CRV Aluminum 013 RLC (Low Leakage)

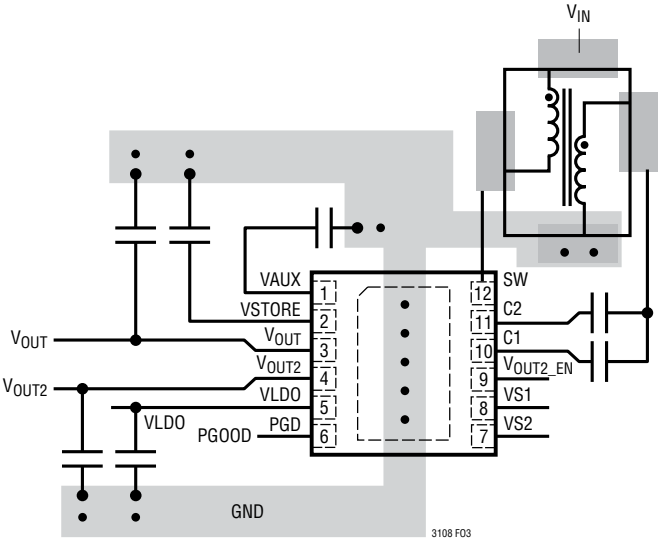
Storage capacitors requiring voltage balancing are not recommended due to the current draw of the balancing resistors.

PCB Layout Guidelines

Due to the rather low switching frequency of the resonant converter and the low power levels involved, PCB layout is not as critical as with many other DC/DC converters. There are, however, a number of things to consider.

Due to the very low input voltage the circuit may operate from, the connections to V_{IN}, the primary of the transformer and the SW and GND pins of the LTC3108 should be designed to minimize voltage drop from stray resistance and able to carry currents as high as 500mA. Any small voltage drop in the primary winding conduction path will lower efficiency and increase capacitor charge time.

Also, due to the low charge currents available at the outputs of the LTC3108, any sources of leakage current on the output voltage pins must be minimized. An example board layout is shown in Figure 3.



• VIAS TO GROUND PLANE

Figure 3. Example Component Placement for Two-Layer PC Board (DFN Package)

Design Example 1

This design example will explain how to calculate the necessary storage capacitor value for V_{OUT} in pulsed load applications, such as a wireless sensor/transmitter. In these types of applications, the load is very small for a majority of the time (while the circuitry is in a low power sleep state), with bursts of load current occurring periodically during a transmit burst. The storage capacitor on V_{OUT} supports the load during the transmit burst, and the long sleep time between bursts allows the LTC3108 to recharge the capacitor. A method for calculating the maximum rate

APPLICATIONS INFORMATION

at which the load pulses can occur for a given output current from the LTC3108 will also be shown.

In this example, V_{OUT} is set to 3.3V, and the maximum allowed voltage droop during a transmit burst is 10%, or 0.33V. The duration of a transmit burst is 1ms, with a total average current requirement of 40mA during the burst. Given these factors, the minimum required capacitance on V_{OUT} is:

$$C_{OUT}(\mu F) \geq \frac{40mA \bullet 1ms}{0.33V} = 121\mu F$$

Note that this equation neglects the effect of capacitor ESR on output voltage droop. For most ceramic or low ESR tantalum capacitors, the ESR will have a negligible effect at these load currents.

A standard value of 150µF or larger could be used for C_{OUT} in this case. Note that the load current is the total current draw on V_{OUT}, V_{OUT2} and VLDO, since the current for all of these outputs must come from V_{OUT} during a burst. Current contribution from the holdup capacitor on VSTORE is not considered, since it may not be able to recharge between bursts. Also, it is assumed that the charge current from the LTC3108 is negligible compared to the magnitude of the load current during the burst.

To calculate the maximum rate at which load bursts can occur, determine how much charge current is available from the LTC3108 V_{OUT} pin given the input voltage source being used. This number is best found empirically, since there are many factors affecting the efficiency of the converter. Also determine what the total load current is on V_{OUT} during the sleep state (between bursts). Note that this must include any losses, such as storage capacitor leakage.

Assume, for instance, that the charge current from the LTC3108 is 50µA and the total current drawn on V_{OUT} in the sleep state is 17µA, including capacitor leakage. In addition, use the value of 150µF for the V_{OUT} capacitor. The maximum transmit rate (neglecting the duration of the transmit burst, which is typically very short) is then given by:

$$t = \frac{150\mu F \bullet 0.33V}{(50\mu A - 17\mu A)} = 1.5sec \text{ or } f_{MAX} = 0.666Hz$$

Therefore, in this application example, the circuit can support a 1ms transmit burst every 1.5 seconds.

It can be determined that for systems that only need to transmit every few seconds (or minutes or hours), the average charge current required is extremely small, as long as the sleep current is low. Even if the available charge current in the example above was only 10µA and the sleep current was only 5µA, it could still transmit a burst every ten seconds.

The following formula enables the user to calculate the time it will take to charge the LDO output capacitor and the V_{OUT} capacitor the first time, from 0V. Here again, the charge current available from the LTC3108 must be known. For this calculation, it is assumed that the LDO output capacitor is 2.2µF.

$$t_{LDO} = \frac{2.2V \bullet 2.2\mu F}{I_{CHG} - I_{LDO}}$$

If there were 50µA of charge current available and a 5µA load on the LDO (when the processor is sleeping), the time for the LDO to reach regulation would be 107ms.

If V_{OUT} were programmed to 3.3V and the V_{OUT} capacitor was 150µF, the time for V_{OUT} to reach regulation would be:

$$t_{VOUT} = \frac{3.3V \bullet 150\mu F}{I_{CHG} - I_{VOUT} - I_{LDO}} + t_{LDO}$$

If there were 50µA of charge current available and 5µA of load on V_{OUT}, the time for V_{OUT} to reach regulation after the initial application of power would be 12.5 seconds.

Design Example 2

In many pulsed load applications, the duration, magnitude and frequency of the load current bursts are known and fixed. In these cases, the average charge current required from the LTC3108 to support the average load must be calculated, which can be easily done by the following:

$$I_{CHG} \geq I_Q + \frac{I_{BURST} \bullet t}{T}$$

Where I_Q is the sleep current on V_{OUT} required by the external circuitry in between bursts (including cap leakage), I_{BURST} is the total load current during the burst, t is the

APPLICATIONS INFORMATION

duration of the burst and T is the period of the transmit burst rate (essentially the time between bursts).

In this example, I_Q = 5µA, I_{BURST} = 100mA, t = 5ms and T = one hour. The average charge current required from the LTC3108 would be:

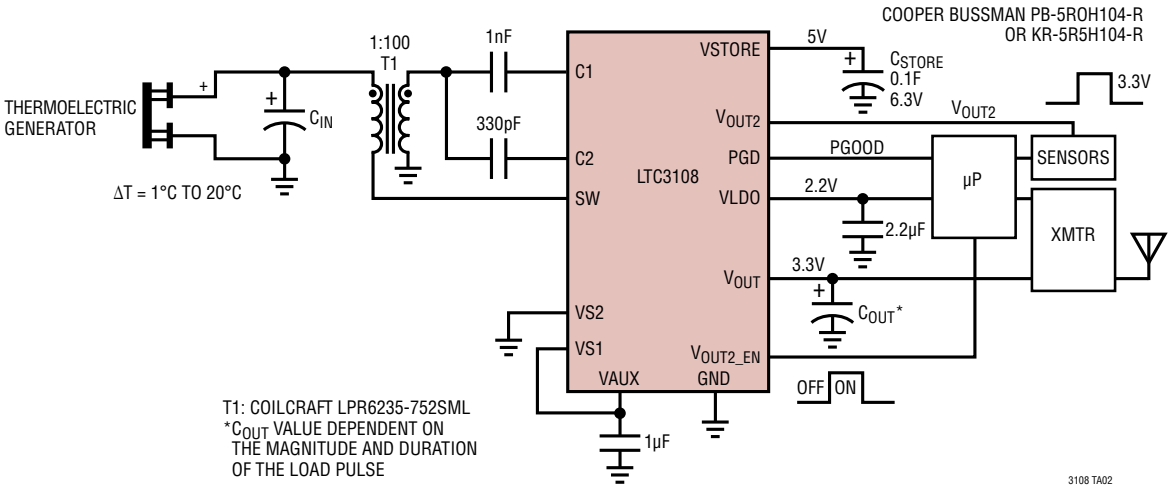
$$I_{CHG} \geq 5\mu A + \frac{100mA \bullet 0.005sec}{3600sec} = 5.14\mu A$$

Therefore, if the LTC3108 has an input voltage that allows it to supply a charge current greater than 5.14µA, the application can support 100mA bursts lasting 5ms every hour. It can be determined that the sleep current of 5µA is the dominant factor because the transmit duty cycle is so small (0.00014%). Note that for a V_{OUT} of 3.3V, the average power required by this application is only 17µW (not including converter losses).

Note that the charge current available from the LTC3108 has no effect on the sizing of the V_{OUT} capacitor (if it is assumed that the load current during a burst is much larger than the charge current), and the V_{OUT} capacitor has no effect on the maximum allowed burst rate.

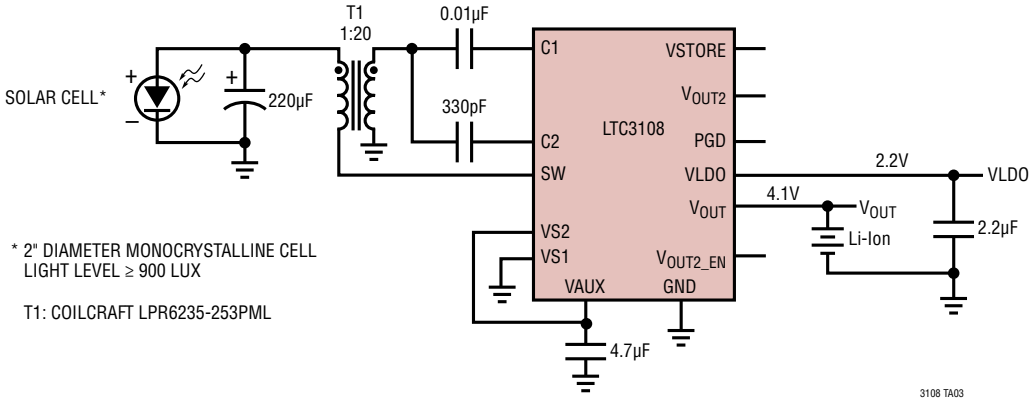
TYPICAL APPLICATIONS

Peltier-Powered Energy Harvester for Remote Sensor Applications

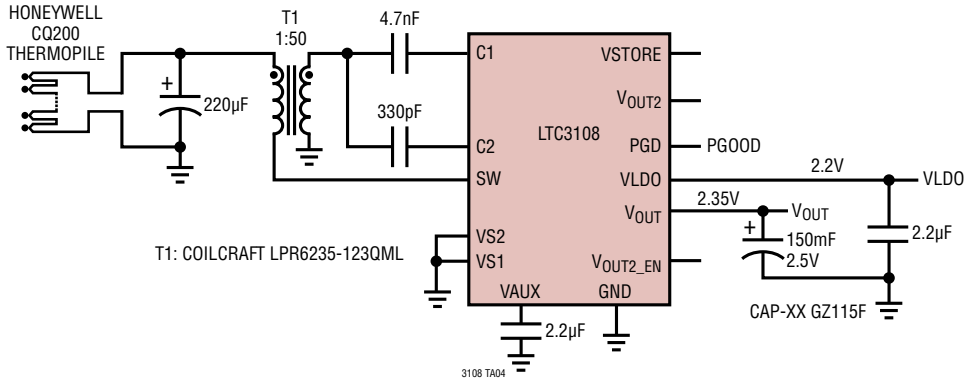


TYPICAL APPLICATIONS

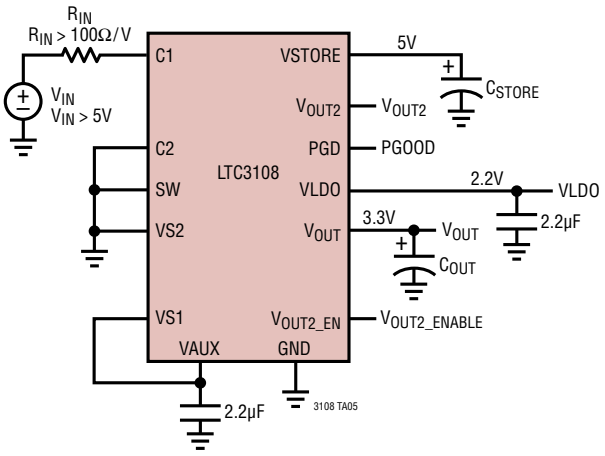
Li-Ion Battery Charger and LDO Powered by a Solar Cell



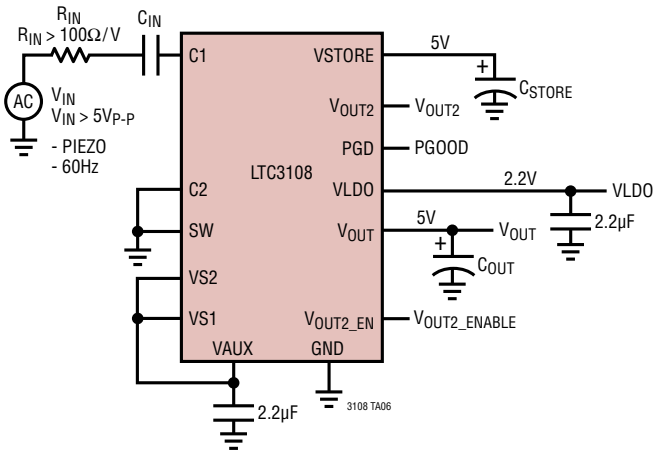
Supercapacitor Charger and LDO Powered by a Thermopile Generator



DC Input Energy Harvester and Power Manager



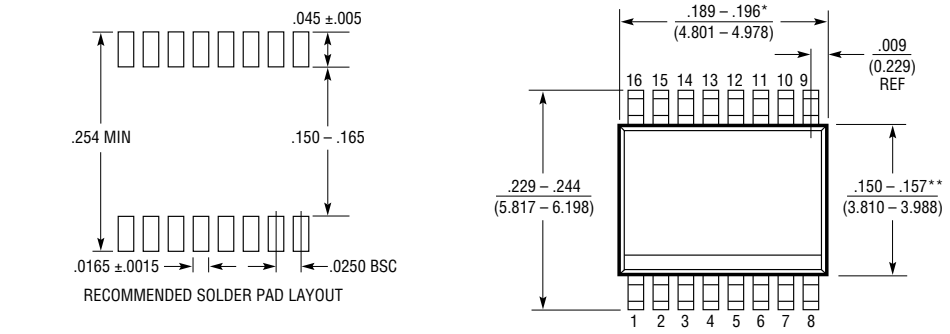
AC Input Energy Harvester and Power Manager



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)

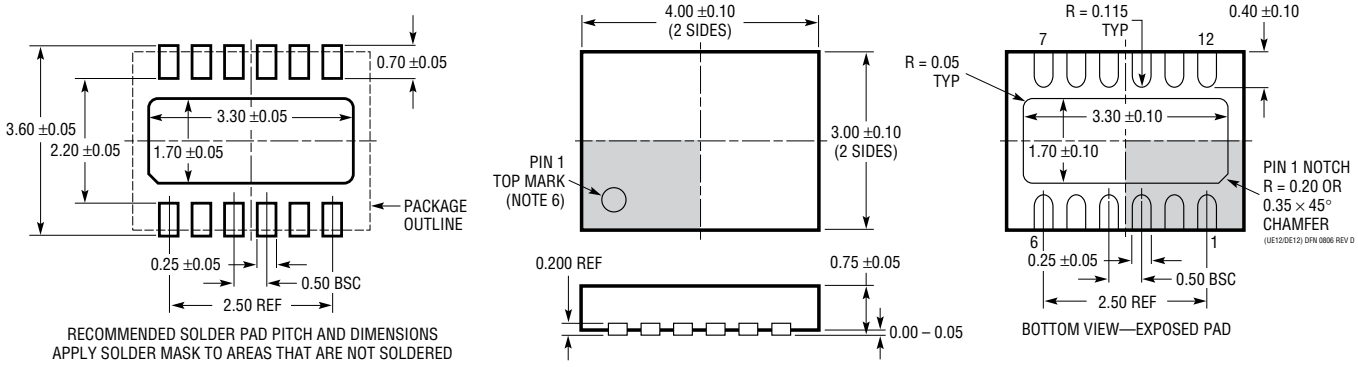


NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695 Rev D)



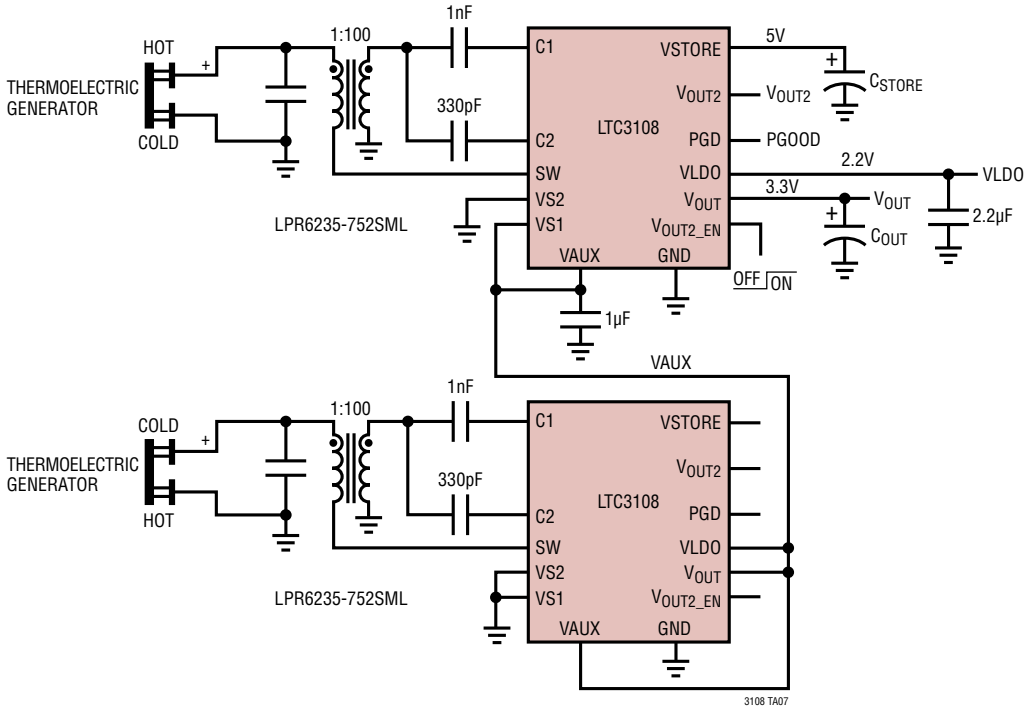
NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/10	Updated front page text and Typical Appliction	1
		Updated Absolute Maximum Ratings and Order Information sections	2
		Updated Electrical Characteristics	3
		Added graph (3108 G00) to Typical Performance Characteristics	4
		Updated Block Diagram	8
		Text added to Operation section	9
		Changes to Applications Information section	12-18
		Updated Typical Applications	18, 19, 22
		Updated Related Parts	22
B	06/13	Added vendor information to Table 5	14
C	08/13	Changed Würth transformer part numbers	14

TYPICAL APPLICATION

Dual TEG Energy Harvester Operates from Temperature Differentials of Either Polarity

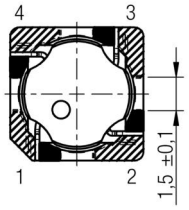


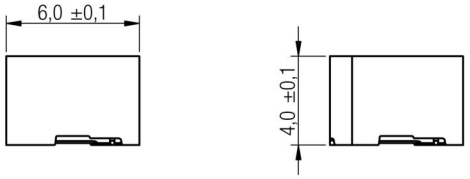
RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1041	Bang-Bang Controller	V_{IN}: 2.8V to 16V; I_Q = 1µA; SO-8 Package
LTC1389	Nanopower Precision Shunt Voltage Reference	$V_{OUT(MIN)}$ = 1.25V; I_Q = 0.8µA; SO-8 Package
LT1672/LT1673/ LT1674	Single-/Dual-/Quad-Precision 2µA Rail-to-Rail Op Amps	SO-8, SO-14 and MSOP-8 Packages
LT3009	3µA I_Q, 20mA Linear Regulator	V_{IN}: 1.6V to 20V; $V_{OUT(MIN)}$: 0.6V to Adj, 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V to Fixed; I_Q = 3µA; I_{SD} < 1µA; 2mm × 2mm DFN-8 and SC70 Packages
LTC3108-1	Ultralow Voltage Step-Up Converter and Power Manager	V_{IN}: 0.02V to 1V; V_{OUT} = 2.5V, 3V, 3.7V, 4.5V Fixed; I_Q = 6µA; 3mm × 4mm DFN-12 and SSOP-16 Packages
LTC3525L-3/ LTC3525L-3.3/ LTC3525L-5	400mA (I_{SW}), Synchronous Step-Up DC/DC Converter with Output Disconnect	V_{IN}: 0.7V to 4V; $V_{OUT(MIN)}$ = $5V_{MAX}$; I_Q = 7µA; I_{SD} < 1µA; SC70 Package
LTC3588-1	Piezoelectric Energy Generator with Integrated High Efficiency Buck Converter	V_{IN}: 2.7V to 20V; $V_{OUT(MIN)}$: Fixed to 1.8V, 2.5V, 3.3V, 3.6V; I_Q = 0.95µA; 3mm × 3mm DFN-10 and MSOP-10E Packages
LTC3642	45V, 50mA Synchronous MicroPower Buck Converter	V_{IN}: 4.5V to 45V, $60V_{MAX}$; $V_{OUT(MIN)}$: 0.8V to Adj, 3.3V Fixed, 5V Fixed; I_Q = 12µA; I_{SD} < 1µA; 3mm × 3mm DFN-8 and MSOP-8E Packages
LTC6656	850mA Precision Reference	Series Low Dropout Precision
LT8410/ LT8410-1	MicroPower 25mA/8mA Low Noise Boost Converter with Integrated Schottky Diode and Output Disconnect	V_{IN}: 2.6V to 16V; $V_{OUT(MIN)}$ = $40V_{MAX}$; I_Q = 8.5µA; I_{SD} < 1µA; 2mm × 2mm DFN-8 Package
LTC4070	Micropower Shunt Li-Ion Charge	Controls Charging with µA Source

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC3108
LT 0813 REV C • PRINTED IN USA

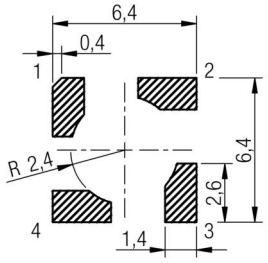
A Dimensions: [mm]





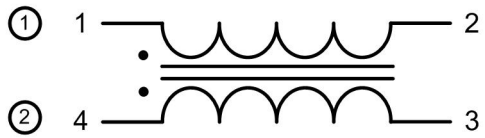
Scale - 3:1

B Recommended land pattern: [mm]



Scale - 3:1

C Schematic:



D Electrical Properties:

Properties	Test conditions		Value	Unit	Tol.
Inductance 1	100 kHz/ 250 mV	L_1	7.5	µH	±20%
Inductance 2	100 kHz/ 250 mV	L_2	75000	µH	±20%
Rated current	ΔT = 40 K	I_{R1}	1.9	A	max.
Saturation current	I∆L/LI < 10%	I_{sat1}	1.3	A	typ.
DC Resistance 1	@ 20°C	R_{DC1}	0.085	Ω	typ.
DC Resistance 2	@ 20°C	R_{DC2}	205.0	Ω	typ.
DC Resistance 1	@ 20°C	R_{DC1}	0.095	Ω	max.
DC Resistance 2	@ 20°C	R_{DC2}	240.0	Ω	max.
Turns ratio		n	1 : 100		
Rated voltage		U_R	80	V	

E General information:

I_{R1} and I_{sat1} related to L_1
It is recommended that the temperature of the part does not exceed 125°C under worst case operating conditions.

- Ambient temperature: -40°C to +85°C (refering to I_R)
- Operating temperature: -40°C to +125°C
- Storage temperature (on tape & reel): -20°C to +40°C; 75% RH max.
- Test conditions of Electrical Properties: 20°C, 33% RH if not specified differently

REV	DATE	BY	CHECKED
1.4	2013-04-29	SSt	SSt
1.3	2012-12-05	SSt	SSt
1.2	2012-11-16	SSt	SvS
1.1	2012-08-24	SSt	SvS
1.0	2012-08-07	SSt	SvS

Projection

Würth Elektronik eiSos GmbH & Co. KG
EMC & Inductive Solutions
Max-Eyth-Str. 1
74638 Waldenburg
Germany
Tel. +49 (0) 79 42 945 - 0
www.we-online.com
eiSos@we-online.com

DESCRIPTION

WE-EHPI Energy Harvesting Coupled Inductor

Order.- No.

74488540070

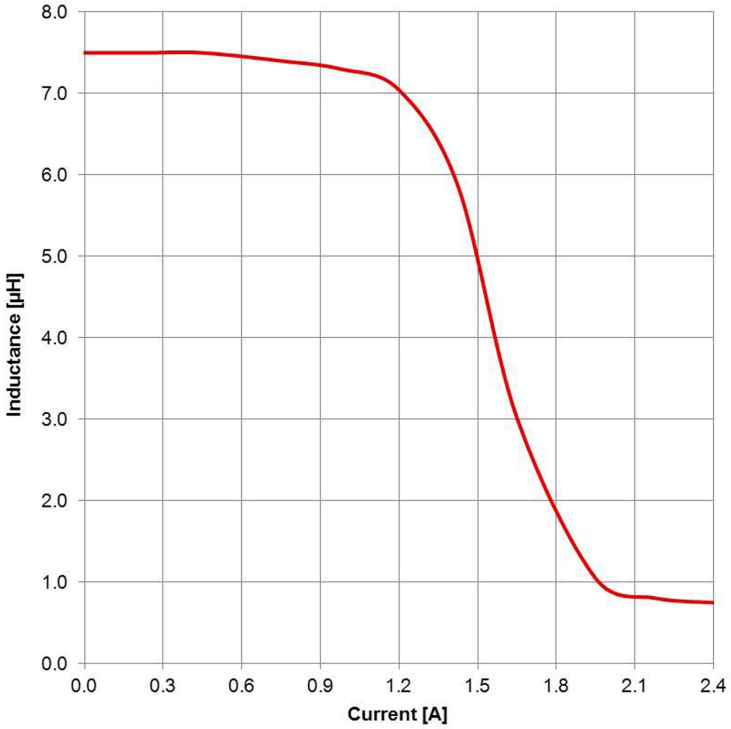
COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE

A4

Size: 5838

F Typical Inductance vs. Current Characteristics:



REV	DATE	BY	CHECKED
1.4	2013-04-29	SSt	SSt
1.3	2012-12-05	SSt	SSt
1.2	2012-11-16	SSt	SvS
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Order.- No.

74488540070

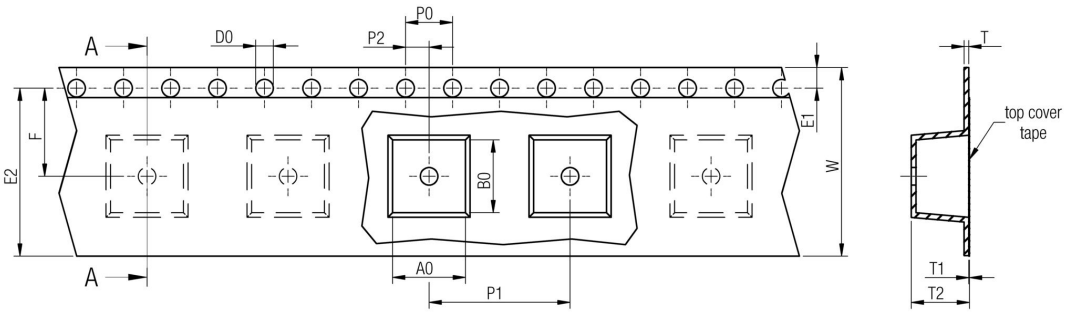
COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE

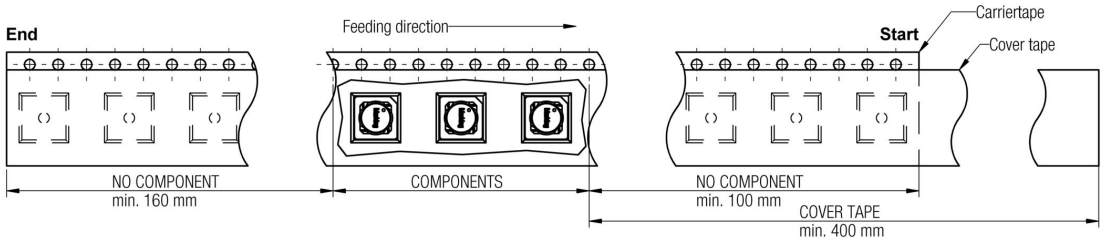
A4

Size: 5838

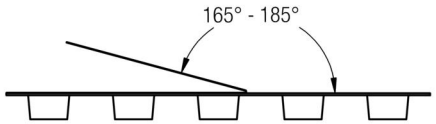
G Packaging Specification - Tape and Reel [mm]:



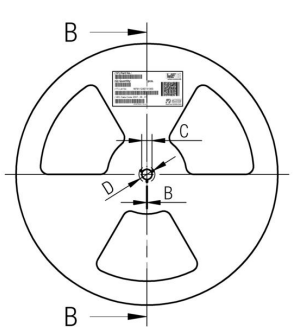
		A0	B0	W	P1	T	T1	T2	D0	E1	E2	F	P0	P2	Tape	VPE / packaging unit
tolerance		typ.	typ.	+0,3 -0,1	± 0,1	± 0,1	max.	typ.	+0,1 -0,0	± 0,1	min.	± 0,05	± 0,1	± 0,05		
size	5838	6,20	6,20	16,00	12,00	0,40	0,10	4,80	1,50	1,75	14,25	7,50	4,00	2,00	Polystyrene	1000

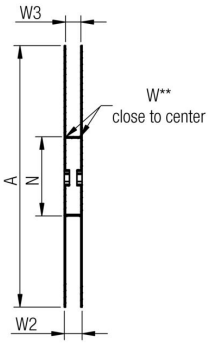


Packaging is referred to the international standard IEC 60286 -3:2007

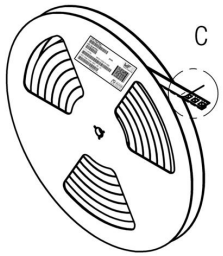


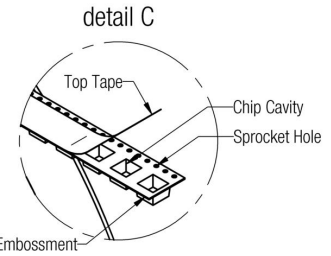
		Pull-of force
Tape width	16 mm	0,1 N - 1,3 N





		A	B	C	D	N	W1	W2	W3	W3
tolerance		± 2,0	min.	± 0,8	min.	min.	+ 1,5	max.	min.	max.
Tape width	16 mm	330,00	1,50	13,00	20,20	100,00	16,40	22,40	15,90	19,40





1.4	2013-04-29	SSt	SSt	
1.3	2012-12-05	SSt	SSt	
1.2	2012-11-16	SSt	SvS	
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REV	DATE	BY	CHECKED	

Projection

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Order.- No.

74488540070

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

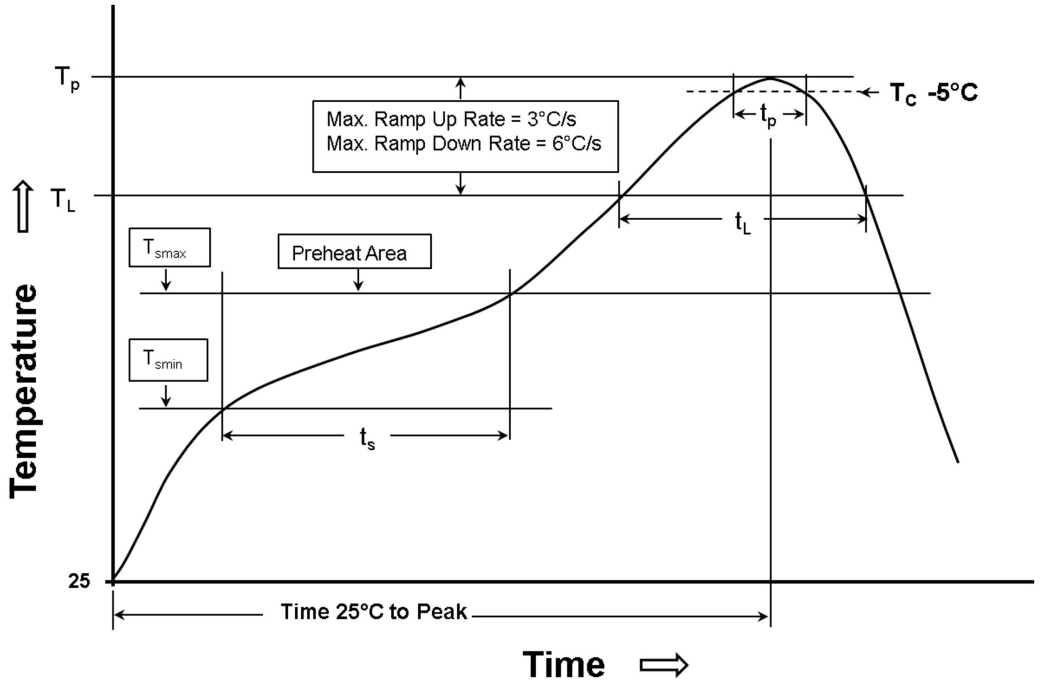
SIZE

A4

Size: 5838

H Soldering Specifications:

H1: Classification Reflow Profile for SMT components:



H2: Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat - Temperature Min (T_{smin}) - Temperature Max (T_{smax}) - Time (t_s) from (T_{smin} to T_{smax})	 150°C 200°C 60-120 seconds
Ramp-up rate (T_L to T_P)	3°C/ second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217°C 60-150 seconds
Peak package body temperature (T_p)	See Table H3
Time within 5°C of actual peak temperature (t_p)	20-30 seconds
Ramp-down rate (T_P to T_L)	6°C/ second max.
Time 25°C to peak temperature	8 minutes max.

refer to IPC/JEDEC J-STD-020D

H3: Package Classification Reflow Temperature

	Package Thickness	Volume mm³ <350	Volume mm³ 350 - 2000	Volume mm³ >2000
PB-Free Assembly	< 1.6 mm	260°C	260°C	260°C
PB-Free Assembly	1.6 - 2.5 mm	260°C	250°C	245°C
PB-Free Assembly	≥ 2.5 mm	250°C	245°C	245°C

refer to IPC/JEDEC J-STD-020D

REV	DATE	BY	CHECKED
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Projection

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www.we-online.com
eiSos@we-online.com

DESCRIPTION

WE-EHPI Energy Harvesting Coupled Inductor

Order.- No.

74488540070

COMPLIANT RoHS&REACh WÜRTH ELEKTRONIK

SIZE

A4

Size: 5838

I Cautions and Warnings:

The following conditions apply to all goods within the product series of WE-EHPI of Würth Elektronik eiSos GmbH & Co. KG:

General:
All recommendations according to the general technical specifications of the data-sheet have to be complied with.

The disposal and operation of the product within ambient conditions which probably alloy or harm the wire isolation has to be avoided.

If the product is potted in customer applications, the potting material might shrink during and after hardening. Accordingly to this the product is exposed to the pressure of the potting material with the effect that the core, wire and termination is possibly damaged by this pressure and so the electrical as well as the mechanical characteristics are endanger to be affected. After the potting material is cured, the core, wire and termination of the product have to be checked if any reduced electrical or mechanical functions or destructions have occurred.

The responsibility for the applicability of customer specific products and use in a particular customer design is always within the authority of the customer. All technical specifications for standard products do also apply for customer specific products.

Cleaning agents that are used to clean application might damage or change the characteristics of the component, body, pins or termination.

Direct mechanical impact to the product shall be prevented as the iron powder material of the core could flake or in the worst case it could break.

Product specific:
Follow all instructions mentioned in the datasheet, especially:

- The solder profile has to be complied with according to the technical reflow soldering specification, otherwise no warranty will be sustained.
- All products shall be used before the end of the period of 12 months based on the product date-code, if not a 100% solderability can´t be warranted.
- Violation of the technical product specifications such as exceeding the nominal rated current will result in the loss of warranty.

REV	DATE	BY	CHECKED
1.4	2013-04-29	SSt	SSt
1.3	2012-12-05	SSt	SSt
1.2	2012-11-16	SSt	SvS
1.1	2012-08-24	SSt	SvS
1.0	2012-08-07	SSt	SvS

Projection

Würth Elektronik eiSos GmbH & Co. KG
EMC & Inductive Solutions
Max-Eyth-Str. 1
74638 Waldenburg
Germany
Tel. +49 (0) 79 42 945 - 0
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J Important Notes:

The following conditions apply to all goods within the product range of Würth Elektronik eiSos GmbH & Co. KG:

1. General Customer Responsibility
Some goods within the product range of Würth Elektronik eiSos GmbH & Co. KG contain statements regarding general suitability for certain application areas. These statements about suitability are based on our knowledge and experience of typical requirements concerning the areas, serve as general guidance and cannot be estimated as binding statements about the suitability for a customer application. The responsibility for the applicability and use in a particular customer design is always solely within the authority of the customer. Due to this fact it is up to the customer to evaluate, where appropriate to investigate and decide whether the device with the specific product characteristics described in the product specification is valid and suitable for the respective customer application or not.

2. Customer Responsibility related to Specific, in particular Safety-Relevant Applications
It has to be clearly pointed out that the possibility of a malfunction of electronic components or failure before the end of the usual lifetime cannot be completely eliminated in the current state of the art, even if the products are operated within the range of the specifications.

In certain customer applications requiring a very high level of safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health it must be ensured by most advanced technological aid of suitable design of the customer application that no injury or damage is caused to third parties in the event of malfunction or failure of an electronic component.

Therefore, customer is cautioned to verify that data sheets are current before placing orders. The current data sheets can be downloaded at www.we-online.com.

3. Best Care and Attention
Any product-specific notes, cautions and warnings must be strictly observed. Any disregard will result in the loss of warranty.

4. Customer Support for Product Specifications
Some products within the product range may contain substances which are subject to restrictions in certain jurisdictions in order to serve specific technical requirements. Necessary information is available on request. In this case the field sales engineer or the internal sales person in charge should be contacted who will be happy to support in this matter.

5. Product R&D
Due to constant product improvement product specifications may change from time to time. As a standard reporting procedure of the Product Change Notification (PCN) according to the JEDEC-Standard inform about minor and major changes. In case of further queries regarding the PCN, the field sales engineer or the internal sales person in charge should be contacted. The basic responsibility of the customer as per Section 1 and 2 remains unaffected.

6. Product Life Cycle
Due to technical progress and economical evaluation we also reserve the right to discontinue production and delivery of products. As a standard reporting procedure of the Product Termination Notification (PTN) according to the JEDEC-Standard we will inform at an early stage about inevitable product discontinuance. According to this we cannot guarantee that all products within our product range will always be available. Therefore it needs to be verified with the field sales engineer or the internal sales person in charge about the current product availability expectancy before or when the product for application design-in disposal is considered.
The approach named above does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.

7. Property Rights
All the rights for contractual products produced by Würth Elektronik eiSos GmbH & Co. KG on the basis of ideas, development contracts as well as models or templates that are subject to copyright, patent or commercial protection supplied to the customer will remain with Würth Elektronik eiSos GmbH & Co. KG.

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8. General Terms and Conditions
Unless otherwise agreed in individual contracts, all orders are subject to the current version of the “General Terms and Conditions of Würth Elektronik eiSos Group”, last version available at www.we-online.com.

REV	DATE	BY	CHECKED
1.4	2013-04-29	SSt	SSt
1.3	2012-12-05	SSt	SSt
1.2	2012-11-16	SSt	SvS
1.1	2012-08-24	SSt	SvS
1.0	2012-08-07	SSt	SvS

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SIZE

A4

Size: 5838

MIXED SIGNAL MICROCONTROLLER

FEATURES

- Low Supply-Voltage Range: 1.8 V to 3.6 V
- Ultra-Low Power Consumption
  - Active Mode: 230 μA at 1 MHz, 2.2 V
  - Standby Mode: 0.5 μA
  - Off Mode (RAM Retention): 0.1 μA
- Five Power-Saving Modes
- Ultra-Fast Wake-Up From Standby Mode in Less Than 1 μs
- 16-Bit RISC Architecture, 62.5-ns Instruction Cycle Time
- Basic Clock Module Configurations
  - Internal Frequencies up to 16 MHz With Four Calibrated Frequency
  - Internal Very-Low-Power Low-Frequency (LF) Oscillator
  - 32-kHz Crystal
  - External Digital Clock Source
- Two 16-Bit Timer_A With Three Capture/Compare Registers
- Up to 24 Capacitive-Touch Enabled I/O Pins
- Universal Serial Communication Interface (USCI)
  - Enhanced UART Supporting Auto Baudrate Detection (LIN)
  - IrDA Encoder and Decoder
  - Synchronous SPI
  - I^2C™
- On-Chip Comparator for Analog Signal Compare Function or Slope Analog-to-Digital (A/D) Conversion
- 10-Bit 200-ksps Analog-to-Digital (A/D) Converter With Internal Reference, Sample-and-Hold, and Autoscan (See Table 1)
- Brownout Detector
- Serial Onboard Programming, No External Programming Voltage Needed, Programmable Code Protection by Security Fuse
- On-Chip Emulation Logic With Spy-Bi-Wire Interface
- Family Members are Summarized in Table 1
- Package Options
  - TSSOP: 20 Pin, 28 Pin
  - PDIP: 20 Pin
  - QFN: 32 Pin
- For Complete Module Descriptions, See the *MSP430x2xx Family User's Guide* (SLAU144)

DESCRIPTION

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μs.

The MSP430G2x13 and MSP430G2x53 series are ultra-low-power mixed signal microcontrollers with built-in 16-bit timers, up to 24 I/O capacitive-touch enabled pins, a versatile analog comparator, and built-in communication capability using the universal serial communication interface. In addition the MSP430G2x53 family members have a 10-bit analog-to-digital (A/D) converter. For configuration details see Table 1.

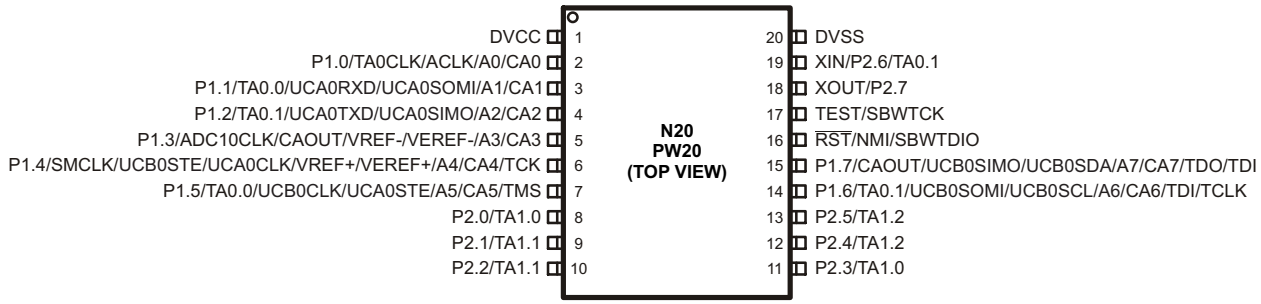
Typical applications include low-cost sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system.

Table 1. Available Options[1][2]

Device	BSL	EEM	Flash (KB)	RAM (B)	Timer_A	COMP_A+ Channel	ADC10 Channel	USCI_A0, USCI_B0	Clock	I/O	Package Type
MSP430G2553IRHB32	1	1	16	512	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2553IPW28										24	28-TSSOP
MSP430G2553IPW20										16	20-TSSOP
MSP430G2553IN20										16	20-PDIP
MSP430G2453IRHB32	1	1	8	512	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2453IPW28										24	28-TSSOP
MSP430G2453IPW20										16	20-TSSOP
MSP430G2453IN20										16	20-PDIP
MSP430G2353IRHB32	1	1	4	256	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2353IPW28										24	28-TSSOP
MSP430G2353IPW20										16	20-TSSOP
MSP430G2353IN20										16	20-PDIP
MSP430G2253IRHB32	1	1	2	256	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2253IPW28										24	28-TSSOP
MSP430G2253IPW20										16	20-TSSOP
MSP430G2253IN20										16	20-PDIP
MSP430G2153IRHB32	1	1	1	256	2x TA3	8	8	1	LF, DCO, VLO	24	32-QFN
MSP430G2153IPW28										24	28-TSSOP
MSP430G2153IPW20										16	20-TSSOP
MSP430G2153IN20										16	20-PDIP
MSP430G2513IRHB32	1	1	16	512	2x TA3	8	-	1	LF, DCO, VLO	24	32-QFN
MSP430G2513IPW28										24	28-TSSOP
MSP430G2513IPW20										16	20-TSSOP
MSP430G2513IN20										16	20-PDIP
MSP430G2413IRHB32	1	1	8	512	2x TA3	8	-	1	LF, DCO, VLO	24	32-QFN
MSP430G2413IPW28										24	28-TSSOP
MSP430G2413IPW20										16	20-TSSOP
MSP430G2413IN20										16	20-PDIP
MSP430G2313IRHB32	1	1	4	256	2x TA3	8	-	1	LF, DCO, VLO	24	32-QFN
MSP430G2313IPW28										24	28-TSSOP
MSP430G2313IPW20										16	20-TSSOP
MSP430G2313IN20										16	20-PDIP
MSP430G2213IRHB32	1	1	2	256	2x TA3	8	-	1	LF, DCO, VLO	24	32-QFN
MSP430G2213IPW28										24	28-TSSOP
MSP430G2213IPW20										16	20-TSSOP
MSP430G2213IN20										16	20-PDIP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

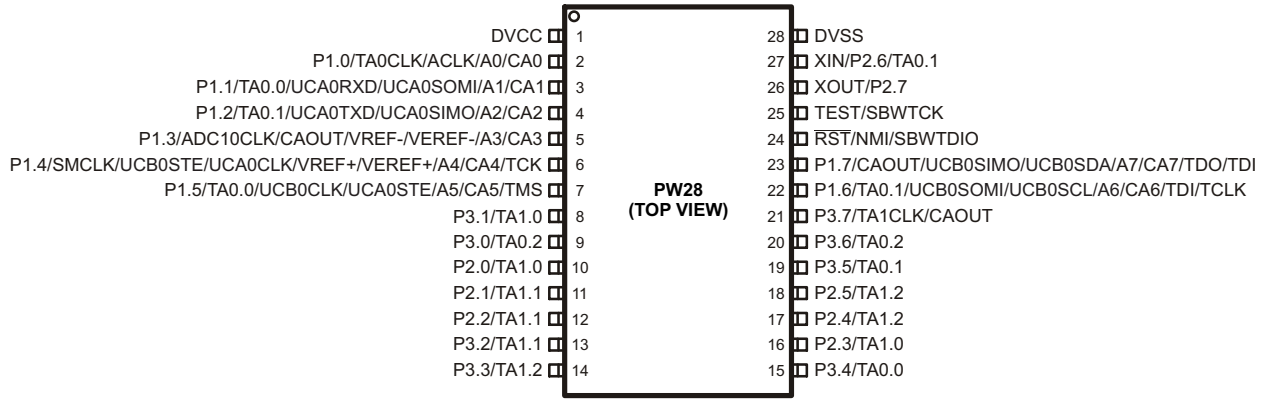
Device Pinout, MSP430G2x13 and MSP430G2x53, 20-Pin Devices, TSSOP and PDIP



NOTE: ADC10 is available on MSP430G2x53 devices only.

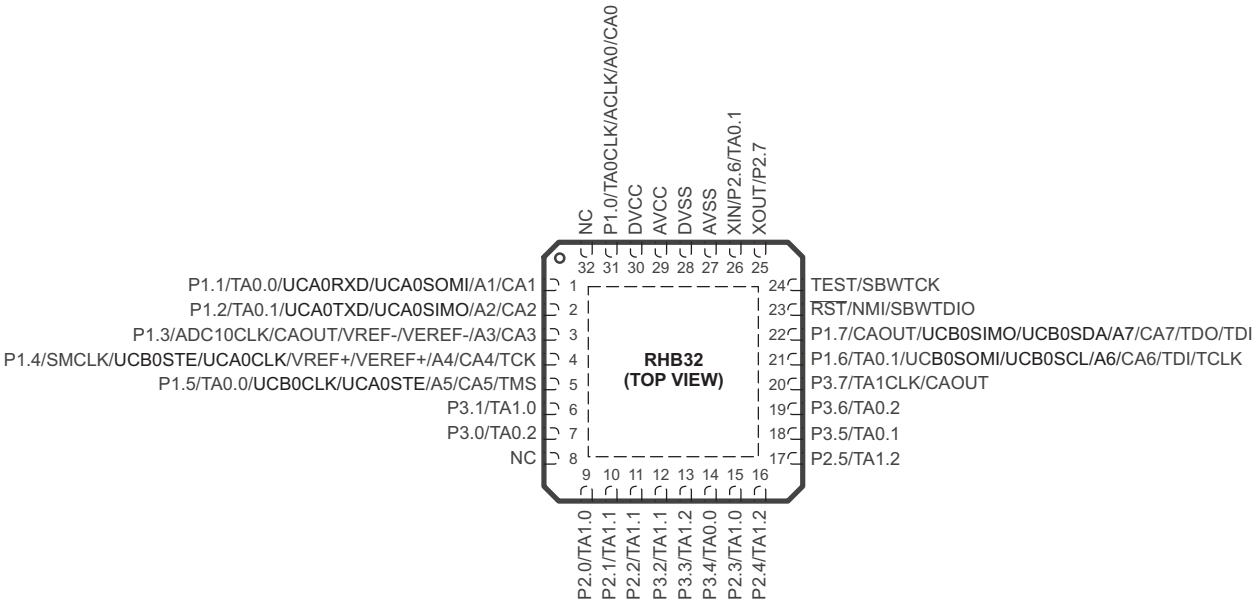
NOTE: The pulldown resistors of port P3 should be enabled by setting P3REN.x = 1.

Device Pinout, MSP430G2x13 and MSP430G2x53, 28-Pin Devices, TSSOP



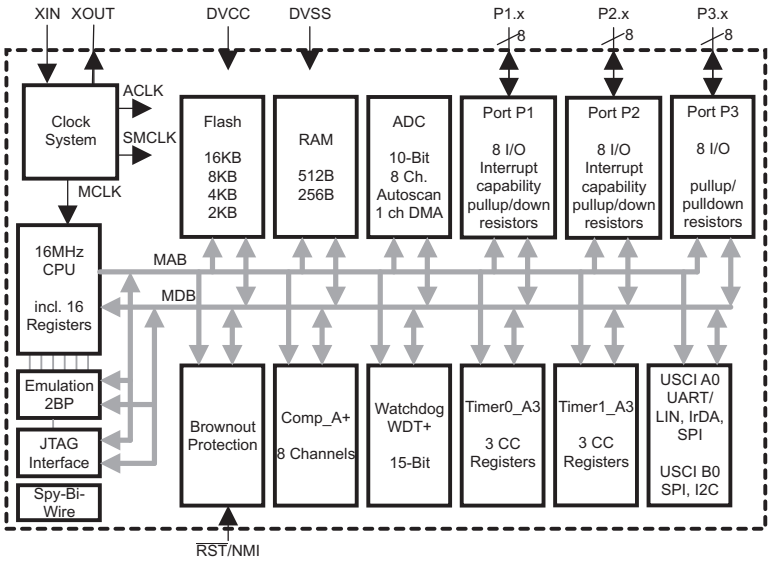
NOTE: ADC10 is available on MSP430G2x53 devices only.

Device Pinout, MSP430G2x13 and MSP430G2x53, 32-Pin Devices, QFN



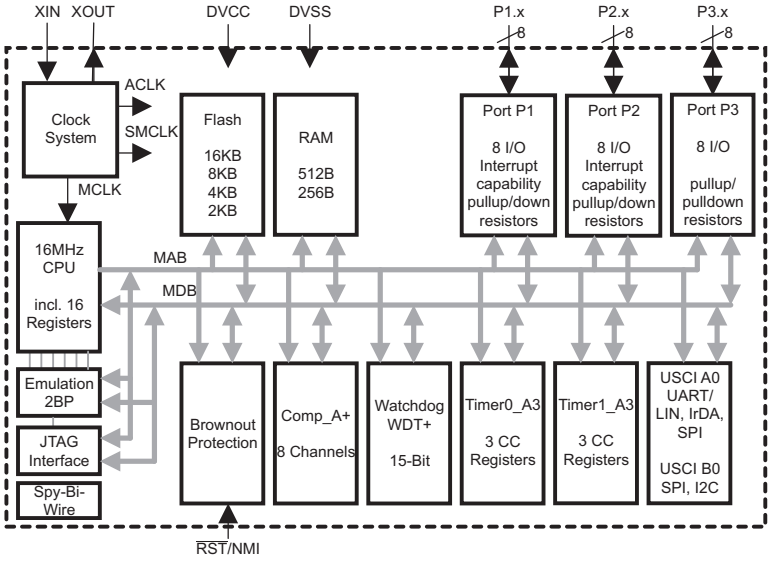
NOTE: ADC10 is available on MSP430G2x53 devices only.

Functional Block Diagram, MSP430G2x53



NOTE: Port P3 is available on 28-pin and 32-pin devices only.

Functional Block Diagram, MSP430G2x13



NOTE: Port P3 is available on 28-pin and 32-pin devices only.

Table 2. Terminal Functions

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PW20, N20	PW28	RHB32		
P1.0/	2	2	31	I/O	General-purpose digital I/O pin
TA0CLK/					Timer0_A, clock signal TACLK input
ACLK/					ACLK signal output
A0					ADC10 analog input A0 (1)
CA0					Comparator_A+, CA0 input
P1.1/	3	3	1	I/O	General-purpose digital I/O pin
TA0.0/					Timer0_A, capture: CCI0A input, compare: Out0 output / BSL transmit
UCA0RXD/					USCI_A0 UART mode: receive data input
UCA0SOMI/					USCI_A0 SPI mode: slave data out/master in
A1/					ADC10 analog input A1 (1)
CA1					Comparator_A+, CA1 input
P1.2/	4	4	2	I/O	General-purpose digital I/O pin
TA0.1/					Timer0_A, capture: CCI1A input, compare: Out1 output
UCA0TXD/					USCI_A0 UART mode: transmit data output
UCA0SIMO/					USCI_A0 SPI mode: slave data in/master out
A2/					ADC10 analog input A2 (1)
CA2					Comparator_A+, CA2 input
P1.3/	5	5	3	I/O	General-purpose digital I/O pin
ADC10CLK/					ADC10, conversion clock output (1)
A3/					ADC10 analog input A3 (1)
VREF-/VEREF-/					ADC10 negative reference voltage (1)
CA3/					Comparator_A+, CA3 input
CAOUT					Comparator_A+, output
P1.4/	6	6	4	I/O	General-purpose digital I/O pin
SMCLK/					SMCLK signal output
UCB0STE/					USCI_B0 slave transmit enable
UCA0CLK/					USCI_A0 clock input/output
A4/					ADC10 analog input A4 (1)
VREF+/VEREF+/					ADC10 positive reference voltage (1)
CA4/					Comparator_A+, CA4 input
TCK					JTAG test clock, input terminal for device programming and test
P1.5/	7	7	5	I/O	General-purpose digital I/O pin
TA0.0/					Timer0_A, compare: Out0 output / BSL receive
UCB0CLK/					USCI_B0 clock input/output
UCA0STE/					USCI_A0 slave transmit enable
A5/					ADC10 analog input A5 (1)
CA5/					Comparator_A+, CA5 input
TMS					JTAG test mode select, input terminal for device programming and test

(1) MSP430G2x53 devices only

Table 2. Terminal Functions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PW20, N20	PW28	RHB32		
P1.6/ TA0.1/ A6/ CA6/ UCB0SOMI/ UCB0SCL/ TDI/TCLK	14	22	21	I/O	General-purpose digital I/O pin Timer0_A, compare: Out1 output ADC10 analog input A6(1) Comparator_A+, CA6 input USCI_B0 SPI mode: slave out master in USCI_B0 I2C mode: SCL I2C clock JTAG test data input or test clock input during programming and test
P1.7/ A7/ CA7/ CAOUT/ UCB0SIMO/ UCB0SDA/ TDO/TDI	15	23	22	I/O	General-purpose digital I/O pin ADC10 analog input A7(1) Comparator_A+, CA7 input Comparator_A+, output USCI_B0 SPI mode: slave in master out USCI_B0 I2C mode: SDA I2C data JTAG test data output terminal or test data input during programming and test(2)
P2.0/ TA1.0	8	10	9	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI0A input, compare: Out0 output
P2.1/ TA1.1	9	11	10	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI1A input, compare: Out1 output
P2.2/ TA1.1	10	12	11	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI1B input, compare: Out1 output
P2.3/ TA1.0	11	16	15	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI0B input, compare: Out0 output
P2.4/ TA1.2	12	17	16	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI2A input, compare: Out2 output
P2.5/ TA1.2	13	18	17	I/O	General-purpose digital I/O pin Timer1_A, capture: CCI2B input, compare: Out2 output
XIN/ P2.6/ TA0.1	19	27	26	I/O	Input terminal of crystal oscillator General-purpose digital I/O pin Timer0_A, compare: Out1 output
XOUT/ P2.7	18	26	25	I/O	Output terminal of crystal oscillator(3) General-purpose digital I/O pin
P3.0/ TA0.2	-	9	7	I/O	General-purpose digital I/O pin Timer0_A, capture: CCI2A input, compare: Out2 output
P3.1/ TA1.0	-	8	6	I/O	General-purpose digital I/O pin Timer1_A, compare: Out0 output
P3.2/ TA1.1	-	13	12	I/O	General-purpose digital I/O pin Timer1_A, compare: Out1 output
P3.3/ TA1.2	-	14	13	I/O	General-purpose digital I/O Timer1_A, compare: Out2 output
P3.4/ TA0.0	-	15	14	I/O	General-purpose digital I/O Timer0_A, compare: Out0 output

(2) TDO or TDI is selected via JTAG instruction.
(3) If XOUT/P2.7 is used as an input, excess current flows until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

Table 2. Terminal Functions (continued)

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	PW20, N20	PW28	RHB32		
P3.5/ TA0.1	-	19	18	I/O	General-purpose digital I/O Timer0_A, compare: Out1 output
P3.6/ TA0.2	-	20	19	I/O	General-purpose digital I/O Timer0_A, compare: Out2 output
P3.7/ TA1CLK/ CAOUT	-	21	20	I/O	General-purpose digital I/O Timer1_A, clock signal TACLK input Comparator_A+, output
$\overline{\text{RST}}$/ NMI/ SBWTDIO	16	24	23	I	Reset Nonmaskable interrupt input Spy-Bi-Wire test data input/output during programming and test
TEST/ SBWTCK	17	25	24	I	Selects test mode for JTAG pins on Port 1. The device protection fuse is connected to TEST. Spy-Bi-Wire test clock input during programming and test
AVCC	NA	NA	29	NA	Analog supply voltage
DVCC	1	1	30	NA	Digital supply voltage
DVSS	20	28	27, 28	NA	Ground reference
NC	NA	NA	8, 32	NA	Not connected
QFN Pad	NA	NA	Pad	NA	QFN package pad. Connection to VSS is recommended.

SHORT-FORM DESCRIPTION

CPU

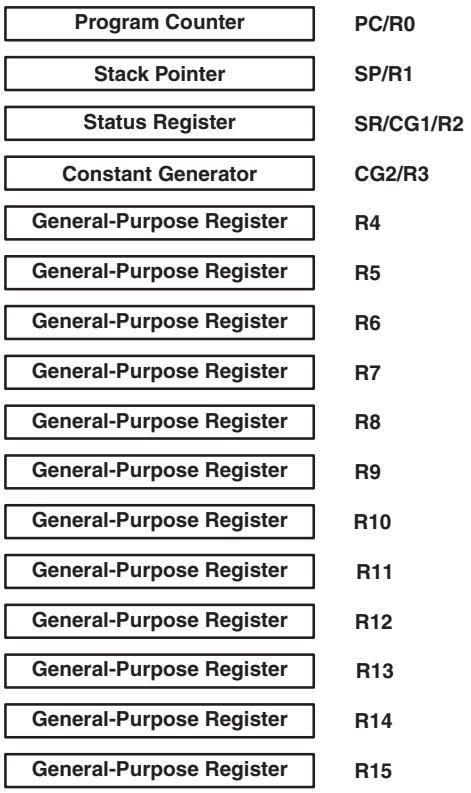
The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.



Instruction Set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 3 shows examples of the three types of instruction formats; Table 4 shows the address modes.

Table 3. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 ---> R5
Single operands, destination only	CALL R8	PC -->(TOS), R8--> PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 4. Address Mode Descriptions(1)

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs,Rd	MOV R10,R11	R10 -- --> R11
Indexed	✓	✓	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) -- --> M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE,TONI		M(EDE) -- --> M(TONI)
Absolute	✓	✓	MOV &MEM,&TCDAT		M(MEM) -- --> M(TCDAT)
Indirect	✓		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) -- --> M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) -- --> R11 R10 + 2-- --> R10
Immediate	✓		MOV #X,TONI	MOV #45,TONI	#45 -- --> M(TONI)

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - DCO's dc generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped

Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are located in the address range 0FFFFh to 0FFC0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (for example, flash is not programmed), the CPU goes into LPM4 immediately after power-up.

Table 5. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-Up External Reset Watchdog Timer+ Flash key violation PC out-of-range(1)	PORIFG RSTIFG WDTIFG KEYV(2)	Reset	0FFFEh	31, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(2)(3)	(non)-maskable (non)-maskable (non)-maskable	0FFFCh	30
Timer1_A3	TA1CCR0 CCIFG(4)	maskable	0FFFAh	29
Timer1_A3	TA1CCR2 TA1CCR1 CCIFG, TAIFG(2)(4)	maskable	0FFF8h	28
Comparator_A+	CAIFG(4)	maskable	0FFF6h	27
Watchdog Timer+	WDTIFG	maskable	0FFF4h	26
Timer0_A3	TA0CCR0 CCIFG(4)	maskable	0FFF2h	25
Timer0_A3	TA0CCR2 TA0CCR1 CCIFG, TAIFG (5)(4)	maskable	0FFF0h	24
USCI_A0/USCI_B0 receive USCI_B0 I2C status	UCA0RXIFG, UCB0RXIFG(2)(5)	maskable	0FFEEh	23
USCI_A0/USCI_B0 transmit USCI_B0 I2C receive/transmit	UCA0TXIFG, UCB0TXIFG(2)(6)	maskable	0FFECh	22
ADC10 (MSP430G2x53 only)	ADC10IFG(4)	maskable	0FFEAh	21
			0FFE8h	20
I/O Port P2 (up to eight flags)	P2IFG.0 to P2IFG.7(2)(4)	maskable	0FFE6h	19
I/O Port P1 (up to eight flags)	P1IFG.0 to P1IFG.7(2)(4)	maskable	0FFE4h	18
			0FFE2h	17
			0FFE0h	16
See (7)			0FFDEh	15
See (8)			0FFDEh to 0FFC0h	14 to 0, lowest

(1) A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h to 01FFh) or from within unused address ranges.
(2) Multiple source flags
(3) (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot.
(4) Interrupt flags are located in the module.
(5) In SPI mode: UCB0RXIFG. In I2C mode: UCALIFG, UCNACKIFG, ICSTTIFG, UCSTPIFG.
(6) In UART or SPI mode: UCB0TXIFG. In I2C mode: UCB0RXIFG, UCB0TXIFG.
(7) This location is used as bootstrap loader security key (BSLSKEY). A 0xAA55 at this location disables the BSL completely. A zero (0h) disables the erasure of the flash if an invalid password is supplied.
(8) The interrupt vectors at addresses 0FFDEh to 0FFC0h are not used in this device and can be used for regular program code if necessary.

Special Function Registers (SFRs)

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

Legend		
	rw:	Bit can be read and written.
	rw-0,1:	Bit can be read and written. It is reset or set by PUC.
	rw-(0,1):	Bit can be read and written. It is reset or set by POR.
		SFR bit is not present in device.

Table 6. Interrupt Enable Register 1 and 2

Address	7	6	5	4	3	2	1	0
00h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE Oscillator fault interrupt enable
NMIIE (Non)maskable interrupt enable
ACCVIE Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h					UCB0TXIE	UCB0RXIE	UCA0TXIE	UCA0RXIE
					rw-0	rw-0	rw-0	rw-0

UCA0RXIE USCI_A0 receive interrupt enable
UCA0TXIE USCI_A0 transmit interrupt enable
UCB0RXIE USCI_B0 receive interrupt enable
UCB0TXIE USCI_B0 transmit interrupt enable

Table 7. Interrupt Flag Register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG Set on watchdog timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-on or a reset condition at the $\overline{RST}$/NMI pin in reset mode.
OFIFG Flag set on oscillator fault.
PORIFG Power-On Reset interrupt flag. Set on V_{CC} power-up.
RSTIFG External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power-up.
NMIIFG Set via $\overline{RST}$/NMI pin

Address	7	6	5	4	3	2	1	0
03h					UCB0TXIFG	UCB0RXIFG	UCA0TXIFG	UCA0RXIFG
					rw-1	rw-0	rw-1	rw-0

UCA0RXIFG USCI_A0 receive interrupt flag
UCA0TXIFG USCI_A0 transmit interrupt flag
UCB0RXIFG USCI_B0 receive interrupt flag
UCB0TXIFG USCI_B0 transmit interrupt flag

Memory Organization

Table 8. Memory Organization

		MSP430G2153	MSP430G2253 MSP430G2213	MSP430G2353 MSP430G2313	MSP430G2453 MSP430G2413	MSP430G2553 MSP430G2513
Memory	Size	1kB	2kB	4kB	8kB	16kB
Main: interrupt vector	Flash	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0	0xFFFF to 0xFFC0
Main: code memory	Flash	0xFFFF to 0xFC00	0xFFFF to 0xF800	0xFFFF to 0xF000	0xFFFF to 0xE000	0xFFFF to 0xC000
Information memory	Size	256 Byte	256 Byte	256 Byte	256 Byte	256 Byte
	Flash	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h
RAM	Size	256 Byte	256 Byte	256 Byte	512 Byte	512 Byte
		0x02FF to 0x0200	0x02FF to 0x0200	0x02FF to 0x0200	0x03FF to 0x0200	0x03FF to 0x0200
Peripherals	16-bit	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h
	8-bit	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h
	8-bit SFR	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h

Bootstrap Loader (BSL)

The MSP430 BSL enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the *MSP430 Programming Via the Bootstrap Loader User's Guide* (SLAU319).

Table 9. BSL Function Pins

BSL FUNCTION	20-PIN PW PACKAGE 20-PIN N PACKAGE	28-PIN PACKAGE PW	32-PIN PACKAGE RHB
Data transmit	3 - P1.1	3 - P1.1	1 - P1.1
Data receive	7 - P1.5	7 - P1.5	5 - P1.5

Flash Memory

The flash memory can be programmed via the Spy-Bi-Wire/JTAG port or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A contains calibration data. After reset segment A is protected against programming and erasing. It can be unlocked but care should be taken not to erase this segment if the device-specific calibration data is required.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x2xx Family User's Guide* (SLAU144).

Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator and an internal digitally controlled oscillator (DCO). The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 μs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced either from a 32768-Hz watch crystal or the internal LF oscillator.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

The DCO settings to calibrate the DCO output frequency are stored in the information memory segment A.

Main DCO Characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

Calibration Data Stored in Information Memory Segment A

Calibration data is stored for both the DCO and for ADC10 organized in a tag-length-value structure.

Table 10. Tags Used by the ADC Calibration Tags

NAME	ADDRESS	VALUE	DESCRIPTION
TAG_DCO_30	0x10F6	0x01	DCO frequency calibration at V_{CC} = 3 V and T_A = 30°C at calibration
TAG_ADC10_1	0x10DA	0x10	ADC10_1 calibration tag
TAG_EMPTY	-	0xFE	Identifier for empty memory areas

Table 11. Labels Used by the ADC Calibration Tags

LABEL	ADDRESS OFFSET	SIZE	CONDITION AT CALIBRATION AND DESCRIPTION
CAL_ADC_25T85	0x0010	word	INCHx = 0x1010, REF2_5 = 1, T_A = 85°C
CAL_ADC_25T30	0x000E	word	INCHx = 0x1010, REF2_5 = 1, T_A = 30°C
CAL_ADC_25VREF_FACTOR	0x000C	word	REF2_5 = 1, T_A = 30°C, I_{VREF+} = 1 mA
CAL_ADC_15T85	0x000A	word	INCHx = 0x1010, REF2_5 = 0, T_A = 85°C
CAL_ADC_15T30	0x0008	word	INCHx = 0x1010, REF2_5 = 0, T_A = 30°C
CAL_ADC_15VREF_FACTOR	0x0006	word	REF2_5 = 0, T_A = 30°C, I_{VREF+} = 0.5 mA
CAL_ADC_OFFSET	0x0004	word	External VREF = 1.5 V, $f_{ADC10CLK}$ = 5 MHz
CAL_ADC_GAIN_FACTOR	0x0002	word	External VREF = 1.5 V, $f_{ADC10CLK}$ = 5 MHz
CAL_BC1_1MHZ	0x0009	byte	-
CAL_DCO_1MHZ	0x0008	byte	-
CAL_BC1_8MHZ	0x0007	byte	-
CAL_DCO_8MHZ	0x0006	byte	-
CAL_BC1_12MHZ	0x0005	byte	-
CAL_DCO_12MHZ	0x0004	byte	-
CAL_BC1_16MHZ	0x0003	byte	-
CAL_DCO_16MHZ	0x0002	byte	-

Brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

Digital I/O

Up to three 8-bit I/O ports are implemented:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt condition (port P1 and port P2 only) is possible.
- Edge-selectable interrupt input capability for all bits of port P1 and port P2 (if available).
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pullup or pulldown resistor.
- Each I/O has an individually programmable pin oscillator enable bit to enable low-cost capacitive touch detection.

Watchdog Timer (WDT+)

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be disabled or configured as an interval timer and can generate interrupts at selected time intervals.

Timer_A3 (TA0, TA1)

Timer0/1_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 12. Timer0_A3 Signal Connections

INPUT PIN NUMBER			DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER		
PW20, N20	PW28	RHB32					PW20, N20	PW28	RHB32
P1.0-2	P1.0-2	P1.0-31	TACLK	TACLK	Timer	NA			
			ACLK	ACLK					
			SMCLK	SMCLK					
PinOsc	PinOsc	PinOsc	TACLK	INCLK					
P1.1-3	P1.1-3	P1.1-1	TA0.0	CCI0A	CCR0	TA0	P1.1-3	P1.1-3	P1.1-1
			ACLK	CCI0B			P1.5-7	P1.5-7	P1.5-5
			V_{SS}	GND				P3.4-15	P3.4-14
			V_{CC}	V_{CC}					
P1.2-4	P1.2-4	P1.2-2	TA0.1	CCI1A	CCR1	TA1	P1.2-4	P1.2-4	P1.2-2
			CAOUT	CCI1B			P1.6-14	P1.6-22	P1.6-21
			V_{SS}	GND			P2.6-19	P2.6-27	P2.6-26
			V_{CC}	V_{CC}				P3.5-19	P3.5-18
	P3.0-9	P3.0-7	TA0.2	CCI2A	CCR2	TA2		P3.0-9	P3.0-7
PinOsc	PinOsc	PinOsc	TA0.2	CCI2B				P3.6-20	P3.6-19
			V_{SS}	GND					
			V_{CC}	V_{CC}					

Table 13. Timer1_A3 Signal Connections

INPUT PIN NUMBER			DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER		
PW20, N20	PW28	RHB32					PW20, N20	PW28	RHB32
-	P3.7-21	P3.7-20	TACLK	TACLK	Timer	NA			
			ACLK	ACLK					
			SMCLK	SMCLK					
-	P3.7-21	P3.7-20	TACLK	INCLK					
P2.0-8	P2.0-10	P2.0-9	TA1.0	CCI0A	CCR0	TA0	P2.0-8	P2.0-10	P2.0-9
P2.3-11	P2.3-16	P2.3-12	TA1.0	CCI0B			P2.3-11	P2.3-16	P2.3-15
			V_{SS}	GND				P3.1-8	P3.1-6
			V_{CC}	V_{CC}					
P2.1-9	P2.1-11	P2.1-10	TA1.1	CCI1A	CCR1	TA1	P2.1-9	P2.1-11	P2.1-10
P2.2-10	P2.2-12	P2.2-11	TA1.1	CCI1B			P2.2-10	P2.2-12	P2.2-11
			V_{SS}	GND				P3.2-13	P3.2-12
			V_{CC}	V_{CC}					
P2.4-12	P2.4-17	P2.4-16	TA1.2	CCI2A	CCR2	TA2	P2.4-12	P2.4-17	P2.4-16
P2.5-13	P2.5-18	P2.5-17	TA1.2	CCI2B			P2.5-13	P2.5-18	P2.5-17
			V_{SS}	GND				P3.3-14	P3.3-13
			V_{CC}	V_{CC}					

Universal Serial Communications Interface (USCI)

The USCI module is used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection (LIN), and IrDA. Not all packages support the USCI functionality.

USCI_A0 provides support for SPI (3 or 4 pin), UART, enhanced UART, and IrDA.

USCI_B0 provides support for SPI (3 or 4 pin) and I2C.

Comparator_A+

The primary function of the comparator_A+ module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

ADC10 (MSP430G2x53 Only)

The ADC10 module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and data transfer controller (DTC) for automatic conversion result handling, allowing ADC samples to be converted and stored without any CPU intervention.

Peripheral File Map

Table 14. Peripherals With Word Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
ADC10 (MSP430G2x53 devices only)	ADC data transfer start address	ADC10SA	1BCh
	ADC memory	ADC10MEM	1B4h
	ADC control register 1	ADC10CTL1	1B2h
	ADC control register 0	ADC10CTL0	1B0h
Timer1_A3	Capture/compare register	TA1CCR2	0196h
	Capture/compare register	TA1CCR1	0194h
	Capture/compare register	TA1CCR0	0192h
	Timer_A register	TA1R	0190h
	Capture/compare control	TA1CCTL2	0186h
	Capture/compare control	TA1CCTL1	0184h
	Capture/compare control	TA1CCTL0	0182h
	Timer_A control	TA1CTL	0180h
	Timer_A interrupt vector	TA1IV	011Eh
Timer0_A3	Capture/compare register	TA0CCR2	0176h
	Capture/compare register	TA0CCR1	0174h
	Capture/compare register	TA0CCR0	0172h
	Timer_A register	TA0R	0170h
	Capture/compare control	TA0CCTL2	0166h
	Capture/compare control	TA0CCTL1	0164h
	Capture/compare control	TA0CCTL0	0162h
	Timer_A control	TA0CTL	0160h
	Timer_A interrupt vector	TA0IV	012Eh
Flash Memory	Flash control 3	FCTL3	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h
Watchdog Timer+	Watchdog/timer control	WDTCTL	0120h

Table 15. Peripherals With Byte Access

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
USCI_B0	USCI_B0 transmit buffer	UCB0TXBUF	06Fh
	USCI_B0 receive buffer	UCB0RXBUF	06Eh
	USCI_B0 status	UCB0STAT	06Dh
	USCI B0 I2C Interrupt enable	UCB0CIE	06Ch
	USCI_B0 bit rate control 1	UCB0BR1	06Bh
	USCI_B0 bit rate control 0	UCB0BR0	06Ah
	USCI_B0 control 1	UCB0CTL1	069h
	USCI_B0 control 0	UCB0CTL0	068h
	USCI_B0 I2C slave address	UCB0SA	011Ah
	USCI_B0 I2C own address	UCB0OA	0118h
USCI_A0	USCI_A0 transmit buffer	UCA0TXBUF	067h
	USCI_A0 receive buffer	UCA0RXBUF	066h
	USCI_A0 status	UCA0STAT	065h
	USCI_A0 modulation control	UCA0MCTL	064h
	USCI_A0 baud rate control 1	UCA0BR1	063h
	USCI_A0 baud rate control 0	UCA0BR0	062h
	USCI_A0 control 1	UCA0CTL1	061h
	USCI_A0 control 0	UCA0CTL0	060h
	USCI_A0 IrDA receive control	UCA0IRRCTL	05Fh
	USCI_A0 IrDA transmit control	UCA0IRTCTL	05Eh
	USCI_A0 auto baud rate control	UCA0ABCTL	05Dh
ADC10 (MSP430G2x53 devices only)	ADC analog enable 0	ADC10AE0	04Ah
	ADC analog enable 1	ADC10AE1	04Bh
	ADC data transfer control register 1	ADC10DTC1	049h
	ADC data transfer control register 0	ADC10DTC0	048h
Comparator_A+	Comparator_A+ port disable	CAPD	05Bh
	Comparator_A+ control 2	CACTL2	05Ah
	Comparator_A+ control 1	CACTL1	059h
Basic Clock System+	Basic clock system control 3	BCSCTL3	053h
	Basic clock system control 2	BCSCTL2	058h
	Basic clock system control 1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P3 (28-pin PW and 32-pin RHB only)	Port P3 selection 2. pin	P3SEL2	043h
	Port P3 resistor enable	P3REN	010h
	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h
Port P2	Port P2 selection 2	P2SEL2	042h
	Port P2 resistor enable	P2REN	02Fh
	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h

Table 15. Peripherals With Byte Access (continued)

MODULE	REGISTER DESCRIPTION	REGISTER NAME	OFFSET
Port P1	Port P1 selection 2	P1SEL2	041h
	Port P1 resistor enable	P1REN	027h
	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Function	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

Absolute Maximum Ratings(1)

Voltage applied at V_{CC} to V_{SS}		–0.3 V to 4.1 V
Voltage applied to any pin(2)		–0.3 V to V_{CC} + 0.3 V
Diode current at any device pin		±2 mA
Storage temperature range, T_{stg} (3)	Unprogrammed device	–55°C to 150°C
	Programmed device	–55°C to 150°C

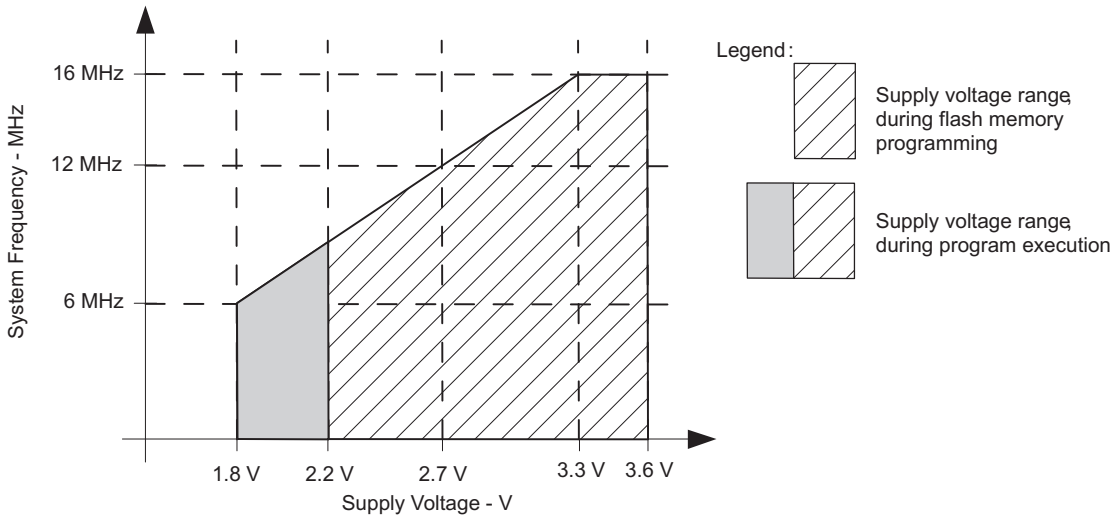
(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	During program execution	1.8		3.6	V
		During flash programming or erase	2.2		3.6	
V_{SS}	Supply voltage			0		V
T_A	Operating free-air temperature	I version	–40		85	°C
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(1)(2)	V_{CC} = 1.8 V, Duty cycle = 50% ± 10%	dc		6	MHz
		V_{CC} = 2.7 V, Duty cycle = 50% ± 10%	dc		12	
		V_{CC} = 3.3 V, Duty cycle = 50% ± 10%	dc		16	

(1) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
(2) Modules might have a different maximum input clock specification. See the specification of the respective module in this data sheet.



Note: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Safe Operating Area

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{AM,1MHz}$	Active mode (AM) current at 1 MHz	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1 MHz, f_{ACLK} = 0 Hz, Program executes in flash, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		230		μA
				3 V		330	420	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.

Typical Characteristics, Active Mode Supply Current (Into V_{CC})

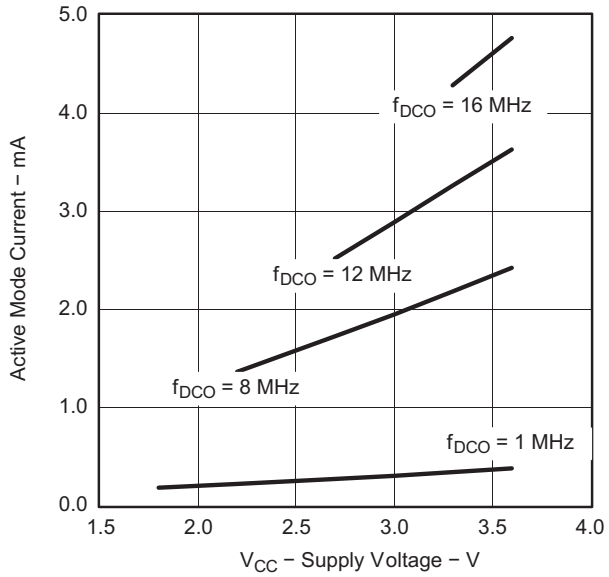


Figure 2. Active Mode Current vs V_{CC}, T_A = 25°C

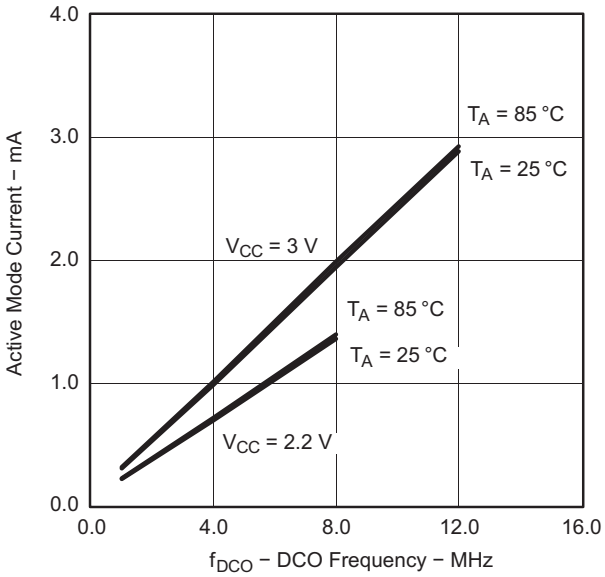


Figure 3. Active Mode Current vs DCO Frequency

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{LPM0,1MHz}$	Low-power mode 0 (LPM0) current(3)	f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0	25°C	2.2 V		56		μA
I_{LPM2}	Low-power mode 2 (LPM2) current(4)	f_{MCLK} = f_{SMCLK} = 0 MHz, f_{DCO} = 1 MHz, f_{ACLK} = 32768 Hz, BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		22		μA
$I_{LPM3,LFXT1}$	Low-power mode 3 (LPM3) current(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.7	1.5	μA
$I_{LPM3,VLO}$	Low-power mode 3 current, (LPM3)(4)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} from internal LF oscillator (VLO), CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	25°C	2.2 V		0.5	0.7	μA
I_{LPM4}	Low-power mode 4 (LPM4) current(5)	f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	25°C	2.2 V		0.1	0.5	μA
			85°C			0.8	1.7	

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance is chosen to closely match the required 9 pF.
(3) Current for brownout and WDT clocked by SMCLK included.
(4) Current for brownout and WDT clocked by ACLK included.
(5) Current for brownout included.

Typical Characteristics, Low-Power Mode Supply Currents

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

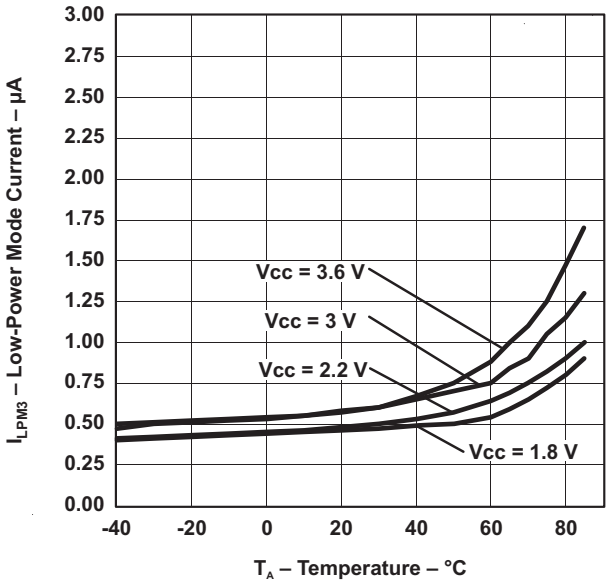


Figure 4. LPM3 Current vs Temperature

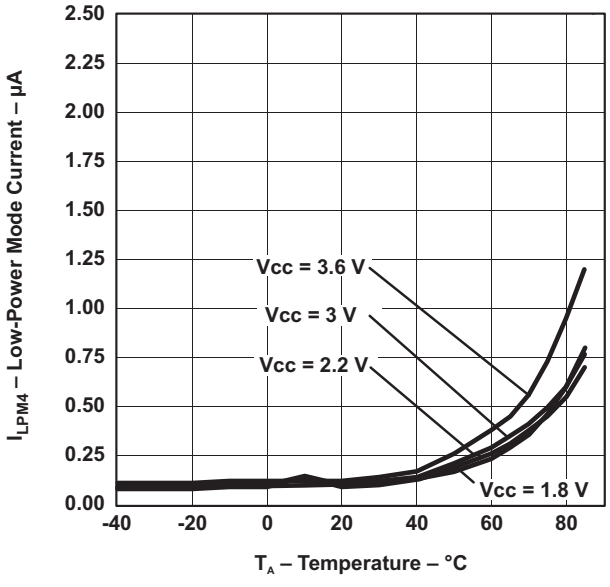


Figure 5. LPM4 Current vs Temperature

Schmitt-Trigger Inputs, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage			0.45 V_{CC}		0.75 V_{CC}	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage			0.25 V_{CC}		0.55 V_{CC}	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		3 V	0.3		1	V
R_{Pull}	Pullup/pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$	3 V	20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

Leakage Current, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	(1) (2)	3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Outputs, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –6 mA(1)	3 V		V_{CC} – 0.3		V
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 6 mA(1)	3 V		V_{SS} + 0.3		V

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

Output Frequency, Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	Px.y, C_L = 20 pF, R_L = 1 kΩ(1) (2)	3 V		12		MHz
f_{Port_CLK}	Clock output frequency	Px.y, C_L = 20 pF(2)	3 V		16		MHz

(1) A resistive divider with two 0.5-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics, Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

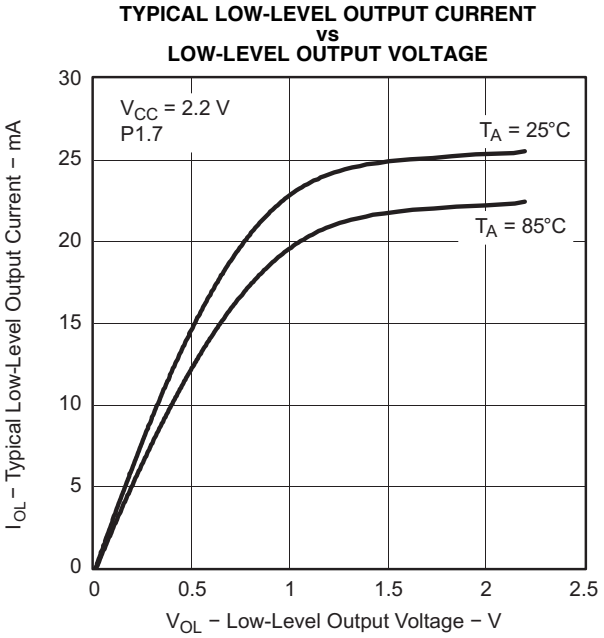


Figure 6.

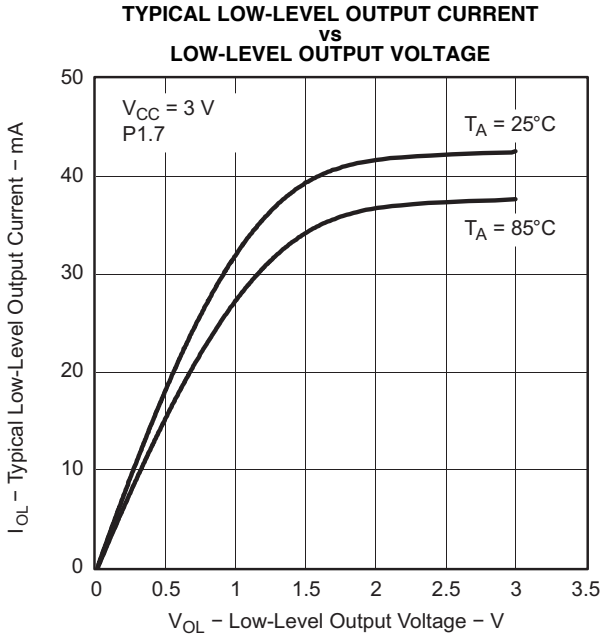


Figure 7.

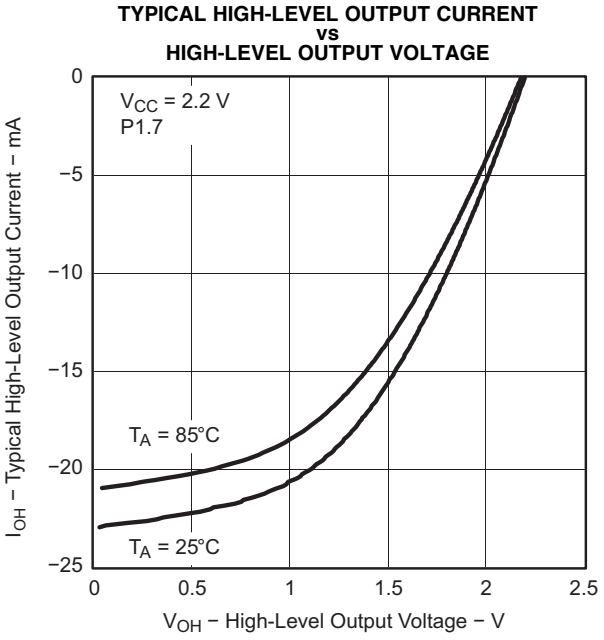


Figure 8.

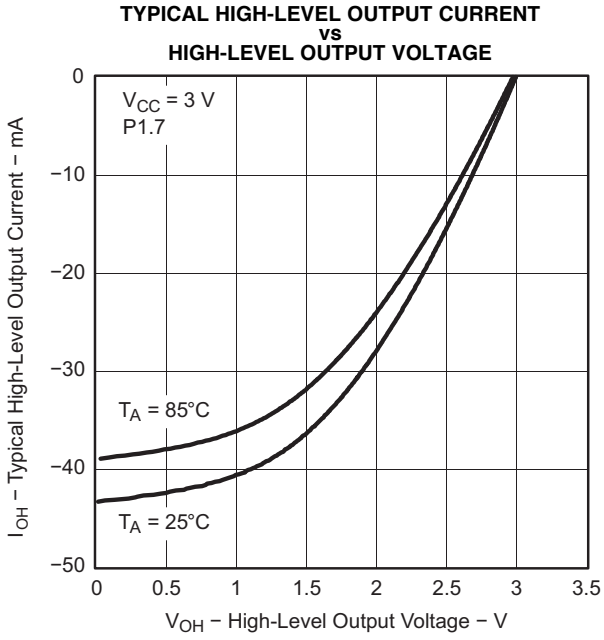


Figure 9.

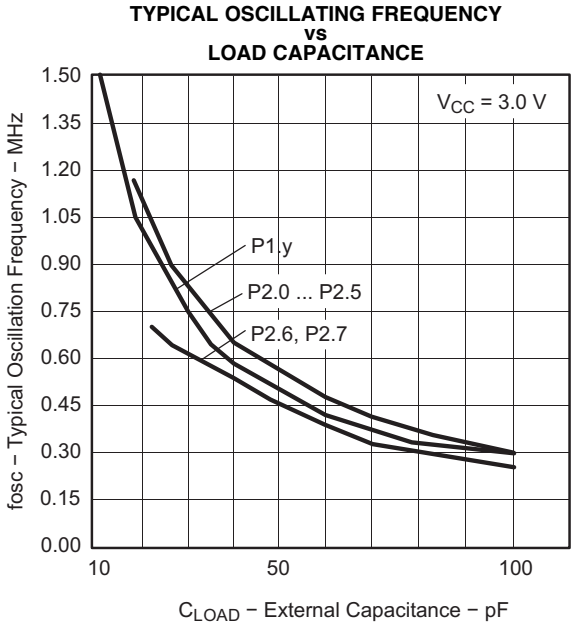
Pin-Oscillator Frequency – Ports Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$fo_{P1.x}$	Port output oscillation frequency	P1.y, C_L = 10 pF, R_L = 100 kΩ(1)(2)	3 V		1400		kHz
		P1.y, C_L = 20 pF, R_L = 100 kΩ(1)(2)			900		
$fo_{P2.x}$	Port output oscillation frequency	P2.0 to P2.5, C_L = 10 pF, R_L = 100 kΩ(1)(2)			1800		kHz
		P2.0 to P2.5, C_L = 20 pF, R_L = 100 kΩ(1)(2)	3 V		1000		
$fo_{P2.6/7}$	Port output oscillation frequency	P2.6 and P2.7, C_L = 20 pF, R_L = 100 kΩ(1)(2)	3 V		700		kHz
$fo_{P3.x}$	Port output oscillation frequency	P3.y, C_L = 10 pF, R_L = 100 kΩ(1)(2)			1800		kHz
		P3.y, C_L = 20 pF, R_L = 100 kΩ(1)(2)			1000		

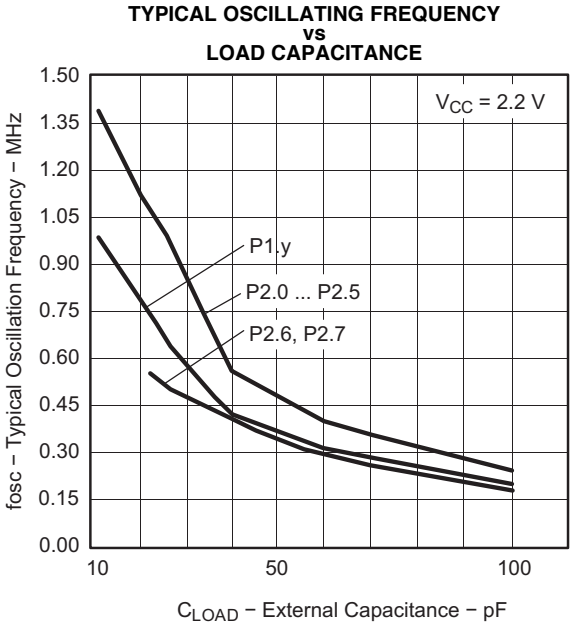
(1) A resistive divider with two 50-kΩ resistors between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics, Pin-Oscillator Frequency



A. One output active at a time.

Figure 10.



A. One output active at a time.

Figure 11.

POR, BOR(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(start)}$	See Figure 12	$dV_{CC}/dt \le 3$ V/s			0.7 × $V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$	See Figure 12 through Figure 14	$dV_{CC}/dt \le 3$ V/s			1.35		V
$V_{hys(B\_IT-)}$	See Figure 12	$dV_{CC}/dt \le 3$ V/s			140		mV
$t_{d(BOR)}$	See Figure 12				2000		μs
$t_{(reset)}$	Pulse duration needed at $\overline{RST}$/NMI pin to accepted reset internally		2.2 V	2			μs

(1) The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)}$ + $V_{hys(B_IT-)}$is ≤ 1.8 V.

(2) During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

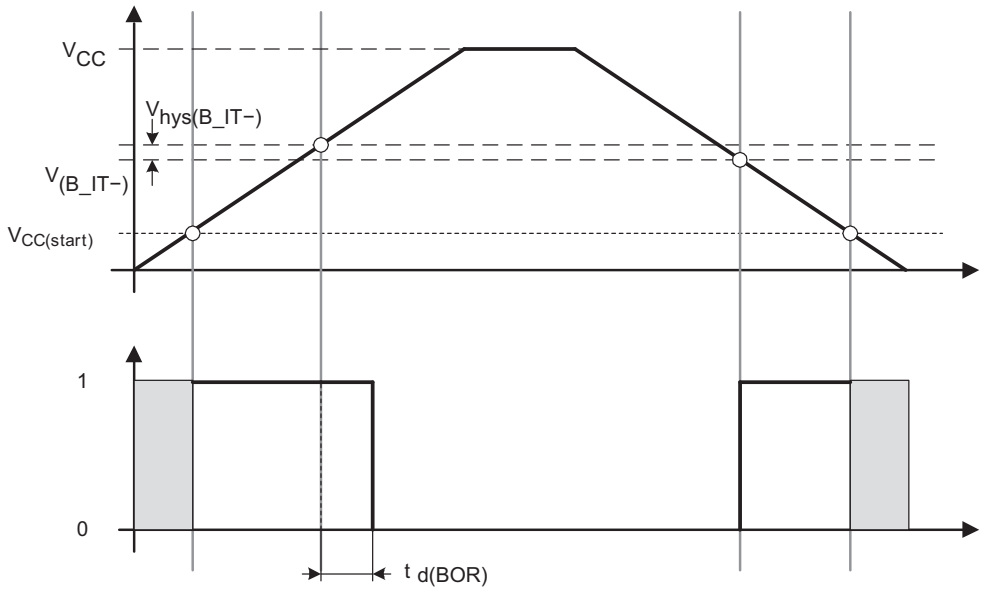


Figure 12. POR and BOR vs Supply Voltage

Typical Characteristics, POR and BOR

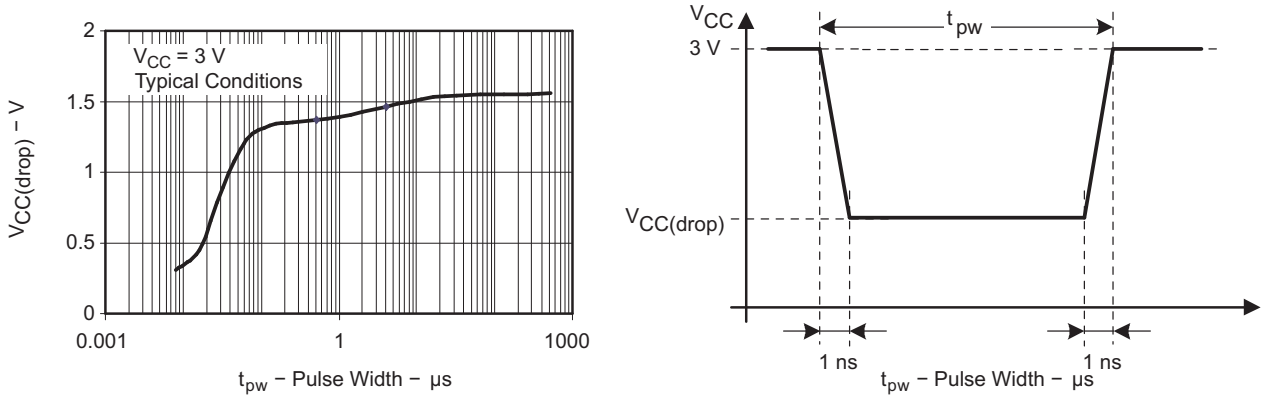


Figure 13. $V_{CC(drop)}$ Level With a Square Voltage Drop to Generate a POR or BOR Signal

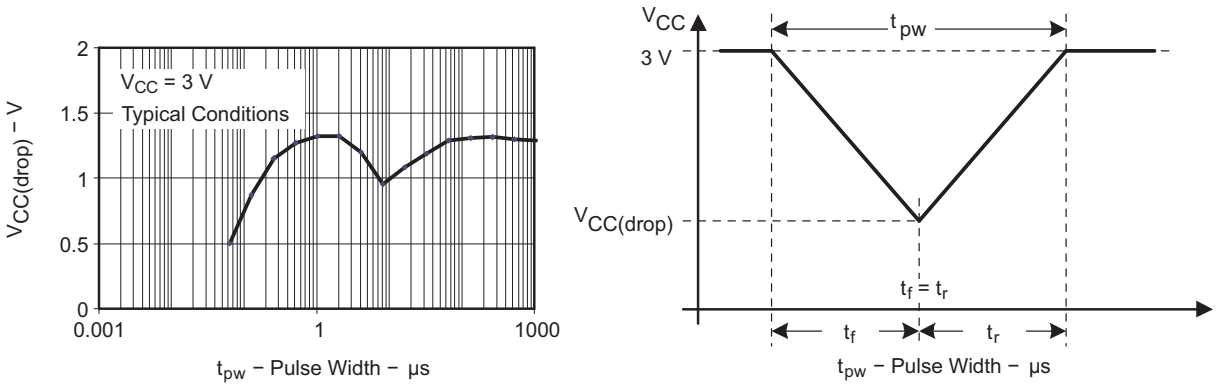


Figure 14. $V_{CC(drop)}$ Level With a Triangle Voltage Drop to Generate a POR or BOR Signal

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	RSELx < 14		1.8		3.6	V
		RSELx = 14		2.2		3.6	
		RSELx = 15		3		3.6	
$f_{DCO(0,0)}$	DCO frequency (0, 0)	RSELx = 0, DCOx = 0, MODx = 0	3 V	0.06		0.14	MHz
$f_{DCO(0,3)}$	DCO frequency (0, 3)	RSELx = 0, DCOx = 3, MODx = 0	3 V	0.07		0.17	MHz
$f_{DCO(1,3)}$	DCO frequency (1, 3)	RSELx = 1, DCOx = 3, MODx = 0	3 V		0.15		MHz
$f_{DCO(2,3)}$	DCO frequency (2, 3)	RSELx = 2, DCOx = 3, MODx = 0	3 V		0.21		MHz
$f_{DCO(3,3)}$	DCO frequency (3, 3)	RSELx = 3, DCOx = 3, MODx = 0	3 V		0.30		MHz
$f_{DCO(4,3)}$	DCO frequency (4, 3)	RSELx = 4, DCOx = 3, MODx = 0	3 V		0.41		MHz
$f_{DCO(5,3)}$	DCO frequency (5, 3)	RSELx = 5, DCOx = 3, MODx = 0	3 V		0.58		MHz
$f_{DCO(6,3)}$	DCO frequency (6, 3)	RSELx = 6, DCOx = 3, MODx = 0	3 V	0.54		1.06	MHz
$f_{DCO(7,3)}$	DCO frequency (7, 3)	RSELx = 7, DCOx = 3, MODx = 0	3 V	0.80		1.50	MHz
$f_{DCO(8,3)}$	DCO frequency (8, 3)	RSELx = 8, DCOx = 3, MODx = 0	3 V		1.6		MHz
$f_{DCO(9,3)}$	DCO frequency (9, 3)	RSELx = 9, DCOx = 3, MODx = 0	3 V		2.3		MHz
$f_{DCO(10,3)}$	DCO frequency (10, 3)	RSELx = 10, DCOx = 3, MODx = 0	3 V		3.4		MHz
$f_{DCO(11,3)}$	DCO frequency (11, 3)	RSELx = 11, DCOx = 3, MODx = 0	3 V		4.25		MHz
$f_{DCO(12,3)}$	DCO frequency (12, 3)	RSELx = 12, DCOx = 3, MODx = 0	3 V	4.30		7.30	MHz
$f_{DCO(13,3)}$	DCO frequency (13, 3)	RSELx = 13, DCOx = 3, MODx = 0	3 V	6.00	7.8	9.60	MHz
$f_{DCO(14,3)}$	DCO frequency (14, 3)	RSELx = 14, DCOx = 3, MODx = 0	3 V	8.60		13.9	MHz
$f_{DCO(15,3)}$	DCO frequency (15, 3)	RSELx = 15, DCOx = 3, MODx = 0	3 V	12.0		18.5	MHz
$f_{DCO(15,7)}$	DCO frequency (15, 7)	RSELx = 15, DCOx = 7, MODx = 0	3 V	16.0		26.0	MHz
S_{RSEL}	Frequency step between range RSEL and RSEL+1	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	3 V		1.35		ratio
S_{DCO}	Frequency step between tap DCO and DCO+1	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	3 V		1.08		ratio
	Duty cycle	Measured at SMCLK output	3 V		50		%

Calibrated DCO Frequencies, Tolerance

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
1-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	+3	%
1-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	30°C	1.8 V to 3.6 V	-3	±2	+3	%
1-MHz tolerance overall	BCSCTL1 = CALBC1_1MHZ, DCOCTL = CALDCO_1MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	1.8 V to 3.6 V	-6	±3	+6	%
8-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	+3	%
8-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	30°C	2.2 V to 3.6 V	-3	±2	+3	%
8-MHz tolerance overall	BCSCTL1 = CALBC1_8MHZ, DCOCTL = CALDCO_8MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	2.2 V to 3.6 V	-6	±3	+6	%
12-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	+3	%
12-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	30°C	2.7 V to 3.6 V	-3	±2	+3	%
12-MHz tolerance overall	BCSCTL1 = CALBC1_12MHZ, DCOCTL = CALDCO_12MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	2.7 V to 3.6 V	-6	±3	+6	%
16-MHz tolerance over temperature(1)	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	0°C to 85°C	3 V	-3	±0.5	+3	%
16-MHz tolerance over V_{CC}	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	30°C	3.3 V to 3.6 V	-3	±2	+3	%
16-MHz tolerance overall	BCSCTL1 = CALBC1_16MHZ, DCOCTL = CALDCO_16MHZ, calibrated at 30°C and 3 V	-40°C to 85°C	3.3 V to 3.6 V	-6	±3	+6	%

(1) This is the frequency change from the measured frequency at 30°C over temperature.

Wake-Up From Lower-Power Modes (LPM3/4)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{DCO,LPM3/4}$	DCO clock wake-up time from LPM3/4 (1)	BCSCTL1 = CALBC1_1MHz, DCOCTL = CALDCO_1MHz	3 V		1.5		μs
$t_{CPU,LPM3/4}$	CPU wake-up time from LPM3/4 (2)				$1/f_{MCLK}$ + $t_{Clock,LPM3/4}$		

(1) The DCO clock wake-up time is measured from the edge of an external wake-up signal (e.g., port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
(2) Parameter applicable only if DCOCLK is used for MCLK.

Typical Characteristics, DCO Clock Wake-Up Time From LPM3/4

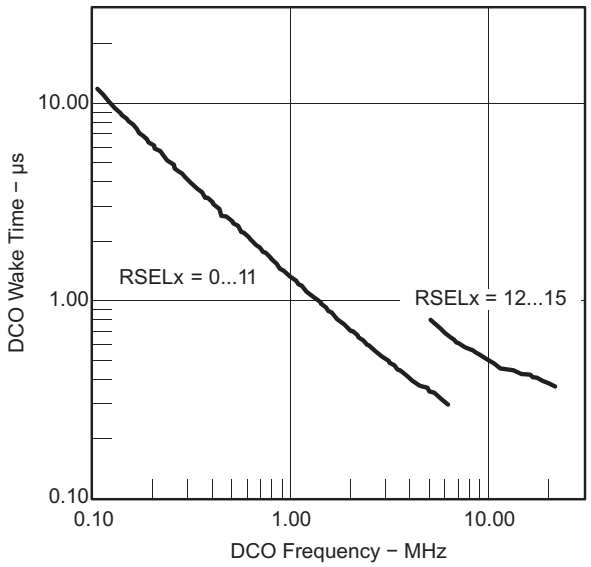


Figure 15. DCO Wake-Up Time From LPM3 vs DCO Frequency

Crystal Oscillator, XT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1	1.8 V to 3.6 V		32768		Hz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, XCAPx = 0, LFXT1Sx = 3	1.8 V to 3.6 V	10000	32768	50000	Hz
OA_{LF}	Oscillation allowance for LF crystals	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			500		kΩ
		XTS = 0, LFXT1Sx = 0, $f_{LFXT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			200		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(2)	XTS = 0, XCAPx = 0			1		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			11		
	Duty cycle, LF mode	XTS = 0, Measured at P2.0/ACLK, $f_{LFXT1,LF}$ = 32768 Hz	2.2 V	30	50	70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(3)	XTS = 0, XCAPx = 0, LFXT1Sx = 3(4)	2.2 V	10		10000	Hz

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and process that avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If a conformal coating is used, ensure that it does not induce capacitive or resistive leakage between the oscillator pins.
(g) Do not route the XOUT line to the JTAG header to support the serial programming adapter as shown in other documentation. This signal is no longer required for the serial programming adapter.

(2) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Because the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(3) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(4) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		T_A	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	-40°C to 85°C	3 V	4	12	20	kHz
df_{VLO}/d_T	VLO frequency temperature drift	-40°C to 85°C	3 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	25°C	1.8 V to 3.6 V		4		%/V

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	SMCLK, duty cycle = 50% ± 10%			f_{SYSTEM}		MHz
$t_{TA,cap}$	Timer_A capture timing	TA0, TA1	3 V	20			ns

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, duty cycle = 50% ± 10%			f_{SYSTEM}		MHz
$f_{max,BITCLK}$	Maximum BITCLK clock frequency (equals baudrate in MBaud) (1)		3 V	2			MHz
t_T	UART receive deglitch time (2)		3 V	50	100	600	ns

(1) The DCO wake-up time must be considered in LPM3 and LPM4 for baud rates above 1 MHz.
(2) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized, their duration should exceed the maximum specification of the deglitch time.

USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 16 and Figure 17)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time		3 V	75			ns
$t_{HD,MI}$	SOMI input data hold time		3 V	0			ns
$t_{VALID,MO}$	SIMO output data valid time	UCLK edge to SIMO valid, C_L = 20 pF	3 V			20	ns

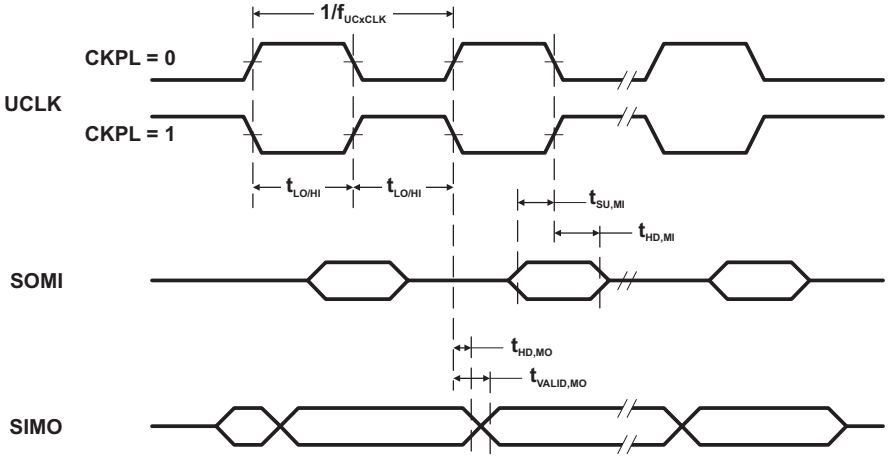


Figure 16. SPI Master Mode, CKPH = 0

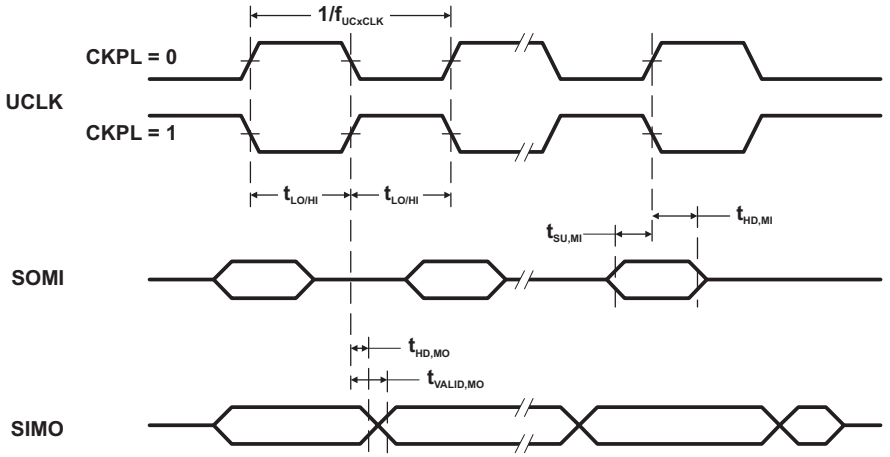


Figure 17. SPI Master Mode, CKPH = 1

USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 18 and Figure 19)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock		3 V		50		ns
$t_{STE,LAG}$	STE lag time, Last clock to STE high		3 V	10			ns
$t_{STE,ACC}$	STE access time, STE low to SOMI data out		3 V		50		ns
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance		3 V		50		ns
$t_{SU,SI}$	SIMO input data setup time		3 V	15			ns
$t_{HD,SI}$	SIMO input data hold time		3 V	10			ns
$t_{VALID,SO}$	SOMI output data valid time	UCLK edge to SOMI valid, C_L = 20 pF	3 V		50	75	ns

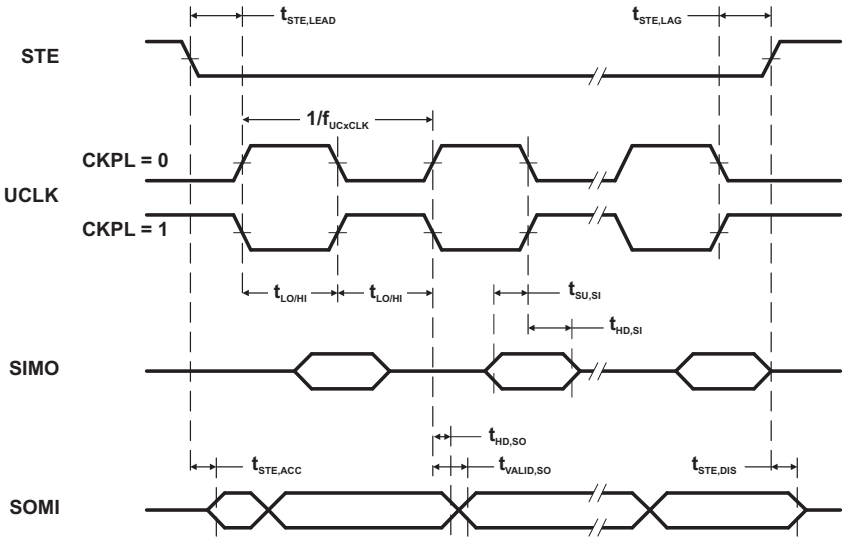


Figure 18. SPI Slave Mode, CKPH = 0

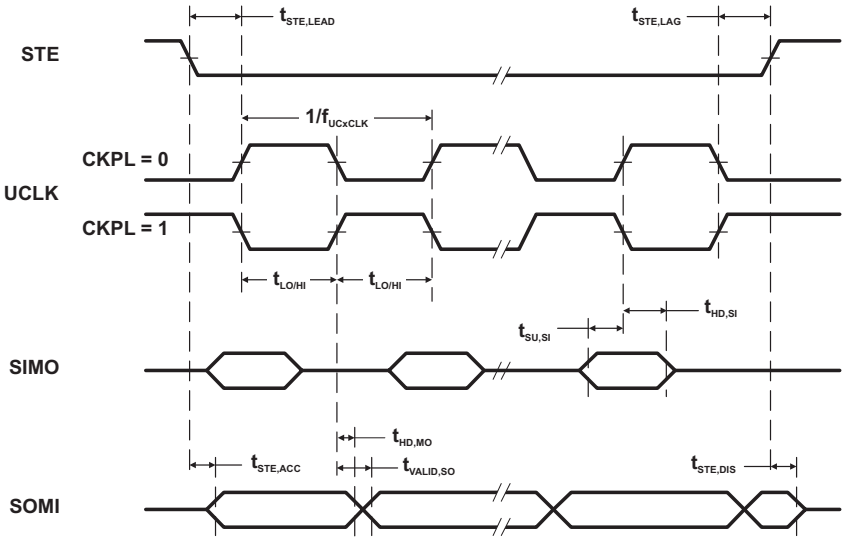


Figure 19. SPI Slave Mode, CKPH = 1

USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 20)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \le 100$ kHz	3 V	4.0			µs
		$f_{SCL} > 100$ kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \le 100$ kHz	3 V	4.7			µs
		$f_{SCL} > 100$ kHz		0.6			
$t_{HD,DAT}$	Data hold time		3 V	0			ns
$t_{SU,DAT}$	Data setup time		3 V	250			ns
$t_{SU,STO}$	Setup time for STOP		3 V	4.0			µs
t_{SP}	Pulse width of spikes suppressed by input filter		3 V	50	100	600	ns

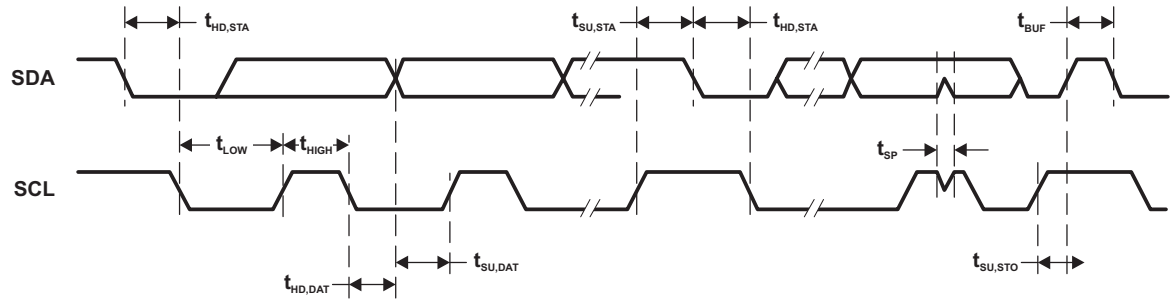


Figure 20. I2C Mode Timing

Comparator_A+

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$ (1)		CAON = 1, CARSEL = 0, CAREF = 0	3 V		45		µA
$I_{(Refladder/RefDiode)}$		CAON = 1, CARSEL = 0, CAREF = 1, 2, or 3, No load at CA0 and CA1	3 V		45		µA
$V_{(IC)}$	Common–mode input voltage	CAON = 1	3 V	0		V_{CC}-1	V
$V_{(Ref025)}$	(Voltage at 0.25 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at CA0 and CA1	3 V		0.24		
$V_{(Ref050)}$	(Voltage at 0.5 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at CA0 and CA1	3 V		0.48		
$V_{(RefVT)}$	See Figure 21 and Figure 22	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at CA0 and CA1, TA = 85°C	3 V		490		mV
$V_{(offset)}$	Offset voltage (2)		3 V		±10		mV
V_{hys}	Input hysteresis	CAON = 1	3 V		0.7		mV
$t_{(response)}$	Response time (low-high and high-low)	T_A = 25°C, Overdrive 10 mV, Without filter: CAF = 0	3 V		120		ns
		T_A = 25°C, Overdrive 10 mV, With filter: CAF = 1			1.5		µs

(1) The leakage current for the Comparator_A+ terminals is identical to $I_{lkg(Px.y)}$ specification.
(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A+ inputs on successive measurements. The two successive measurements are then summed together.

Typical Characteristics – Comparator_A+

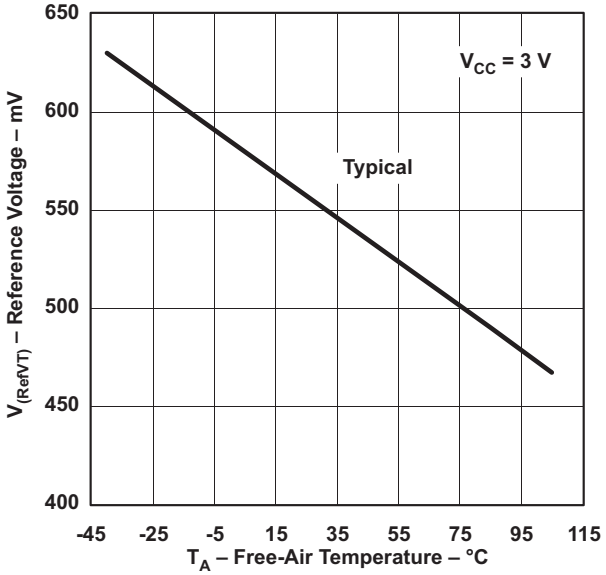


Figure 21. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

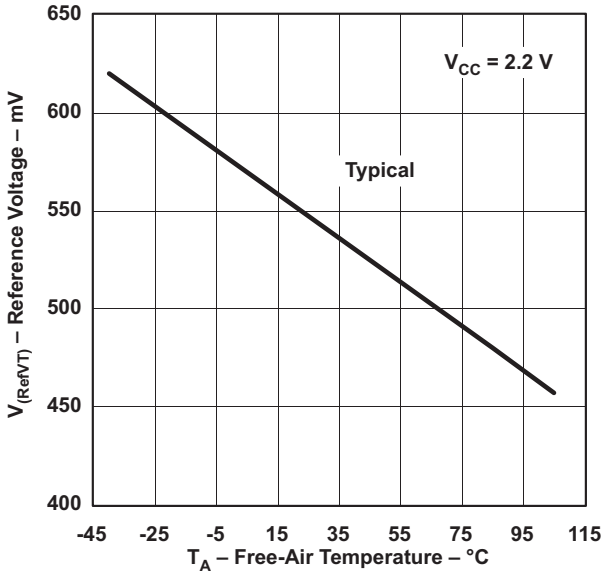


Figure 22. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

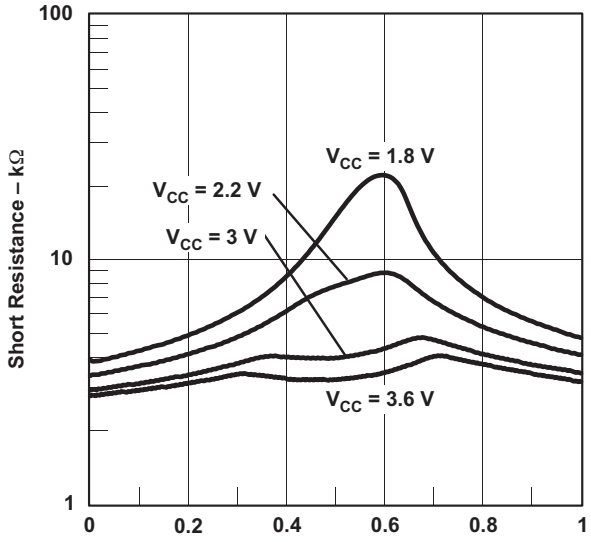


Figure 23. Short Resistance vs V_{IN}/V_{CC}

10-Bit ADC, Power Supply and Input Range Conditions (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Analog supply voltage	V_{SS} = 0 V			2.2		3.6	V
V_{Ax}	Analog input voltage(2)	All Ax terminals, Analog inputs selected in ADC10AE register		3 V	0		V_{CC}	V
I_{ADC10}	ADC10 supply current(3)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 1, REFON = 0, ADC10SHT0 = 1, ADC10SHT1 = 0, ADC10DIV = 0	25°C	3 V		0.6		mA
I_{REF+}	Reference supply current, reference buffer disabled(4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 0, REFON = 1, REFOUT = 0	25°C	3 V		0.25		mA
		$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REF2_5V = 1, REFON = 1, REFOUT = 0				0.25		
$I_{REFB,0}$	Reference buffer supply current with ADC10SR = 0(4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 0	25°C	3 V		1.1		mA
$I_{REFB,1}$	Reference buffer supply current with ADC10SR = 1(4)	$f_{ADC10CLK}$ = 5.0 MHz, ADC10ON = 0, REFON = 1, REF2_5V = 0, REFOUT = 1, ADC10SR = 1	25°C	3 V		0.5		mA
C_I	Input capacitance	Only one terminal Ax can be selected at one time	25°C	3 V			27	pF
R_I	Input MUX ON resistance	0 V ≤ V_{Ax} ≤ V_{CC}	25°C	3 V		1000		Ω

(1) The leakage current is defined in the leakage current table with Px.y/Ax parameter.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC10}.
(4) The internal reference current is supplied via terminal V_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables the built-in reference to settle before starting an A/D conversion.

10-Bit ADC, Built-In Voltage Reference (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC,REF+}$	Positive built-in reference analog supply voltage range	$I_{VREF+} \le 1$ mA, REF2_5V = 0		2.2			V
		$I_{VREF+} \le 1$ mA, REF2_5V = 1		2.9			
V_{REF+}	Positive built-in reference voltage	$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 0	3 V	1.41	1.5	1.59	V
		$I_{VREF+} \le I_{VREF+}$max, REF2_5V = 1		2.35	2.5	2.65	
$I_{LD,VREF+}$	Maximum VREF+ load current		3 V			±1	mA
	VREF+ load regulation	I_{VREF+} = 500 μA ± 100 μA, Analog input voltage $V_{Ax} \ne$ 0.75 V, REF2_5V = 0	3 V			±2	LSB
		I_{VREF+} = 500 μA ± 100 μA, Analog input voltage $V_{Ax} \ne$ 1.25 V, REF2_5V = 1				±2	
	V_{REF+} load regulation response time	I_{VREF+} = 100 μA→900 μA, $V_{Ax} \ne 0.5 \times$ VREF+, Error of conversion result ≤ 1 LSB, ADC10SR = 0	3 V			400	ns
C_{VREF+}	Maximum capacitance at pin VREF+	$I_{VREF+} \le \pm 1$ mA, REFON = 1, REFOUT = 1	3 V			100	pF
TC_{REF+}	Temperature coefficient (1)	I_{VREF+} = const with 0 mA ≤ I_{VREF+} ≤ 1 mA	3 V			±100	ppm/°C
t_{REFON}	Settling time of internal reference voltage to 99.9% VREF	I_{VREF+} = 0.5 mA, REF2_5V = 0, REFON = 0 → 1	3.6 V			30	μs
$t_{REFBURST}$	Settling time of reference buffer to 99.9% VREF	I_{VREF+} = 0.5 mA, REF2_5V = 1, REFON = 1, REFBURST = 1, ADC10SR = 0	3 V			2	μs

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))

10-Bit ADC, External Reference[1] (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
VEREF+	Positive external reference input voltage range [2]	VEREF+ > VEREF–, SREF1 = 1, SREF0 = 0		1.4		V_{CC}	V
		VEREF– ≤ VEREF+ ≤ V_{CC} – 0.15 V, SREF1 = 1, SREF0 = 1 [3]		1.4		3	
VEREF–	Negative external reference input voltage range [4]	VEREF+ > VEREF–		0		1.2	V
ΔVEREF	Differential external reference input voltage range, ΔVEREF = VEREF+ – VEREF–	VEREF+ > VEREF– [5]		1.4		V_{CC}	V
I_{VEREF+}	Static input current into VEREF+	0 V ≤ VEREF+ ≤ V_{CC}, SREF1 = 1, SREF0 = 0	3 V		±1		μA
		0 V ≤ VEREF+ ≤ V_{CC} – 0.15 V ≤ 3 V, SREF1 = 1, SREF0 = 1 [3]	3 V		0		
$I_{VEREF–}$	Static input current into VEREF–	0 V ≤ VEREF– ≤ V_{CC}	3 V		±1		μA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) Under this condition the external reference is internally buffered. The reference buffer is active and requires the reference buffer supply current I_{REFB}. The current consumption can be limited to the sample and conversion period with REBURST = 1.
(4) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(5) The accuracy limits the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

10-Bit ADC, Timing Parameters (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC10 input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR = 0	3 V	0.45		6.3	MHz
			ADC10SR = 1		0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	2.06		3.51	μs
		$f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0			13 × ADC10DIV × $1/f_{ADC10CLK}$			
$t_{ADC10ON}$	Turn-on settling time of the ADC	[1]					100	ns

(1) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

10-Bit ADC, Linearity Parameters (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		3 V			±1	LSB
E_D	Differential linearity error		3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω	3 V			±1	LSB
E_G	Gain error		3 V		±1.1	±2	LSB
E_T	Total unadjusted error		3 V		±2	±5	LSB

10-Bit ADC, Temperature Sensor and Built-In V_{MID} (MSP430G2x53 Only)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Temperature sensor supply current (1)	REFON = 0, INCHx = 0Ah, T_A = 25°C	3 V		60		µA
TC_{SENSOR}		ADC10ON = 1, INCHx = 0Ah (2)	3 V		3.55		mV/°C
$t_{Sensor(sample)}$	Sample time required if channel 10 is selected (3)	ADC10ON = 1, INCHx = 0Ah, Error of conversion result ≤ 1 LSB	3 V	30			µs
I_{VMID}	Current into divider at channel 11	ADC10ON = 1, INCHx = 0Bh	3 V			(4)	µA
V_{MID}	V_{CC} divider at channel 11	ADC10ON = 1, INCHx = 0Bh, $V_{MID} \neq 0.5 \times V_{CC}$	3 V		1.5		V
$t_{VMID(sample)}$	Sample time required if channel 11 is selected (5)	ADC10ON = 1, INCHx = 0Bh, Error of conversion result ≤ 1 LSB	3 V	1220			ns

(1) The sensor current I_{SENSOR} is consumed if (ADC10ON = 1 and REFON = 1) or (ADC10ON = 1 and INCH = 0Ah and sample signal is high). When REFON = 1, I_{SENSOR} is included in I_{REF+}. When REFON = 0, I_{SENSOR} applies during conversion of the temperature sensor input (INCH = 0Ah).
(2) The following formula can be used to calculate the temperature sensor output voltage:
$V_{Sensor,typ} = TC_{Sensor}$ (273 + T [°C]) + $V_{Offset,sensor}$ [mV] or
$V_{Sensor,typ} = TC_{Sensor}$ T [°C] + $V_{Sensor}(T_A = 0°C)$ [mV]
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) No additional current is needed. The V_{MID} is used during sampling.
(5) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage			2.2		3.6	V
f_{FTG}	Flash timing generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.2 V, 3.6 V		1	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.2 V, 3.6 V		1	7	mA
t_{CPT}	Cumulative program time (1)		2.2 V, 3.6 V			10	ms
$t_{CMErase}$	Cumulative mass erase time		2.2 V, 3.6 V	20			ms
	Program/erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	(2)			30		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word	(2)			25		t_{FTG}
$t_{Block, 1-63}$	Block program time for each additional byte or word	(2)			18		t_{FTG}
$t_{Block, End}$	Block program end-sequence wait time	(2)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time	(2)			10593		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time	(2)			4819		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
(2) These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{(RAMh)}$	RAM retention supply voltage [1]	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage V_{CC} when the data in RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency		2.2 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration		2.2 V	0.025		15	μs
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge[1])		2.2 V			1	μs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time		2.2 V	15		100	μs
f_{TCK}	TCK input frequency[2]		2.2 V	0		5	MHz
$R_{Internal}$	Internal pulldown resistance on TEST		2.2 V	25	60	90	kΩ

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the maximum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse[1]

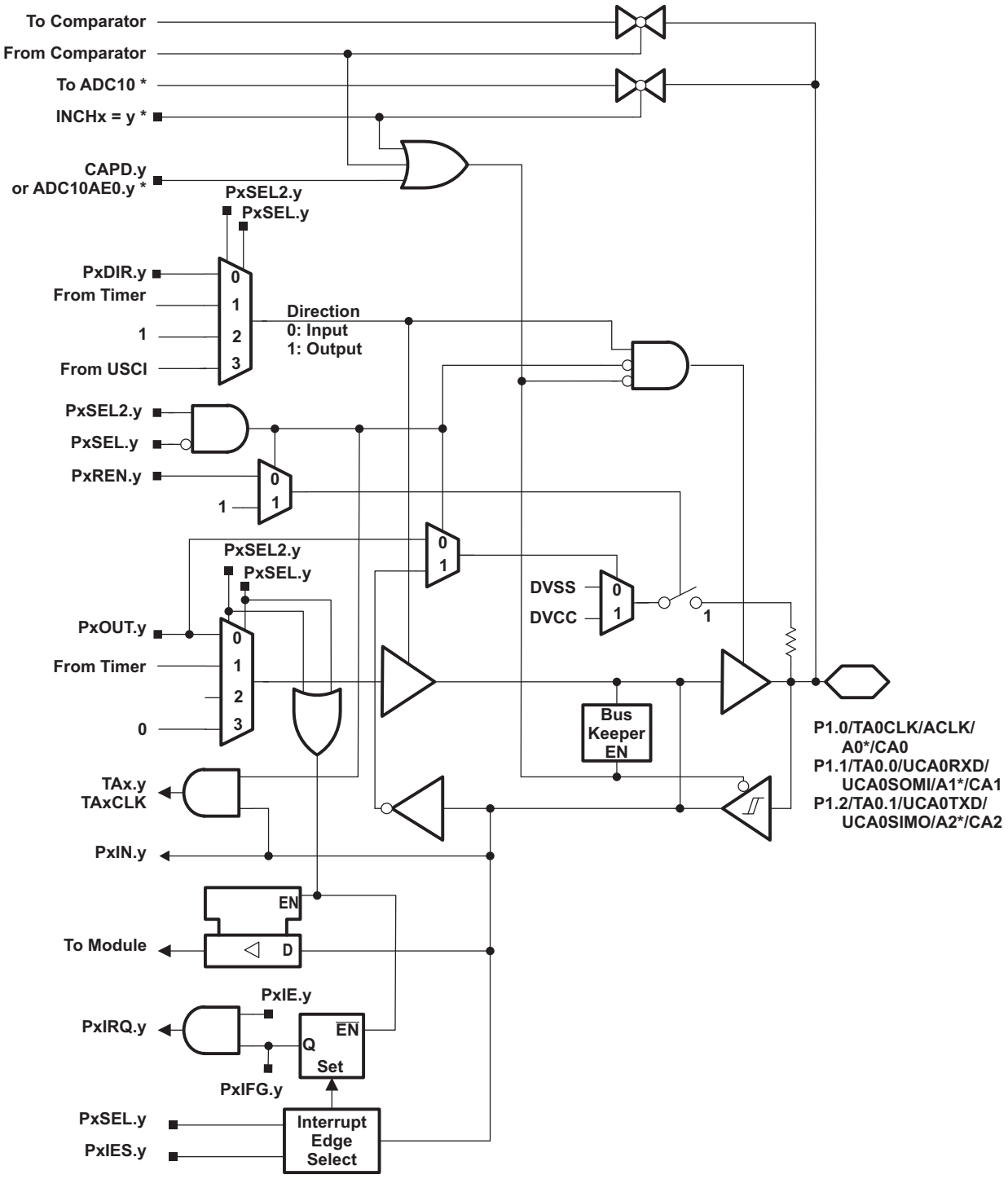
over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C	2.5		V
V_{FB}	Voltage level on TEST for fuse blow		6	7	V
I_{FB}	Supply current into TEST during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) Once the fuse is blown, no further access to the JTAG/Test, Spy-Bi-Wire, and emulation feature is possible, and JTAG is switched to bypass mode.

PORT SCHEMATICS

Port P1 Pin Schematic: P1.0 to P1.2, Input/Output With Schmitt Trigger



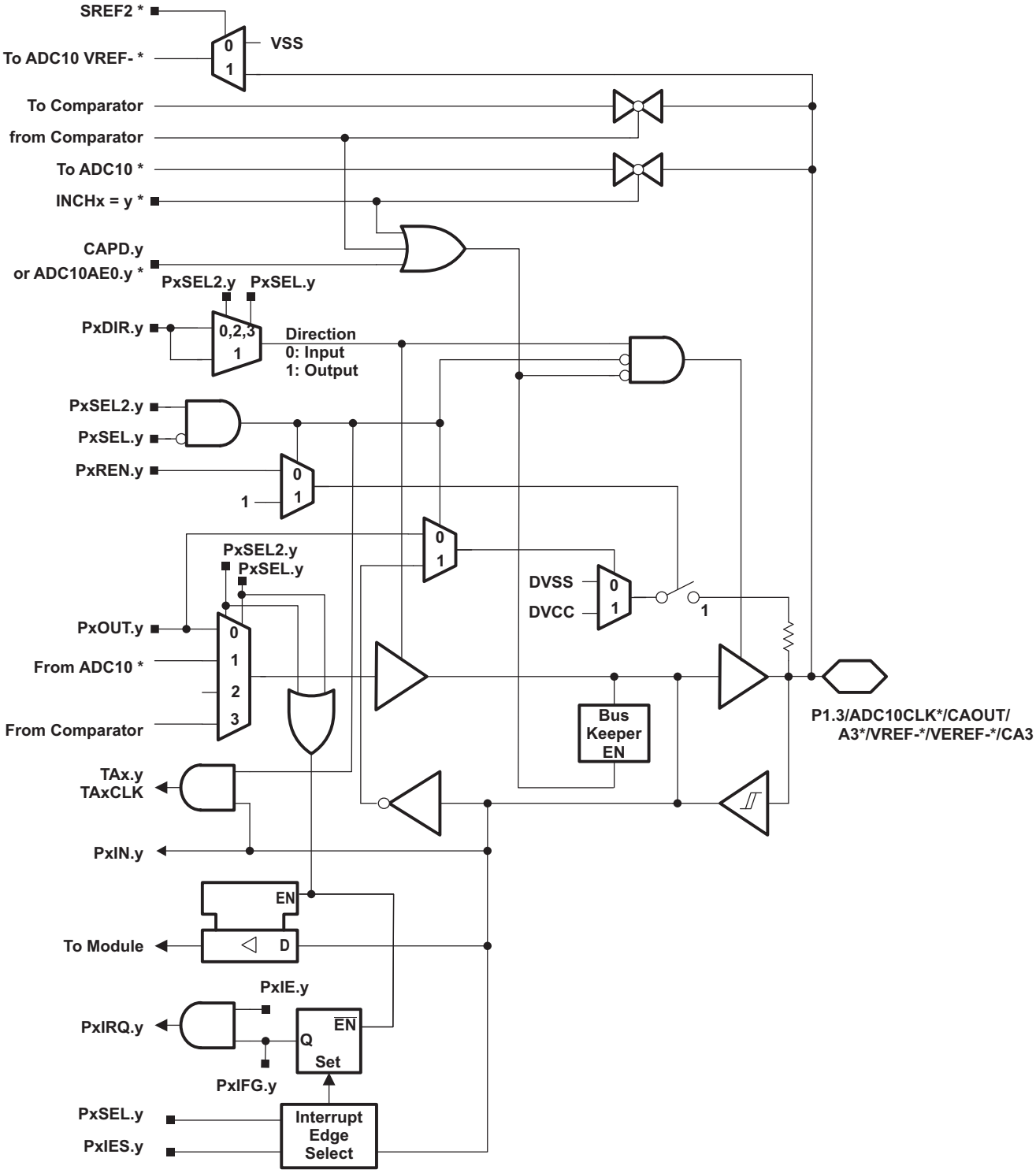
* Note: MSP430G2x53 devices only. MSP430G2x13 devices have no ADC10.

Table 16. Port P1 (P1.0 to P1.2) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	CAPD.y
P1.0/	0	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0CLK/		TA0.TACLK	0	1	0	0	0
ACLK/		ACLK	1	1	0	0	0
A0[2]/		A0	X	X	X	1 (y = 0)	0
CA0/		CA0	X	X	X	0	1 (y = 0)
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.1/	1	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.0/		TA0.0	1	1	0	0	0
		TA0.CCI0A	0	1	0	0	0
UCA0RXD/		UCA0RXD	from USCI	1	1	0	0
UCA0SOMI/		UCA0SOMI	from USCI	1	1	0	0
A1[2]/		A1	X	X	X	1 (y = 1)	0
CA1/		CA1	X	X	X	0	1 (y = 1)
Pin Osc		Capacitive sensing	X	0	1	0	0
P1.2/	2	P1.x (I/O)	I: 0; O: 1	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0
		TA0.CCI1A	0	1	0	0	0
UCA0TXD/		UCA0TXD	from USCI	1	1	0	0
UCA0SIMO/		UCA0SIMO	from USCI	1	1	0	0
A2[2]/		A2	X	X	X	1 (y = 2)	0
CA2/		CA2	X	X	X	0	1 (y = 2)
Pin Osc		Capacitive sensing	X	0	1	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Port P1 Pin Schematic: P1.3, Input/Output With Schmitt Trigger



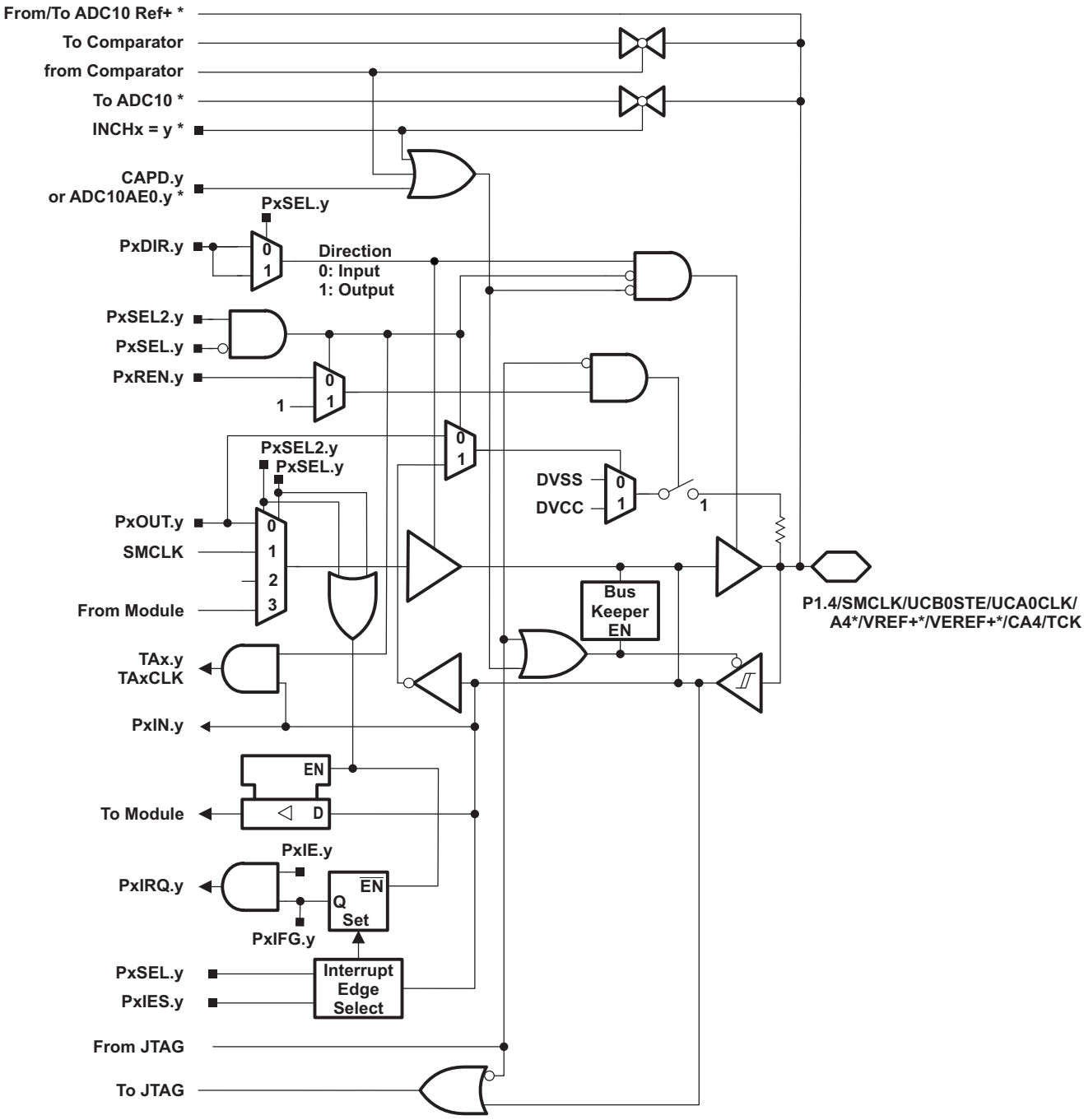
*** Note: MSP430G2x53 devices only. MSP430G2x13 devices have no ADC10.**

Table 17. Port P1 (P1.3) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]				
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	CAPD.y
P1.3/	3	P1.x (I/O)	I: 0; O: 1	0	0	0	0
ADC10CLK[2]/		ADC10CLK	1	1	0	0	0
CAOUT/		CAOUT	1	1	1	0	0
A3[2]/		A3	X	X	X	1 (y = 3)	0
VREF-[2]/		VREF-	X	X	X	1	0
VEREF-[2]/		VEREF-	X	X	X	1	0
CA3/		CA3	X	X	X	0	1 (y = 3)
Pin Osc		Capacitive sensing	X	0	1	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Port P1 Pin Schematic: P1.4, Input/Output With Schmitt Trigger



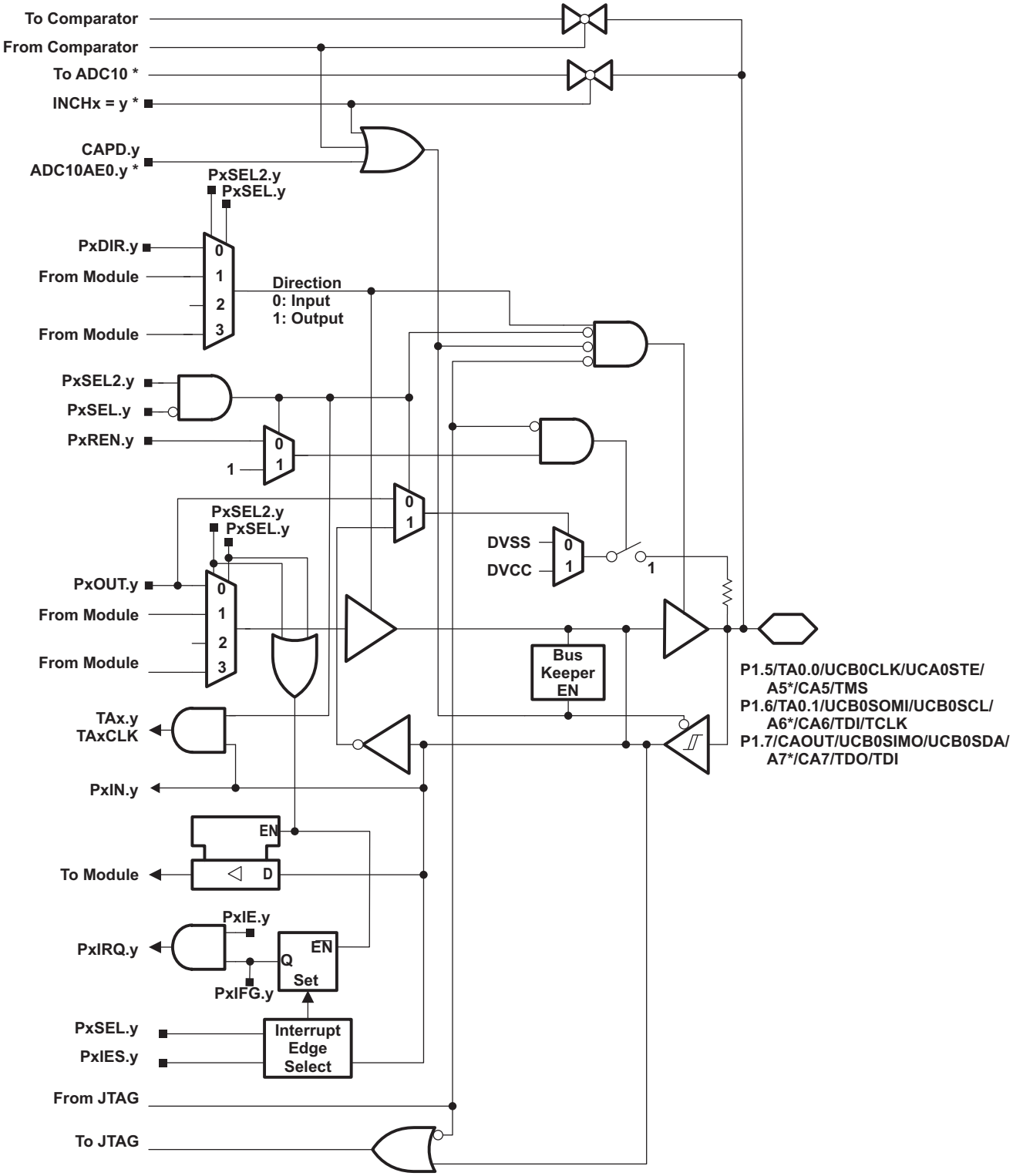
* Note: MSP430G2x52 devices only. MSP430G2x12 devices have no ADC10.

Table 18. Port P1 (P1.4) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]					
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	JTAG Mode	CAPD.y
P1.4/	4	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
SMCLK/		SMCLK	1	1	0	0	0	0
UCB0STE/		UCB0STE	from USCI	1	1	0	0	0
UCA0CLK/		UCA0CLK	from USCI	1	1	0	0	0
VREF+[2]/		VREF+	X	X	X	1	0	0
VEREF+[2]/		VEREF+	X	X	X	1	0	0
A4[2]/		A4	X	X	X	1 (y = 4)	0	0
CA4		CA4	X	X	X	0	0	1 (y = 4)
TCK/		TCK	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Port P1 Pin Schematic: P1.5 to P1.7, Input/Output With Schmitt Trigger



*** Note: MSP430G2x53 devices only. MSP430G2x13 devices have no ADC10.**

Table 19. Port P1 (P1.5 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]					
			P1DIR.x	P1SEL.x	P1SEL2.x	ADC10AE.x INCH.x=1[2]	JTAG Mode	CAPD.y
P1.5/	5	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
TA0.0/		TA0.0	1	1	0	0	0	0
UCB0CLK/		UCB0CLK	from USCI	1	1	0	0	0
UCA0STE/		UCA0STE	from USCI	1	1	0	0	0
A5[2]/		A5	X	X	X	1 (y = 5)	0	0
CA5		CA5	X	X	X	0	0	1 (y = 5)
TMS		TMS	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0
P1.6/	6	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
TA0.1/		TA0.1	1	1	0	0	0	0
UCB0SOMI/		UCB0SOMI	from USCI	1	1	0	0	0
UCB0SCL/		UCB0SCL	from USCI	1	1	0	0	0
A6[2]/		A6	X	X	X	1 (y = 6)	0	0
CA6		CA6	X	X	X	0	0	1 (y = 6)
TDI/TCLK/		TDI/TCLK	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0
P1.7/	7	P1.x (I/O)	I: 0; O: 1	0	0	0	0	0
UCB0SIMO/		UCB0SIMO	from USCI	1	1	0	0	0
UCB0SDA/		UCB0SDA	from USCI	1	1	0	0	0
A7[2]/		A7	X	X	X	1 (y = 7)	0	0
CA7		CA7	X	X	X	0	0	1 (y = 7)
CAOUT		CAOUT	1	1	0	0	0	0
TDO/TDI/		TDO/TDI	X	X	X	0	1	0
Pin Osc		Capacitive sensing	X	0	1	0	0	0

(1) X = don't care
(2) MSP430G2x53 devices only

Port P2 Pin Schematic: P2.0 to P2.5, Input/Output With Schmitt Trigger

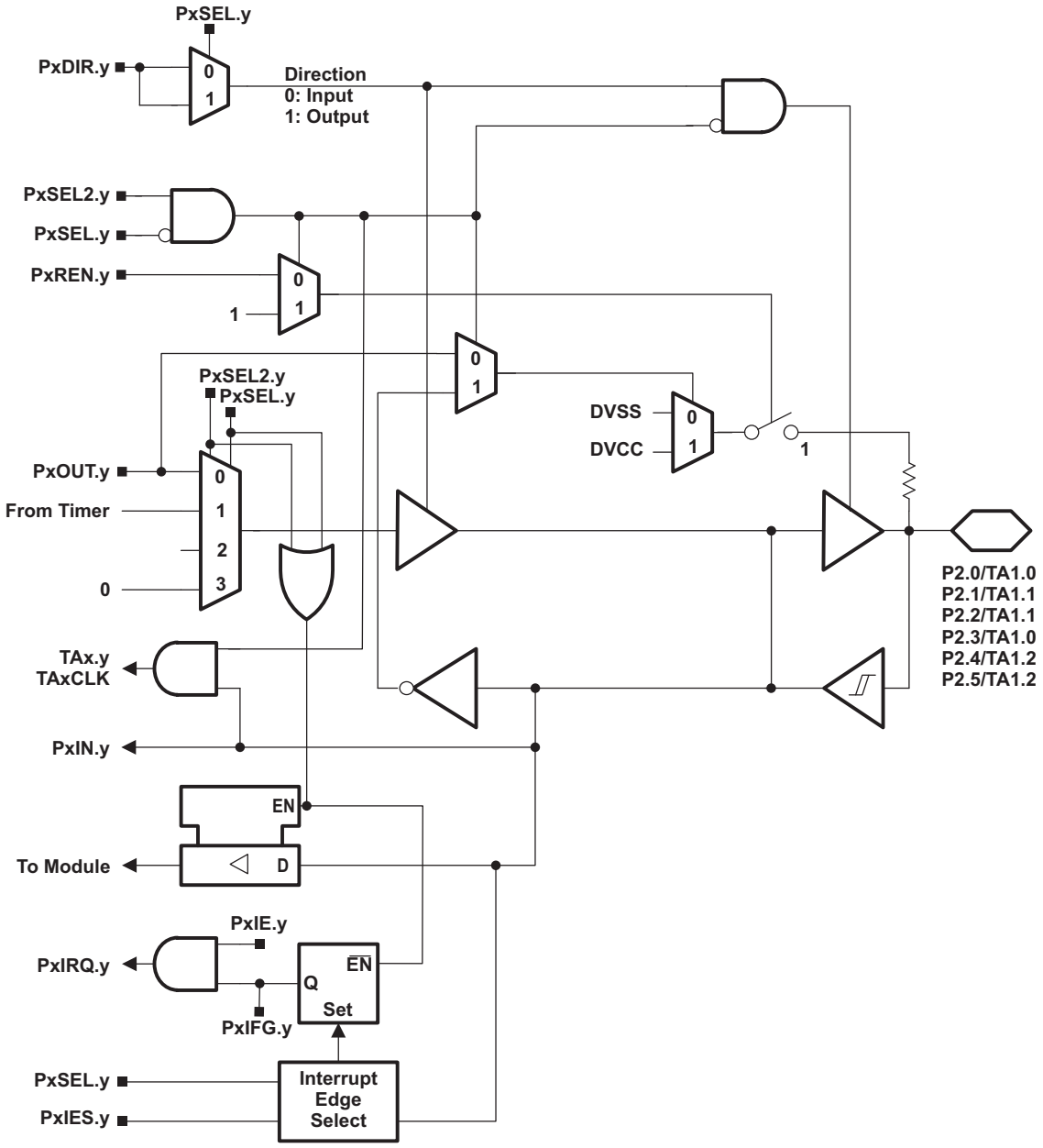


Table 20. Port P2 (P2.0 to P2.5) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P2DIR.x	P2SEL.x	P2SEL2.x
P2.0/	0	P2.x (I/O)	I: 0; O: 1	0	0
TA1.0/		Timer1_A3.CCI0A	0	1	0
		Timer1_A3.TA0	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.1/	1	P2.x (I/O)	I: 0; O: 1	0	0
TA1.1/		Timer1_A3.CCI1A	0	1	0
		Timer1_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.2/	2	P2.x (I/O)	I: 0; O: 1	0	0
TA1.1/		Timer1_A3.CCI1B	0	1	0
		Timer1_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.3/	3	P2.x (I/O)	I: 0; O: 1	0	0
TA1.0/		Timer1_A3.CCI0B	0	1	0
		Timer1_A3.TA0	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.4/	4	P2.x (I/O)	I: 0; O: 1	0	0
TA1.2/		Timer1_A3.CCI2A	0	1	0
		Timer1_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P2.5/	5	P2.x (I/O)	I: 0; O: 1	0	0
TA1.2/		Timer1_A3.CCI2B	0	1	0
		Timer1_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1

(1) X = don't care

Port P2 Pin Schematic: P2.6, Input/Output With Schmitt Trigger

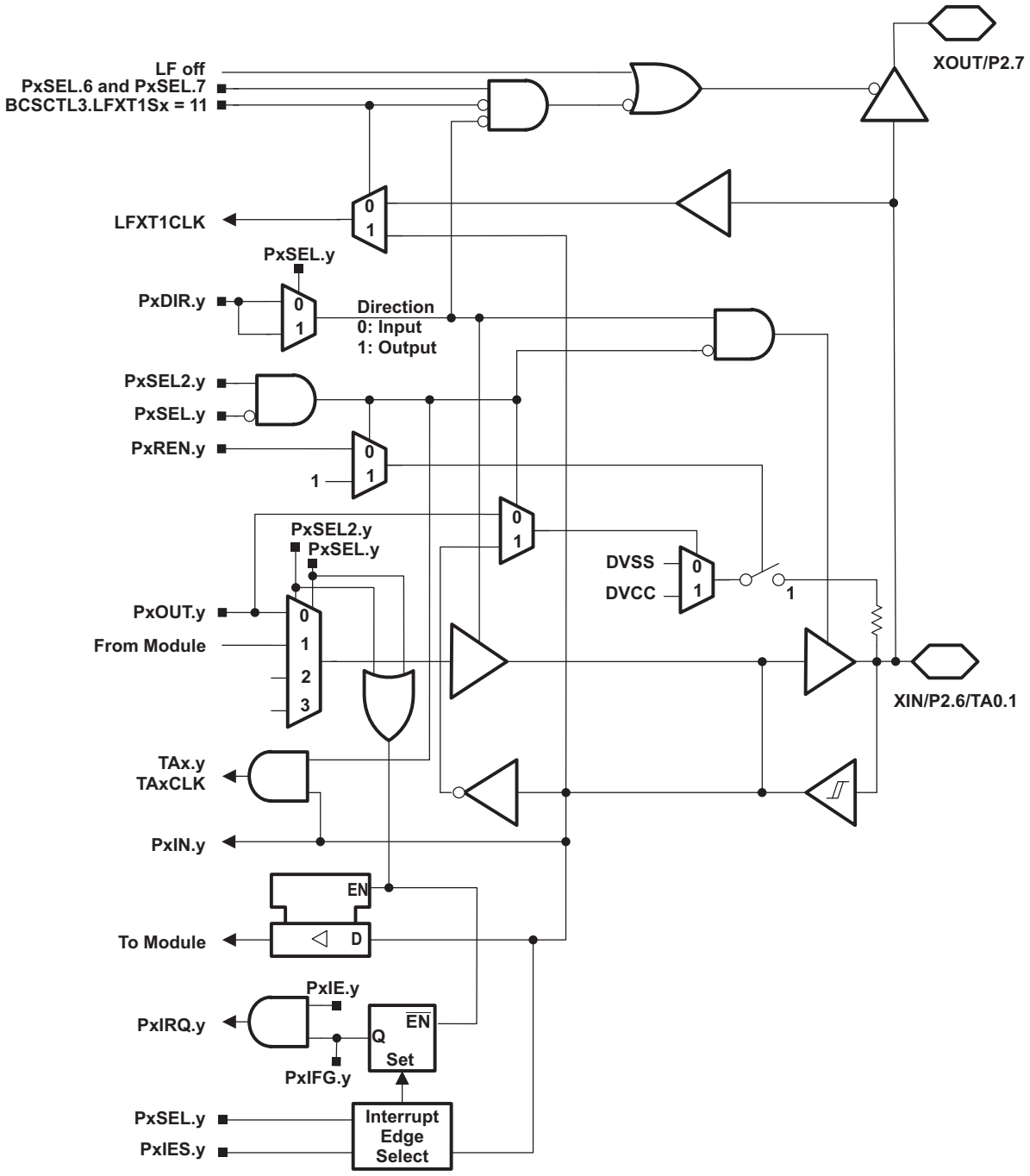


Table 21. Port P2 (P2.6) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P2DIR.x	P2SEL.6 P2SEL.7	P2SEL2.6 P2SEL2.7
XIN	6	XIN	0	1 1	0 0
P2.6		P2.x (I/O)	I: 0; O: 1	0 X	0 0
TA0.1		Timer0_A3.TA1	1	1 0	0 0
Pin Osc		Capacitive sensing	X	0 X	1 X

(1) X = don't care

Port P2 Pin Schematic: P2.7, Input/Output With Schmitt Trigger

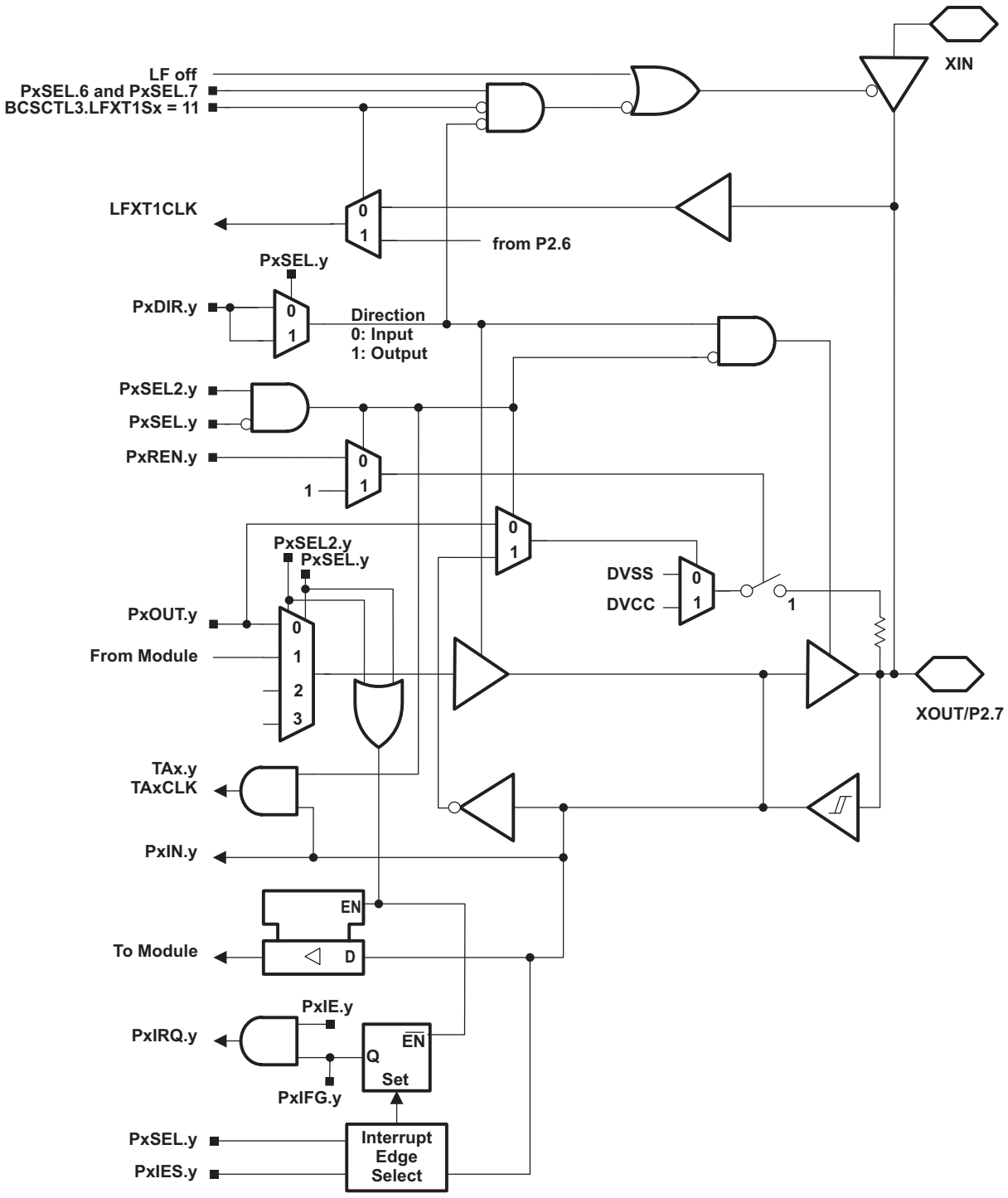


Table 22. Port P2 (P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P2DIR.x	P2SEL.6 P2SEL.7	P2SEL2.6 P2SEL2.7
XOUT/	7	XOUT	1	1 1	0 0
P2.7/		P2.x (I/O)	I: 0; O: 1	0 X	0 0
Pin Osc		Capacitive sensing	X	0 X	1 X

(1) X = don't care

Port P3 Pin Schematic: P3.0 to P3.7, Input/Output With Schmitt Trigger (28-Pin PW and 32-Pin RHB Packages Only)

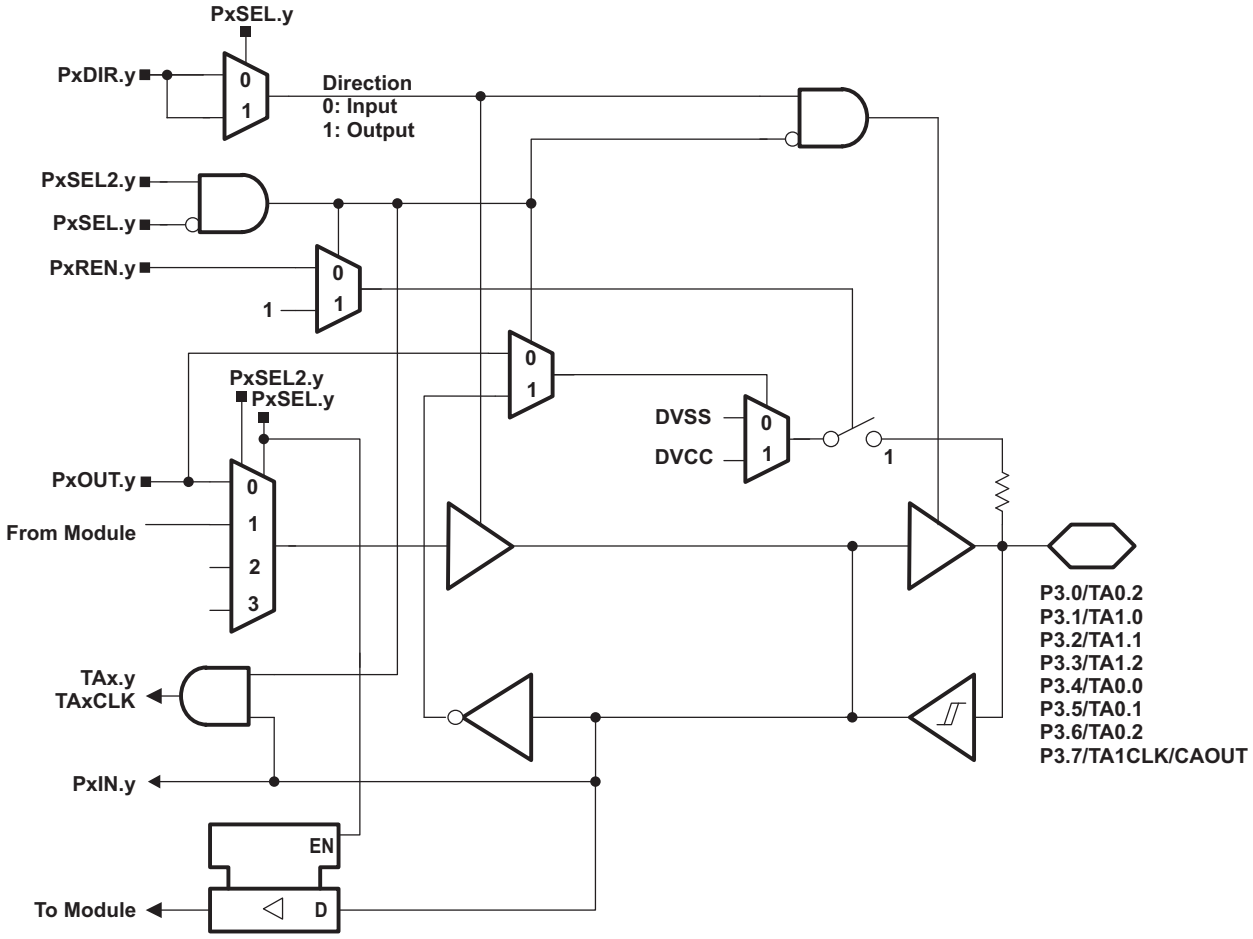


Table 23. Port P3 (P3.0 to P3.7) Pin Functions (28-Pin PW and 32-Pin RHB Packages Only)

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]		
			P3DIR.x	P3SEL.x	P3SEL2.x
P3.0/	0	P3.x (I/O)	I: 0; O: 1	0	0
TA0.2/		Timer0_A3.CCI2A	0	1	0
		Timer0_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.1/	1	P3.x (I/O)	I: 0; O: 1	0	0
TA1.0/		Timer1_A3.TA0	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.2/	2	P3.x (I/O)	I: 0; O: 1	0	0
TA1.1/		Timer1_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.3/	3	P3.x (I/O)	I: 0; O: 1	0	0
TA1.2/		Timer1_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.4/	4	P3.x (I/O)	I: 0; O: 1	0	0
TA0.0/		Timer0_A3.TA0	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.5/	5	P3.x (I/O)	I: 0; O: 1	0	0
TA0.1/		Timer0_A3.TA1	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.6/	6	P3.x (I/O)	I: 0; O: 1	0	0
TA0.2/		Timer0_A3.TA2	1	1	0
Pin Osc		Capacitive sensing	X	0	1
P3.7/	7	P3.x (I/O)	I: 0; O: 1	0	0
TA1CLK/		Timer1_A3.TACLK	0	1	0
CAOUT/		Comparator output	1	1	0
Pin Osc		Capacitive sensing	X	0	1

(1) X = don't care

REVISION HISTORY

REVISION	DESCRIPTION
SLAS735	Initial release
SLAS735A	Changed Control Bits / Signals column in Table 18 Changed Pin Name and Function columns in Table 23
SLAS735B	Changed Storage temperature range limit in Absolute Maximum Ratings Added BSL functions to P1.1 and P1.5 in Table 2. Added CAOUT information to Table 17.
SLAS735C	Changed T_{stg}, Programmed device, to -55°C to 150°C in Absolute Maximum Ratings. Changed TAG_ADC10_1 value to 0x10 in Table 10.
SLAS735D	Added AVCC (RHB package only, pin 29) to Table 2 Terminal Functions. Corrected typo in P3.7/TA1CLK/CAOUT description in Table 2. Corrected PW28 terminal assignment in Input and Output Pin Number columns in Table 13. Changed all port schematics (added buffer after PxOUT.y mux) in Port Schematics.
SLAS735E	Table 5 and Table 14, Corrected Timer_A register names.
SLAS735F	Added note on TC_{REF+} in 10-Bit ADC, Built-In Voltage Reference (MSP430G2x53 Only). Corrected signal names on Port P1 Pin Schematic: P1.4, Input/Output With Schmitt Trigger.
SLAS735G	Recommended Operating Conditions, Removed mention of USART module from f_{SYSTEM} description. Port P3 Pin Schematic: P3.0 to P3.7, Input/Output With Schmitt Trigger (28-Pin PW and 32-Pin RHB Packages Only), Added PW28 to available packages.
SLAS735H	Recommended Operating Conditions, Added test conditions for typical values. Pin-Oscillator Frequency – Ports Px, Corrected resistor value in note (1). POR, BOR, Added note (2).
SLAS735I	Throughout, Changed all variations of touch sense(1) to capacitive touch.
SLAS735J	Removed all information regarding MSP430G2113.

(1) TouchSense is a trademark of Immersion Corporation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430G2113IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2113	Samples
MSP430G2113IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2113	Samples
MSP430G2153IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2153	Samples
MSP430G2153IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2153	Samples
MSP430G2153IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2153	Samples
MSP430G2153IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2153	Samples
MSP430G2153IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2153	Samples
MSP430G2153IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2153	Samples
MSP430G2153IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2153	Samples
MSP430G2213IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2213	Samples
MSP430G2213IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2213	Samples
MSP430G2213IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2213	Samples
MSP430G2213IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2213	Samples
MSP430G2213IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2213	Samples
MSP430G2213IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2213	Samples
MSP430G2213IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2213	Samples
MSP430G2253IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2253	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430G2253IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2253	Samples
MSP430G2253IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2253	Samples
MSP430G2253IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2253	Samples
MSP430G2253IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2253	Samples
MSP430G2253IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2253	Samples
MSP430G2253IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2253	Samples
MSP430G2313IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2313	Samples
MSP430G2313IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2313	Samples
MSP430G2313IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2313	Samples
MSP430G2313IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2313	Samples
MSP430G2313IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2313	Samples
MSP430G2313IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2313	Samples
MSP430G2313IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2313	Samples
MSP430G2353IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2353	Samples
MSP430G2353IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2353	Samples
MSP430G2353IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2353	Samples
MSP430G2353IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2353	Samples
MSP430G2353IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2353	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430G2353IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2353	Samples
MSP430G2353IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2353	Samples
MSP430G2413IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2413	Samples
MSP430G2413IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2413	Samples
MSP430G2413IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2413	Samples
MSP430G2413IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2413	Samples
MSP430G2413IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2413	Samples
MSP430G2413IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2413	Samples
MSP430G2413IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2413	Samples
MSP430G2453IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2453	Samples
MSP430G2453IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2453	Samples
MSP430G2453IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2453	Samples
MSP430G2453IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2453	Samples
MSP430G2453IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2453	Samples
MSP430G2453IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2453	Samples
MSP430G2453IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2453	Samples
MSP430G2513IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2513	Samples
MSP430G2513IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2513	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430G2513IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2513	Samples
MSP430G2513IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2513	Samples
MSP430G2513IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2513	Samples
MSP430G2513IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2513	Samples
MSP430G2513IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2513	Samples
MSP430G2553IN20	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	M430G2553	Samples
MSP430G2553IPW20	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2553	Samples
MSP430G2553IPW20R	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2553	Samples
MSP430G2553IPW28	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2553	Samples
MSP430G2553IPW28R	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	430G2553	Samples
MSP430G2553IRHB32R	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2553	Samples
MSP430G2553IRHB32T	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MSP430 G2553	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF MSP430G2453, MSP430G2553 :

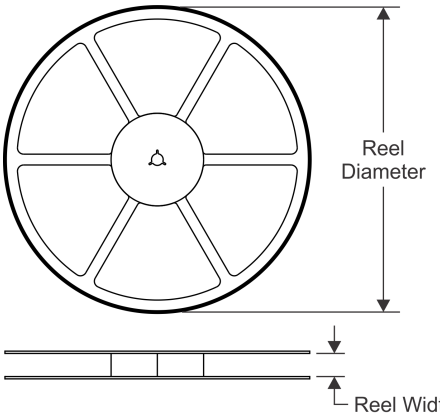
- Automotive: MSP430G2453-Q1, MSP430G2553-Q1

NOTE: Qualified Version Definitions:

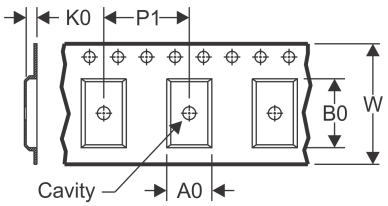
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

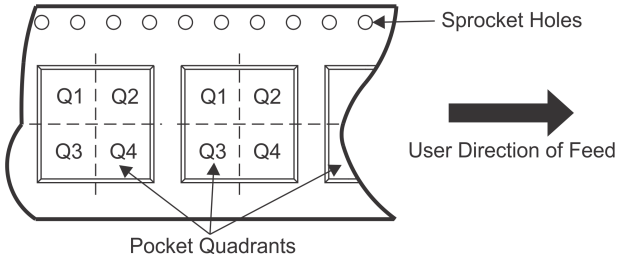


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

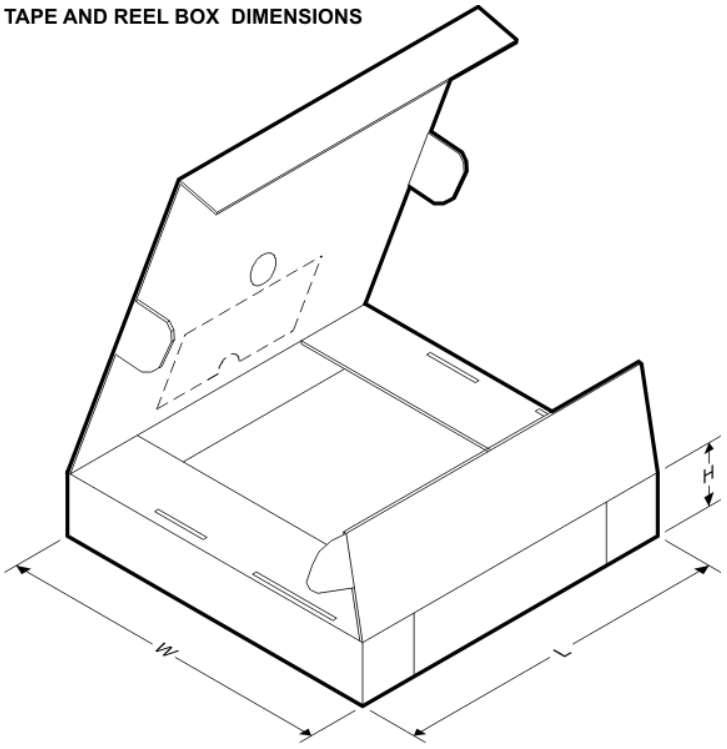


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430G2153IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2153IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2153IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2153IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2153IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2153IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2213IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2213IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2213IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2213IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2213IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2213IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2253IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2253IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2253IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2253IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2253IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2253IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430G2313IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2313IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2313IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2313IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2353IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2353IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2353IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2353IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2353IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2413IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2413IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2413IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2413IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2413IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2413IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2453IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2453IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2453IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2453IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2453IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2513IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2513IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2513IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2513IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2513IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2553IPW20R	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MSP430G2553IPW28R	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
MSP430G2553IRHB32R	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
MSP430G2553IRHB32T	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

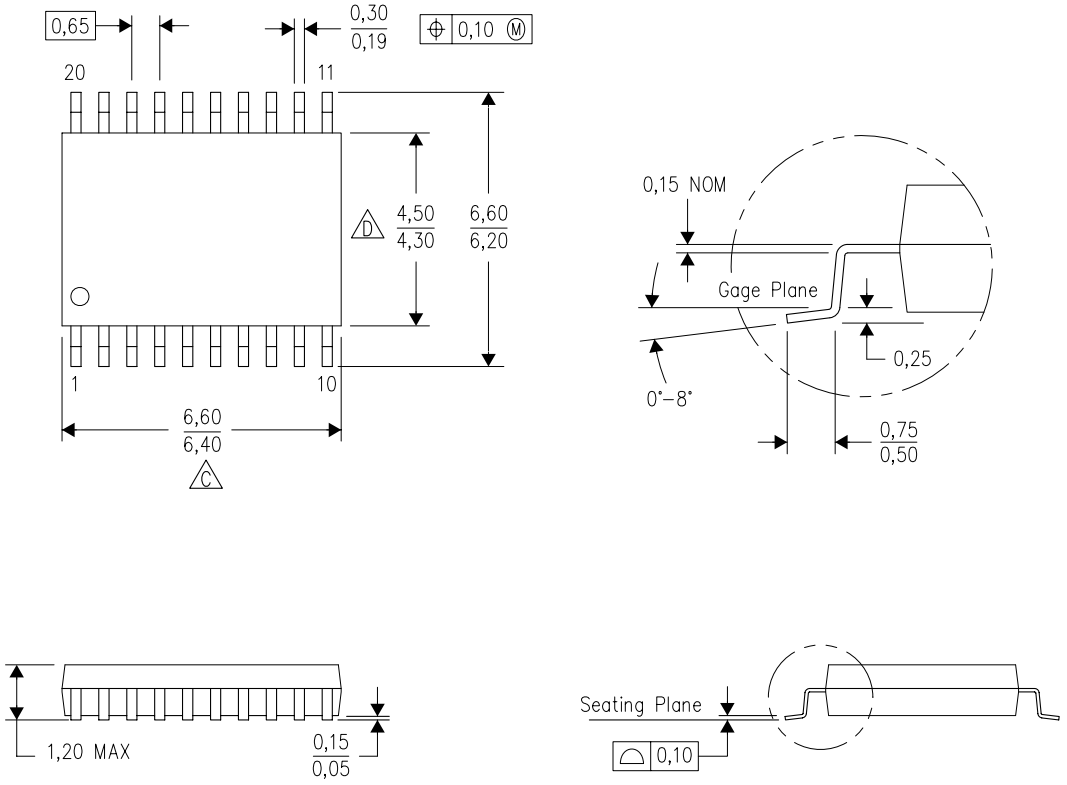


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430G2153IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2153IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2153IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2153IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2153IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2153IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2213IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2213IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2213IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2213IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2213IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2213IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2253IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2253IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2253IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2253IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2253IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2253IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2313IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2313IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430G2313IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2313IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2353IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2353IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2353IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2353IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2353IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2413IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2413IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2413IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2413IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2413IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2413IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2453IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2453IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2453IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2453IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2453IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2513IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2513IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2513IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2513IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2513IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0
MSP430G2553IPW20R	TSSOP	PW	20	2000	367.0	367.0	38.0
MSP430G2553IPW28R	TSSOP	PW	28	2000	367.0	367.0	38.0
MSP430G2553IRHB32R	VQFN	RHB	32	3000	367.0	367.0	35.0
MSP430G2553IRHB32T	VQFN	RHB	32	250	210.0	185.0	35.0

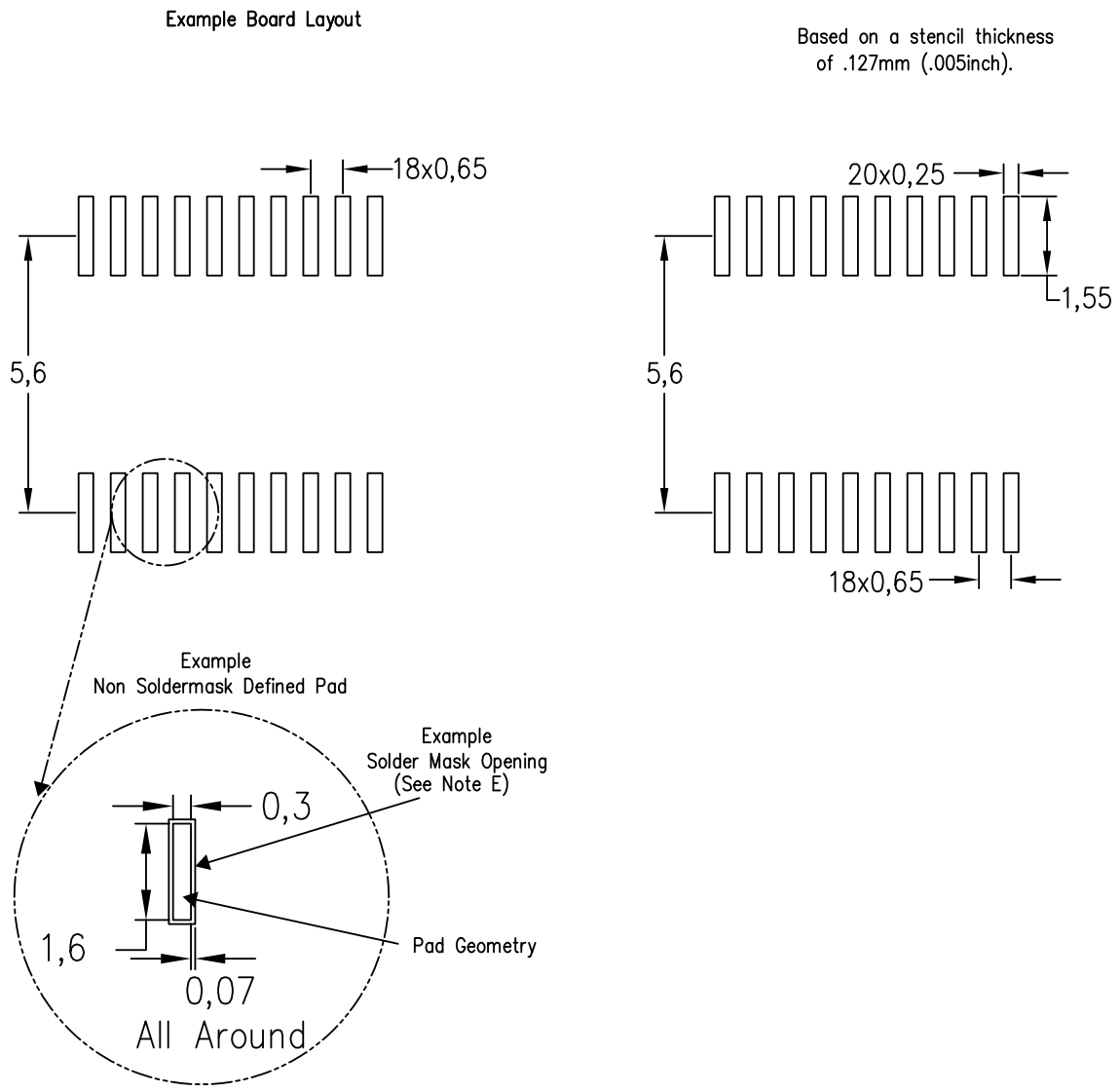
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

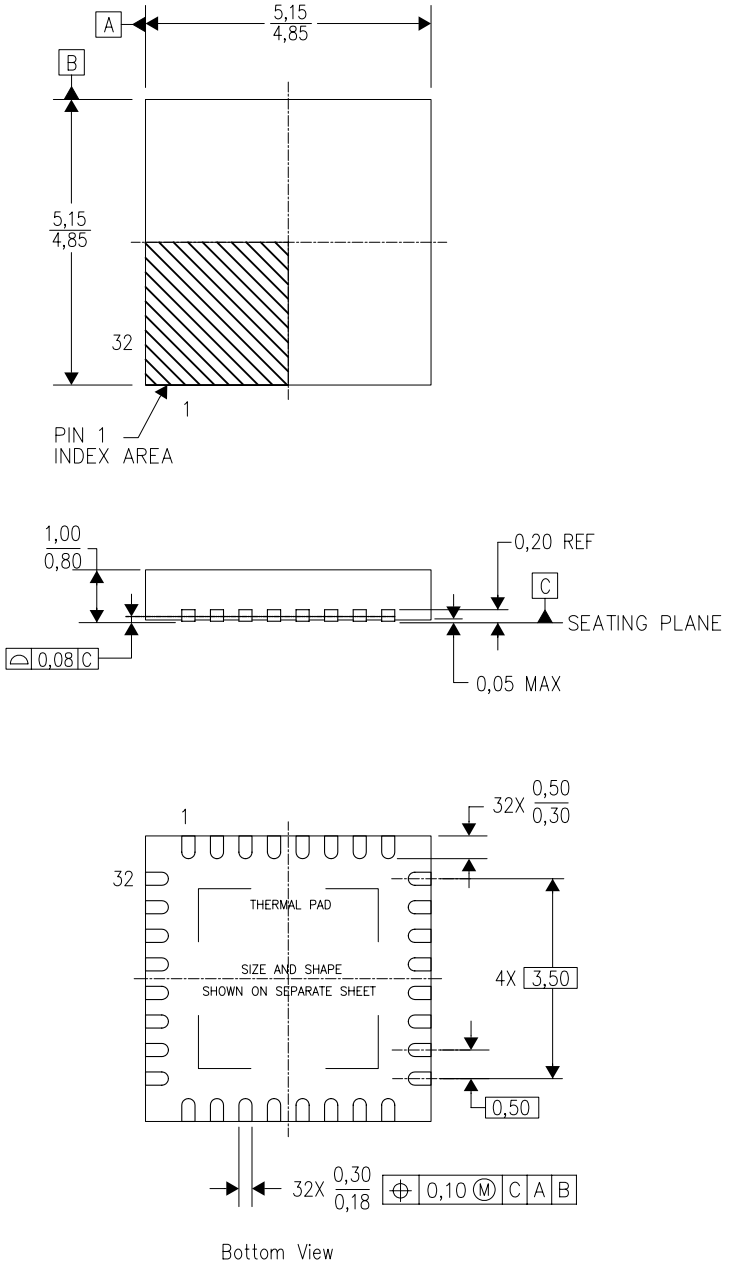
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4204326/D 06/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

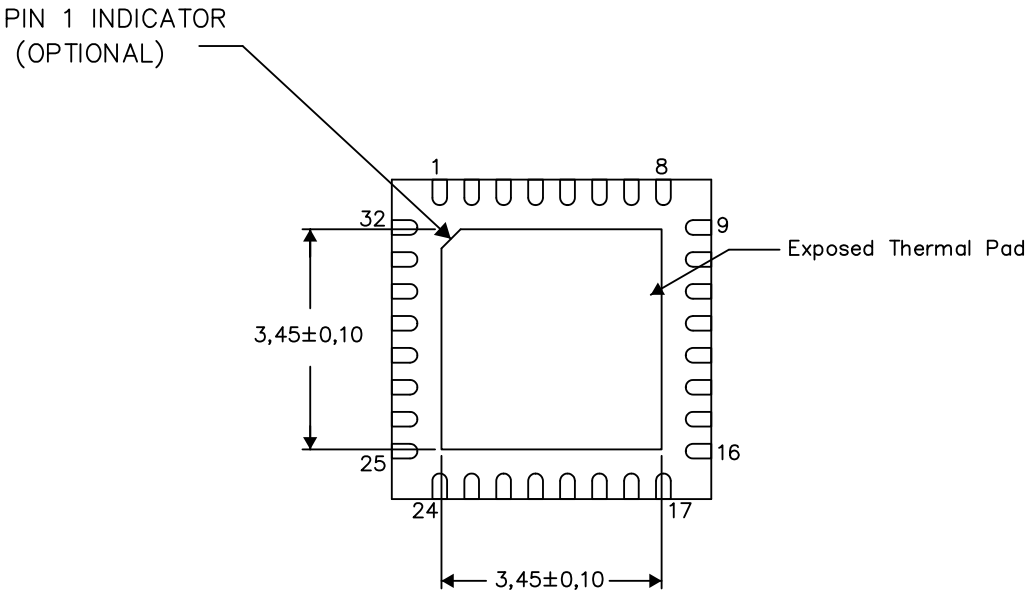
RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



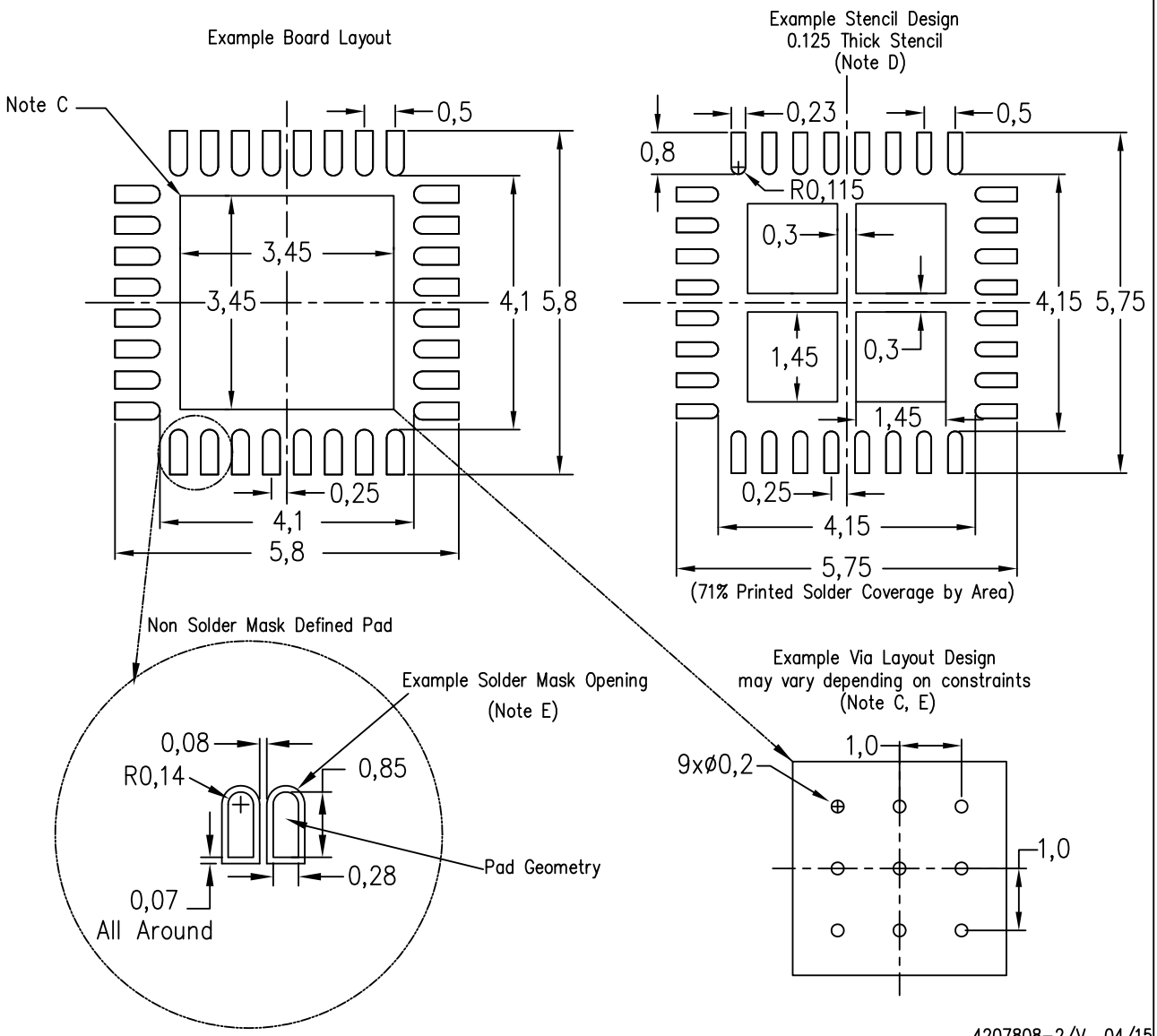
Bottom View

Exposed Thermal Pad Dimensions

4206356–2/AC 05/15

NOTE: A. All linear dimensions are in millimeters

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

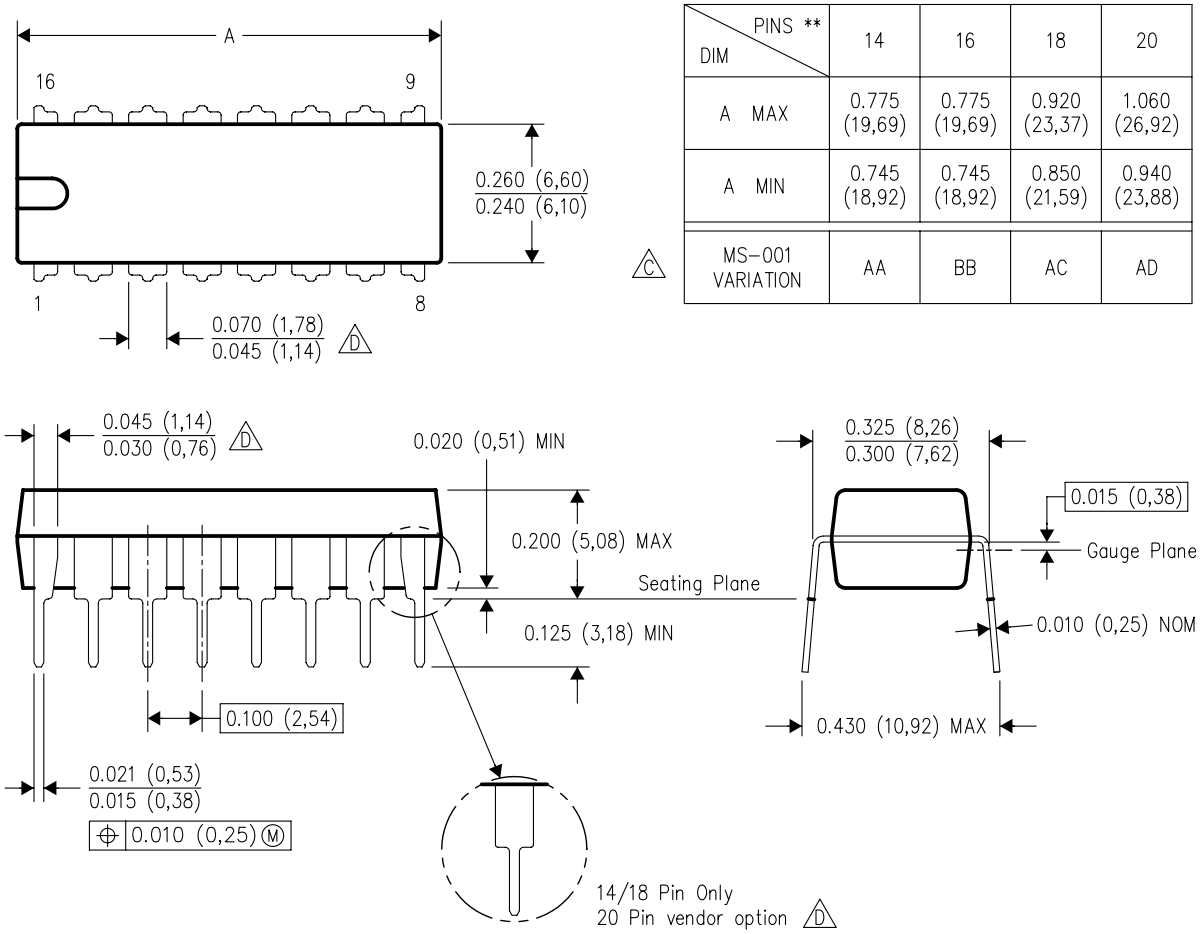


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

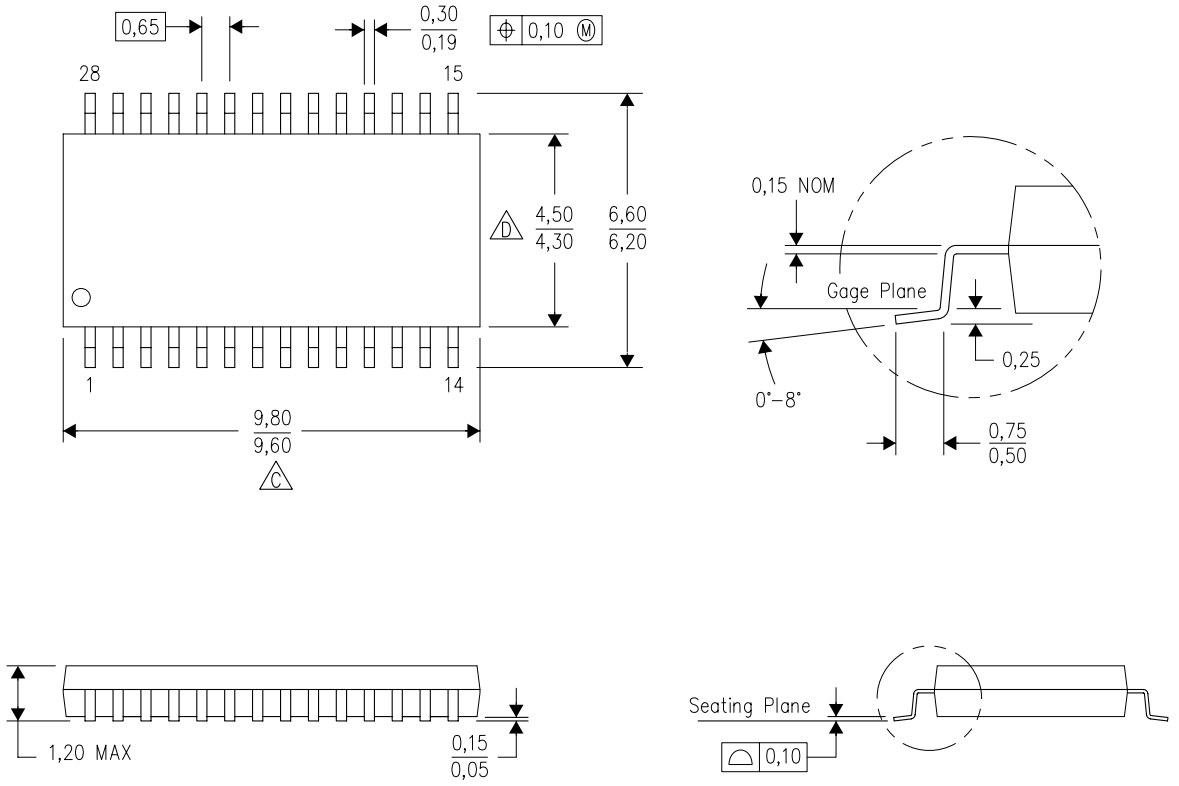


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD

4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

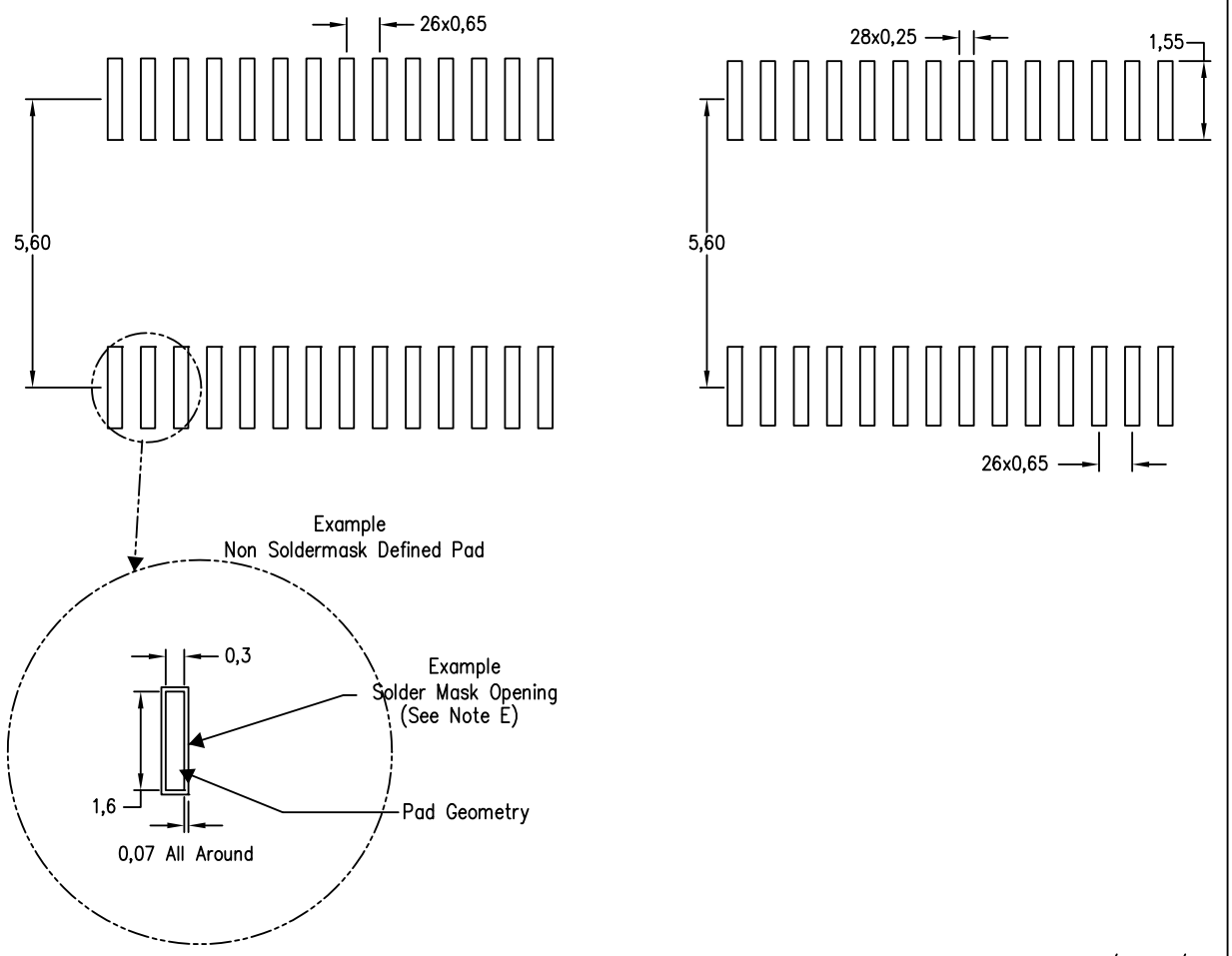
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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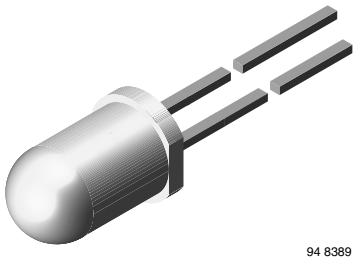
Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

High Power Infrared Emitting Diode, 940 nm, GaAlAs, MQW



94 8389

FEATURES

- Package type: leaded
- Package form: T-1¾
- Dimensions (in mm): Ø 5
- Peak wavelength: λ_p = 940 nm
- High reliability
- High radiant power
- High radiant intensity
- Angle of half intensity: φ = ± 10°
- Low forward voltage
- Suitable for high pulse current operation
- Good spectral matching with Si photodetectors
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE
GREEN (5-2008)

DESCRIPTION

TSAL6100 is an infrared, 940 nm emitting diode in GaAlAs multi quantum well (MQW) technology with high radiant power and high speed molded in a blue-gray plastic package.

APPLICATIONS

- Infrared remote control units with high power reqirements
- Free air transmission systems
- Infrared source for optical counters and card readers
- IR source for smoke detectors

PRODUCT SUMMARY

COMPONENT	I_e (mW/sr)	φ (deg)	λ_p (nm)	t_r (ns)
TSAL6100	170	± 10	940	15

Note

- Test conditions see table “Basic Characteristics”

ORDERING INFORMATION

ORDERING CODE	PACKAGING	REMARKS	PACKAGE FORM
TSAL6100	Bulk	MOQ: 4000 pcs, 4000 pcs/bulk	T-1¾

Note

- MOQ: minimum order quantity

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Reverse voltage		V_R	5	V
Forward current		I_F	100	mA
Peak forward current	t_p/T = 0.5, t_p = 100 µs	I_{FM}	200	mA
Surge forward current	t_p = 100 µs	I_{FSM}	1.5	A
Power dissipation		P_V	160	mW
Junction temperature		T_j	100	°C
Operating temperature range		T_{amb}	-40 to +85	°C
Storage temperature range		T_{stg}	-40 to +100	°C
Soldering temperature	t ≤ 5 s, 2 mm from case	T_{sd}	260	°C
Thermal resistance junction/ambient	J-STD-051, leads 7 mm soldered on PCB	R_{thJA}	230	K/W

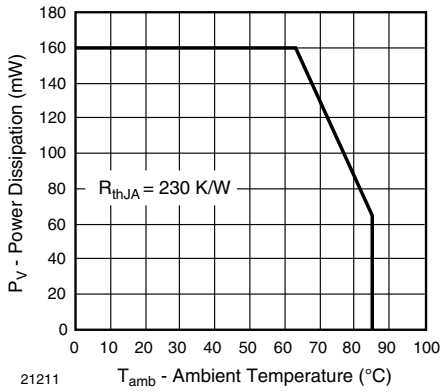


Fig. 1 - Power Dissipation Limit vs. Ambient Temperature

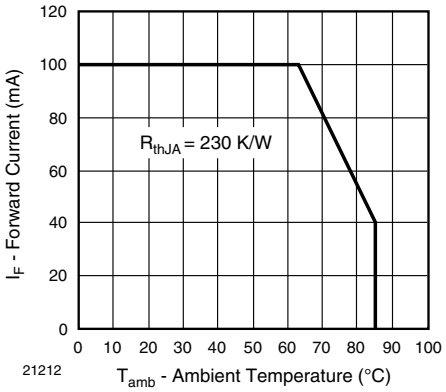


Fig. 2 - Forward Current Limit vs. Ambient Temperature

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Forward voltage	I_F = 100 mA, t_p = 20 ms	V_F		1.35	1.6	V
	I_F = 1 A, t_p = 100 µs	V_F		2.2	3	V
Temperature coefficient of V_F	I_F = 1 mA	TK_{VF}		-1.8		mV/K
Reverse current	V_R = 5 V	I_R			10	µA
Junction capacitance	V_R = 0 V, f = 1 MHz, E = 0	C_j		40		pF
Radiant intensity	I_F = 100 mA, t_p = 20 ms	I_e	80	170	400	mW/sr
	I_F = 1 A, t_p = 100 µs	I_e	650	1450		mW/sr
Radiant power	I_F = 100 mA, t_p = 20 ms	ϕ_e		40		mW
Temperature coefficient of ϕ_e	I_F = 20 mA	$TK\phi_e$		-0.6		%/K
Angle of half intensity		φ		± 10		deg
Peak wavelength	I_F = 100 mA	λ_p		940		nm
Spectral bandwidth	I_F = 100 mA	$\Delta\lambda$		30		nm
Temperature coefficient of λ_p	I_F = 100 mA	$TK\lambda_p$		0.2		nm/K
Rise time	I_F = 100 mA	t_r		15		ns
Fall time	I_F = 100 mA	t_f		15		ns

BASIC CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

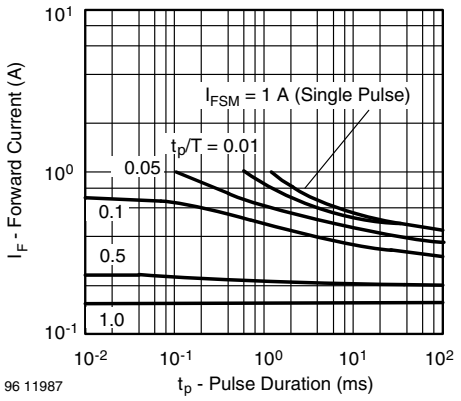


Fig. 3 - Pulse Forward Current vs. Pulse Duration

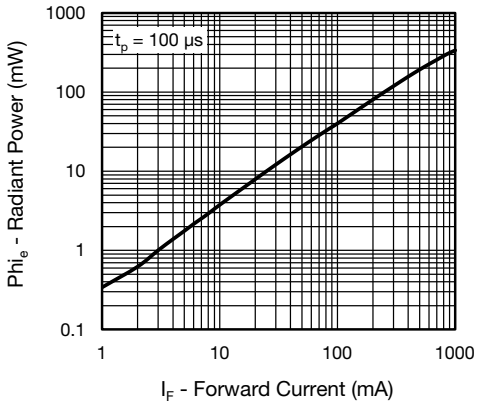


Fig. 6 - Radiant Power vs. Forward Current

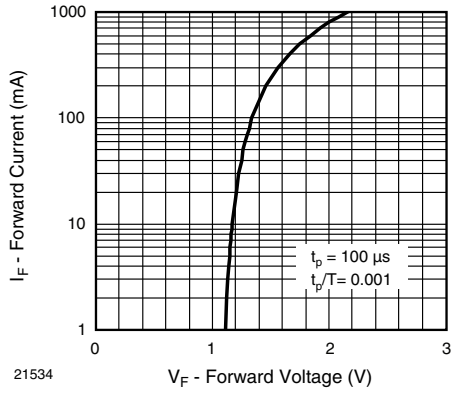


Fig. 4 - Forward Current vs. Forward Voltage

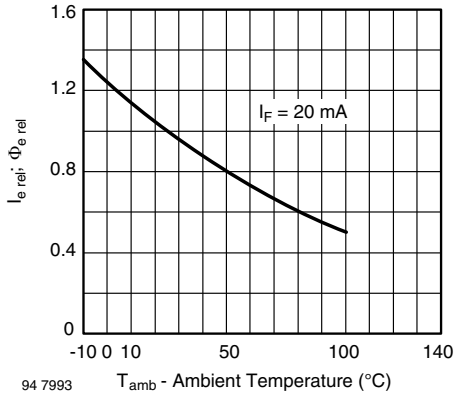


Fig. 7 - Rel. Radiant Intensity/Power vs. Ambient Temperature

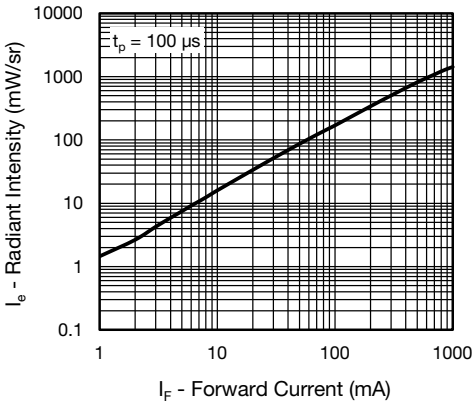


Fig. 5 - Radiant Intensity vs. Forward Current

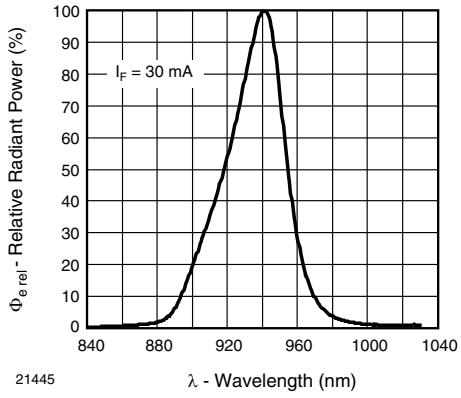


Fig. 8 - Relative Radiant Power vs. Wavelength

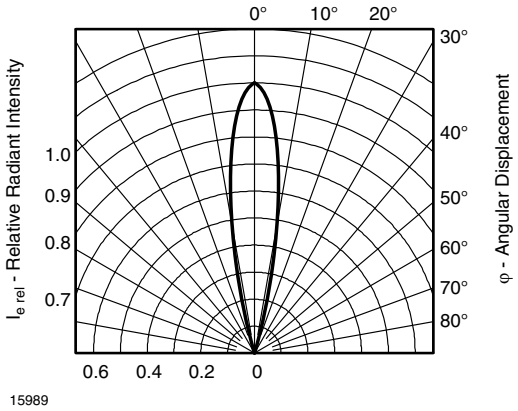
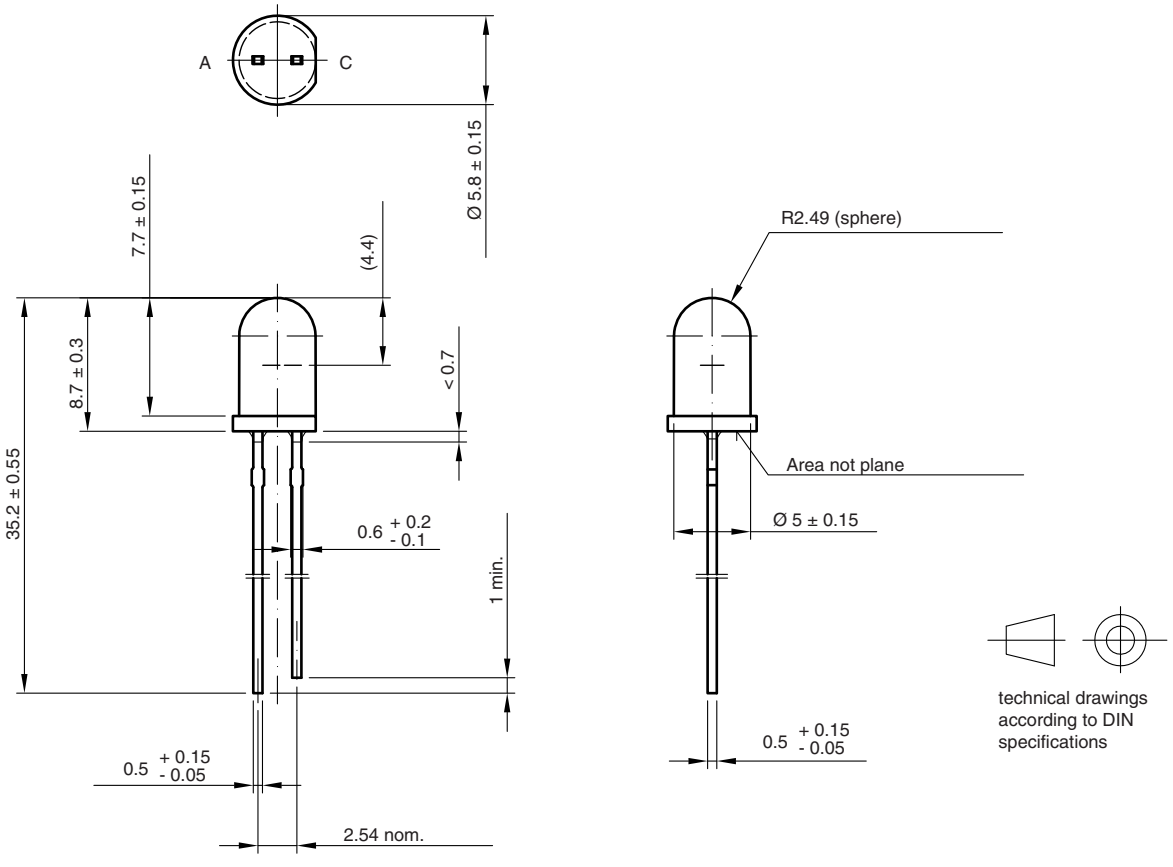


Fig. 9 - Relative Radiant Intensity vs. Angular Displacement

PACKAGE DIMENSIONS in millimeters



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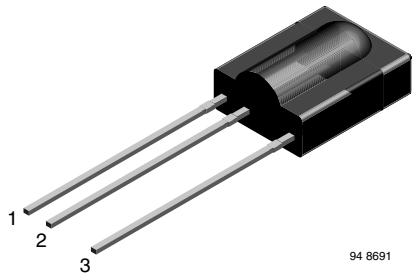
IR Receiver Modules for Remote Control Systems



FEATURES

- Very low supply current
- Photo detector and preamplifier in one package
- Internal filter for PCM frequency
- Supply voltage: 2.5 V to 5.5 V
- Improved immunity against ambient light
- Insensitive to supply voltage ripple and noise
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

e3

RoHS COMPLIANT

HALOGEN FREE

GREEN (5-2008)

MECHANICAL DATA

Pinning:

1 = GND, 2 = V_S, 3 = OUT

DESCRIPTION

The TSOP312.., TSOP314..series are miniaturized IR receiver modules for infrared remote control systems. A PIN diode and a preamplifier are assembled on a leadframe, the epoxy package contains an IR filter.

The demodulated output signal can be directly connected to a microprocessor for decoding.

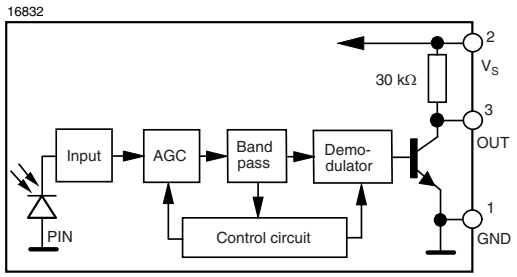
The TSOP314.. series devices are optimized to suppress almost all spurious pulses from energy saving lamps like CFLs. The AGC4 used in the TSOP314.. may suppress some data signals. The TSOP312.. series are provided primarily for compatibility with old AGC2 designs. New designs should prefer the TSOP314.. series containing the newer AGC4.

These components have not been qualified according to automotive specifications.

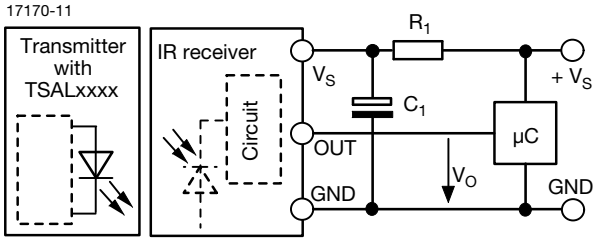
PARTS TABLE

AGC		LEGACY, FOR LONG BURST REMOTE CONTROLS (AGC2)	RECOMMENDED FOR LONG BURST CODES (AGC4)
Carrier frequency	30 kHz	TSOP31230	TSOP31430
	33 kHz	TSOP31233	TSOP31433
	36 kHz	TSOP31236	TSOP31436 (1)(2)(3)
	38 kHz	TSOP31238	TSOP31438 (4)(5)
	40 kHz	TSOP31240	TSOP31440
	56 kHz	TSOP31256	TSOP31456 (6)(7)
Package		Cast	
Pinning		1 = GND, 2 = V_S, 3 = OUT	
Dimensions (mm)		10.0 W x 12.5 H x 5.8 D	
Mounting		Leaded	
Application		Remote control	
Best remote control code		(1) RC-5 (2) RC-6 (3) Panasonic (4) NEC (5) Sharp (6) r-step (7) Thomson RCA	

BLOCK DIAGRAM



APPLICATION CIRCUIT



R_1 and C_1 recommended to reduce supply ripple for V_S < 2.8 V

ABSOLUTE MAXIMUM RATINGS

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Supply voltage (pin 2)		V_S	-0.3 to +6.0	V
Supply current (pin 2)		I_S	3	mA
Output voltage (pin 3)		V_O	-0.3 to (V_S + 0.3)	V
Output current (pin 3)		I_O	5	mA
Junction temperature		T_j	100	°C
Storage temperature range		T_{stg}	-25 to +85	°C
Operating temperature range		T_{amb}	-25 to +85	°C
Power consumption	$T_{amb} \leq 85$ °C	P_{tot}	10	mW
Soldering temperature	t ≤ 10 s, 1 mm from case	T_{sd}	260	°C

Note

- Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

ELECTRICAL AND OPTICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply current (pin 2)	E_v = 0, V_S = 3.3 V	I_{SD}	0.27	0.35	0.45	mA
	E_v = 40 klx, sunlight	I_{SH}	-	0.45	-	mA
Supply voltage		V_S	2.5	-	5.5	V
Transmission distance	E_v = 0, test signal see Fig. 1, IR diode TSAL6200, I_F = 200 mA	d	-	45	-	m
Output voltage low (pin 3)	I_{OSL} = 0.5 mA, E_e = 0.7 mW/m², test signal see Fig. 1	V_{OSL}	-	-	100	mV
Minimum irradiance	Pulse width tolerance: $t_{pi} - 5/f_o < t_{po} < t_{pi} + 6/f_o$, test signal see Fig. 1	$E_{e\ min.}$	-	0.12	0.25	mW/m²
Maximum irradiance	$t_{pi} - 5/f_o < t_{po} < t_{pi} + 6/f_o$, test signal see Fig. 1	$E_{e\ max.}$	30	-	-	W/m²
Directivity	Angle of half transmission distance	$\varphi_{1/2}$	-	± 45	-	deg

TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

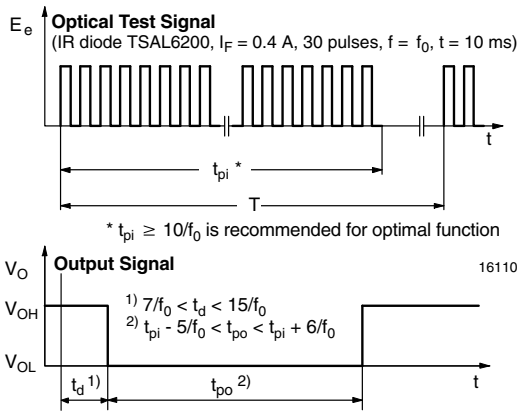


Fig. 1 - Output Active Low

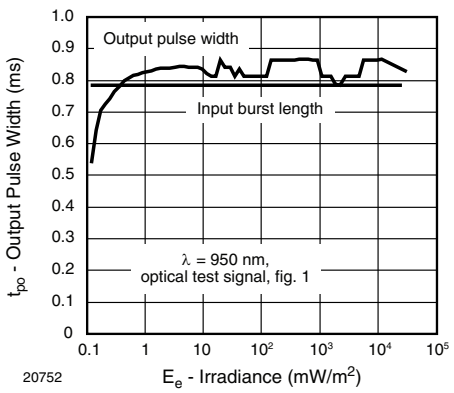


Fig. 2 - Pulse Length and Sensitivity in Dark Ambient

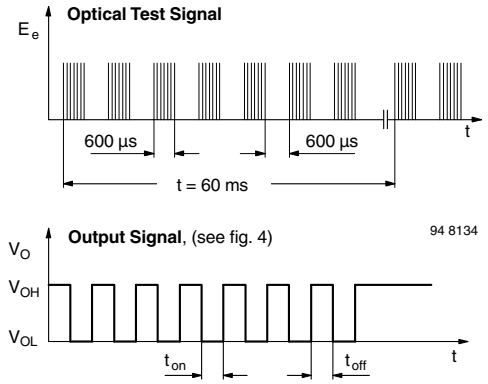


Fig. 3 - Output Function

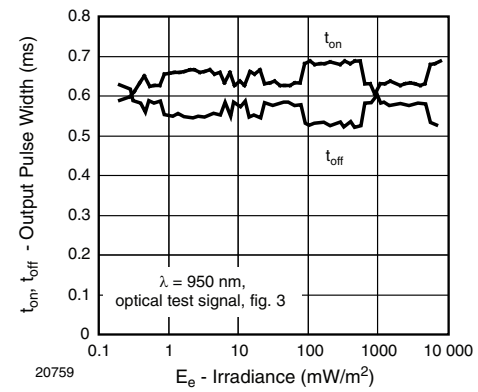


Fig. 4 - Output Pulse Diagram

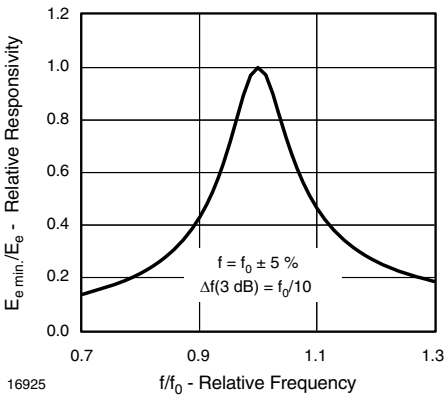


Fig. 5 - Frequency Dependence of Responsivity

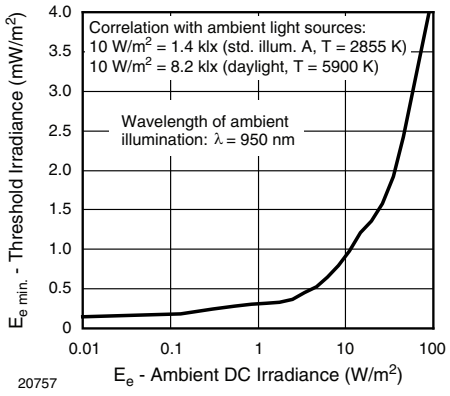


Fig. 6 - Sensitivity in Bright Ambient

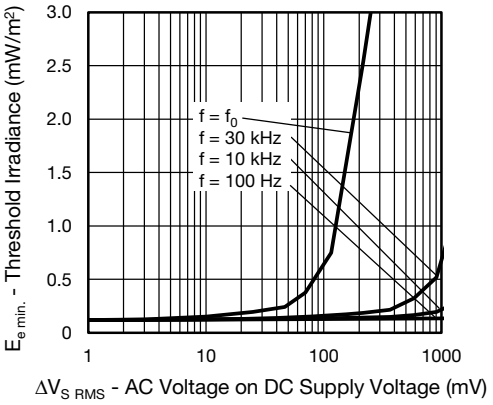


Fig. 7 - Sensitivity vs. Supply Voltage Disturbances

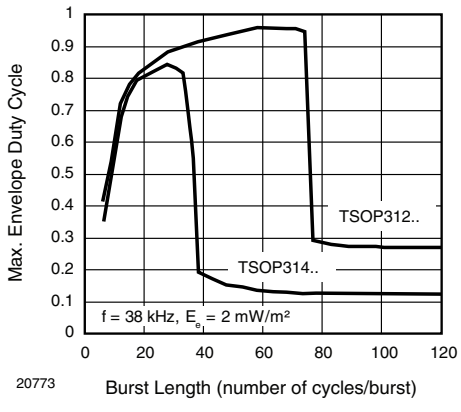


Fig. 8 - Maximum Envelope Duty Cycle vs. Burst Length

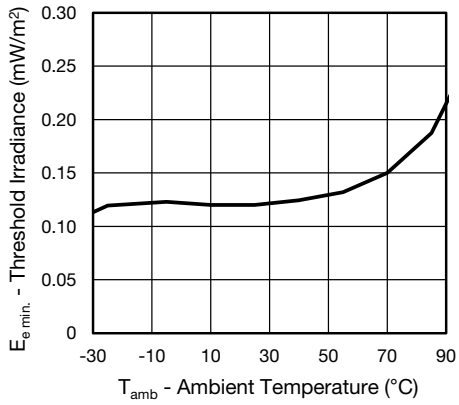


Fig. 9 - Sensitivity vs. Ambient Temperature

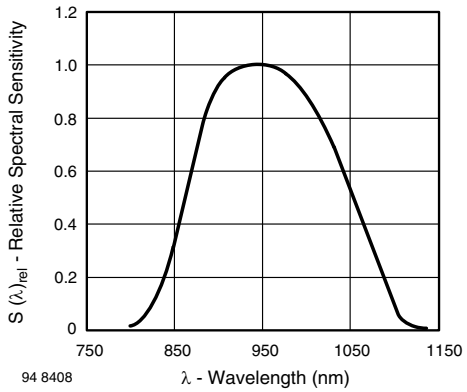


Fig. 10 - Relative Spectral Sensitivity vs. Wavelength

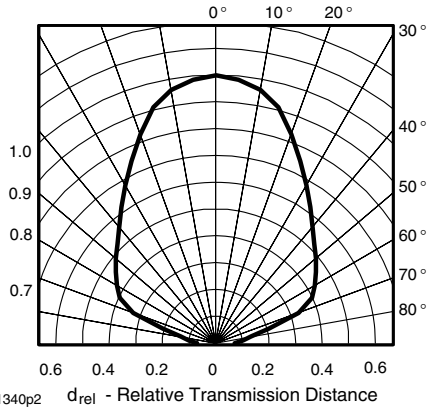


Fig. 11 - Horizontal Directivity

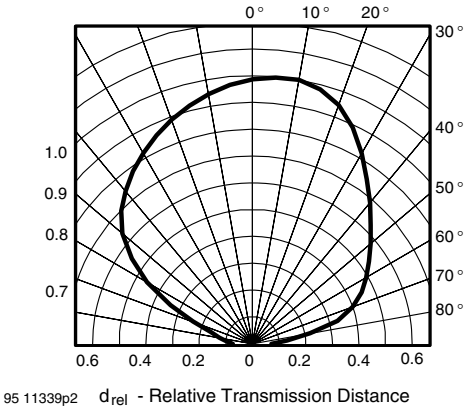


Fig. 12 - Vertical Directivity

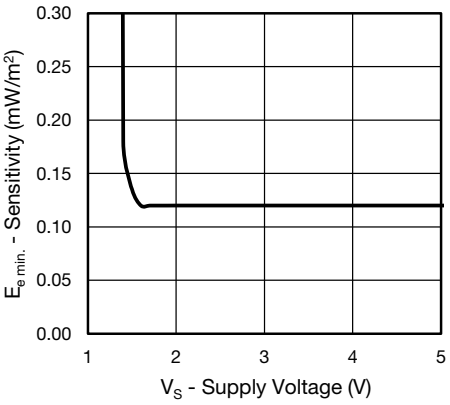


Fig. 13 - Sensitivity vs. Supply Voltage

SUITABLE DATA FORMAT

This series is designed to suppress spurious output pulses due to noise or disturbance signals. The devices can distinguish data signals from noise due to differences in frequency, burst length, and envelope duty cycle. The data signal should be close to the device's band-pass center frequency (e.g. 38 kHz) and fulfill the conditions in the table below.

When a data signal is applied to the product in the presence of a disturbance, the sensitivity of the receiver is automatically reduced by the AGC to insure that no spurious pulses are present at the receiver's output. Some examples which are suppressed are:

- DC light (e.g. from tungsten bulbs sunlight)
- Continuous signals at any frequency
- Strongly or weakly modulated patterns from fluorescent lamps with electronic ballasts (see Fig. 14 or Fig. 15).

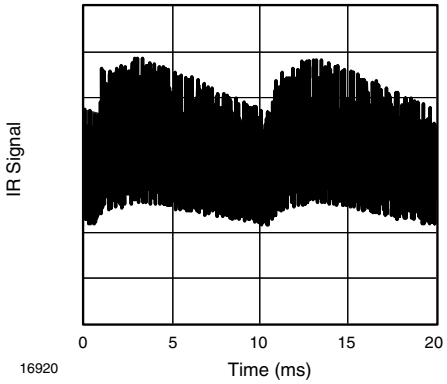


Fig. 14 - IR Disturbance from Fluorescent Lamp with Low Modulation

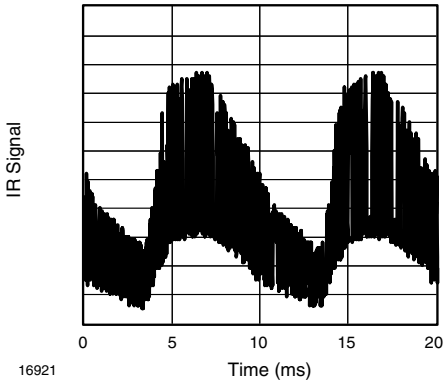


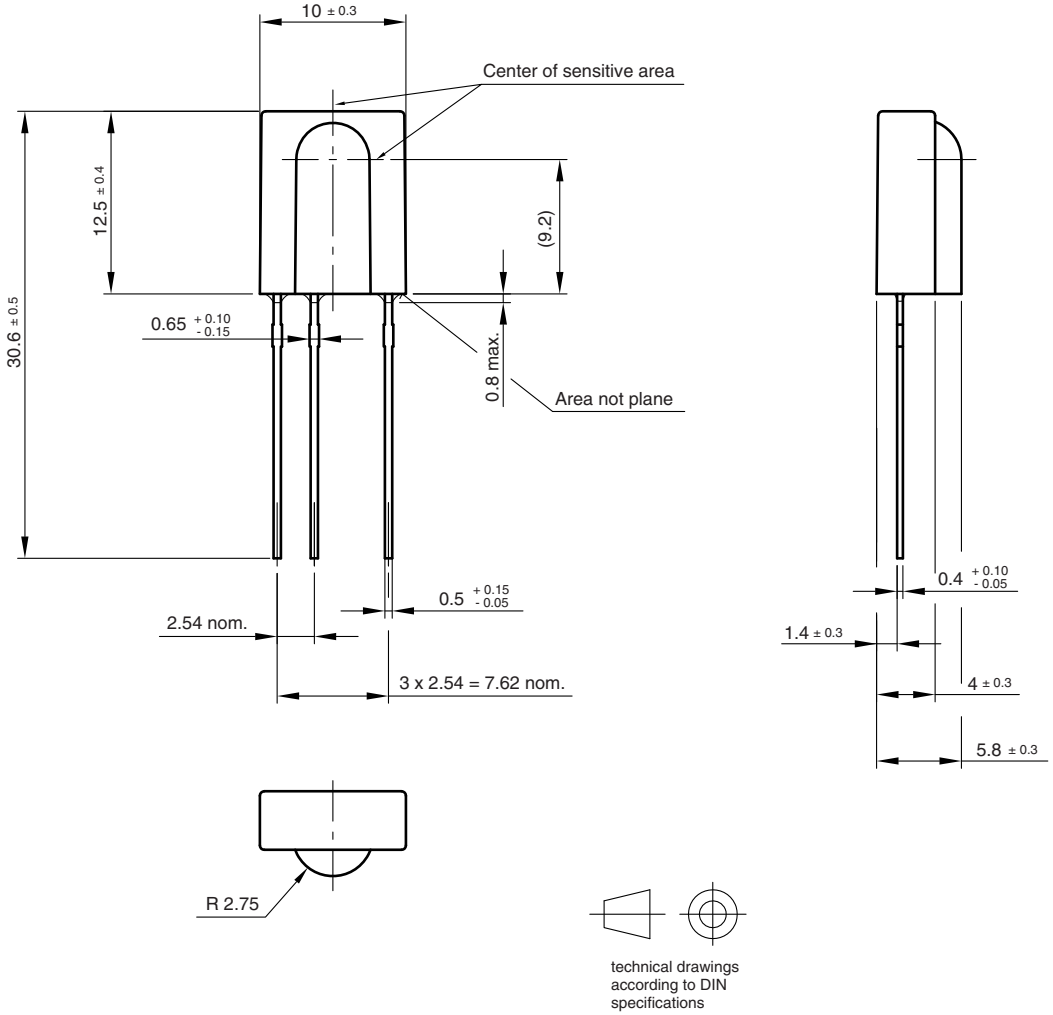
Fig. 15 - IR Disturbance from Fluorescent Lamp with High Modulation

	TSOP312..	TSOP314..
Minimum burst length	10 cycles/burst	10 cycles/burst
After each burst of length a minimum gap time is required of	10 to 70 cycles ≥ 10 cycles	10 to 35 cycles ≥ 10 cycles
For bursts greater than a minimum gap time in the data stream is needed of	70 cycles > 4 x burst length	35 cycles > 10 x burst length
Maximum number of continuous short bursts/second	1800	1500
NEC code	Yes	Preferred
RC5/RC6 code	Yes	Preferred
Thomson 56 kHz code	Yes	Preferred
Sharp code	Yes	Preferred
Suppression of interference from fluorescent lamps	Mild disturbance patterns are suppressed (example: signal pattern of Fig. 14)	Complex and critical disturbance patterns are suppressed (example: signal pattern of Fig. 15 or highly dimmed LCDs)

Notes

- For data formats with short bursts please see the datasheet for TSOP311.., TSOP313..
- For SIRCS 15 and 20 bit, Sony 12 bit IR codes, please see the datasheet for TSOP31S40

PACKAGE DIMENSIONS in millimeters



Drawing-No.: 6.550-5095.01-4

Issue: 20; 15.03.10

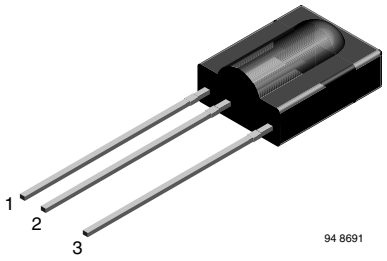
96 12116

Cast IR Receiver Packaging Options

IR Receiver Modules for Remote Control Systems

Vishay offers stock Cast IR Receivers in three different packages:

- Loose packed in tubes and mounted on tape for reel or ammopack
- Vishay IR receiver with plastic holders are packed in plastic tubes



FEATURES

- Material categorization:
  For definitions of compliance please see www.vishay.com/doc?99912

Pb-free

e3

RoHS COMPLIANT

GREEN (5-2008)

AVAILABLE FOR

- TSOP312..
- TSOP311..
- TSOP12...
- TSOP11...
- TSOP13...
- TSOP313..
- TSOP314..
- TSOP315..
- TSMP1138

LOOSE PACKED IN TUBE

ORDERING INFORMATION

T	S	d	P	d	d	d	d	d

2 or 3 digit product series — 2 digit frequency

O = for IR receiver applications
M = for repeater/learning applications

Note

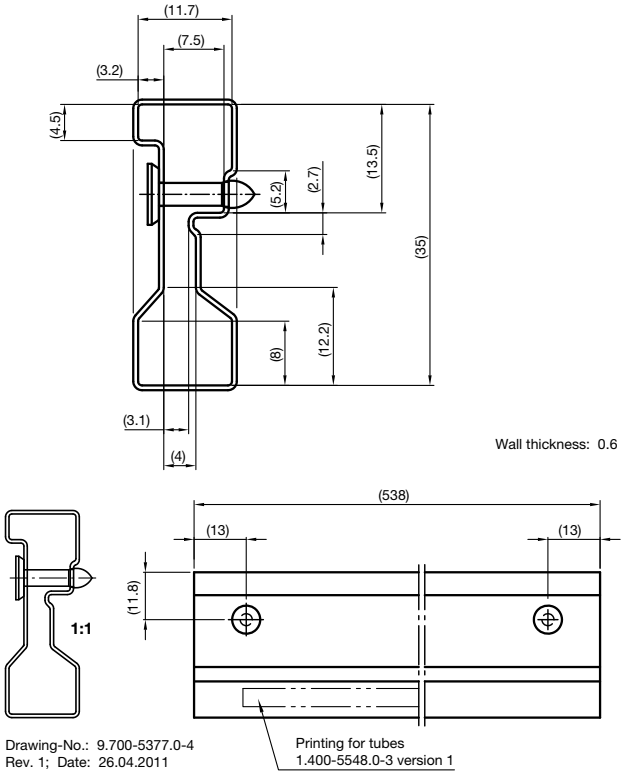
- d = “digit”, please consult the list of available devices create a valid part number.

EXAMPLE: TSOP1238

PACKAGING QUANTITY

- 50 pieces per tube
- 20 tubes per carton

PACKAGING DIMENSIONS in millimeters

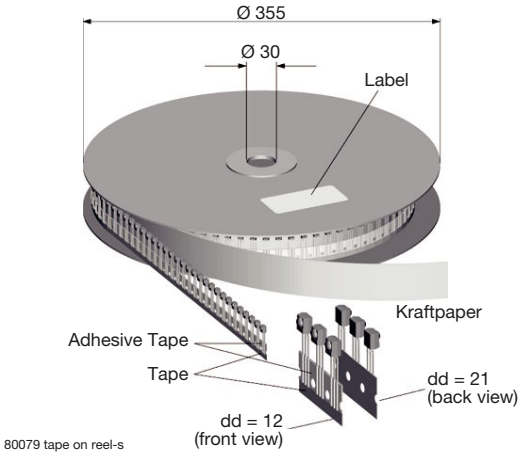


TAPE AND REEL/AMMOPACK

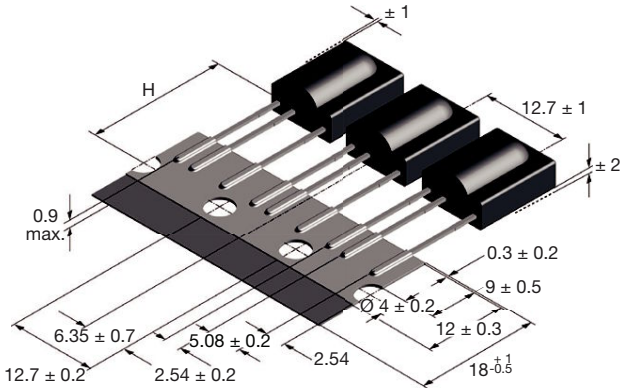
Up to 3 consecutive components may be missing if the gap is followed by at least 6 components. A maximum of 0.5 % of the components per reel quantity may be missing. At least 5 empty positions are present at the start and the end of the tape to enable insertion.

Tensile strength of the tape: > 15 N

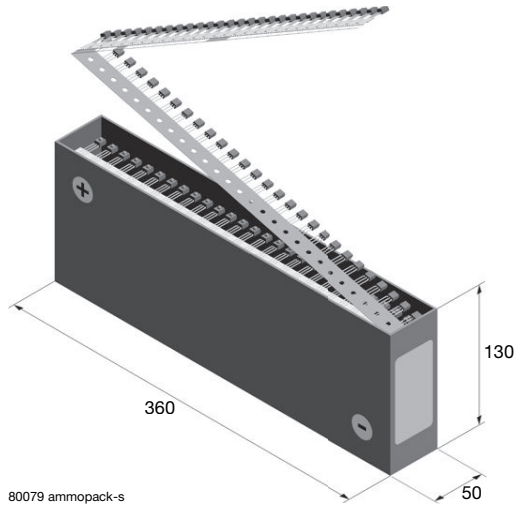
Pulling force in the plane of the tape, at right angles to the reel: > 5 N



80079 tape on reel-s



80079 tape-s



80079 ammopack-s

VERSION	DIMENSION "H"
BS	20 ± 0.5
PS	23.3 ± 0.5
OS	26 ± 0.5

ORDERING INFORMATION

T	S	d	P	d	d	d	d	d	S	S	1	d	d	d	d	Z

- T S d P: O = for IR receiver applications; M = for repeater/learning applications
- d d d d d: 2 or 3 digit product series; 2 digit frequency
- S S 1: SS1 for T and R, bulk or ammopack
- d d: dd = BS, PS, or OS
- d d: Tape and reel
- d d: dd = 12 or 21
- Z: Ammopack

Note

- d = "digit", please consult the list of available devices create a valid part number.

EXAMPLE: TSOP1238SS1BS12

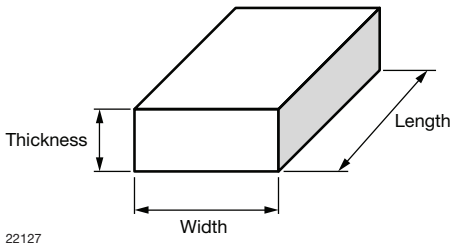
TSOP1238SS1BS12Z

PACKAGING QUANTITY

- 1000 pieces per reel
- 1000 pieces per ammopack

OUTER PACKAGING

CARTON BOX DIMENSIONS in millimeters



KINDS OF CARTON BOX	THICKNESS	WIDTH	LENGTH
Packaging Plastic Tubes (Normal/auxiliary devices)	82	152	564
Tape and Reel Box (Taping in reels)	400	310	410
Ammo-Box (Zigzag taping)	50	130	350

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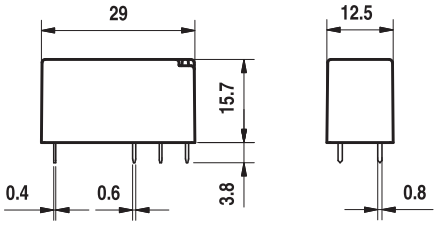
Características

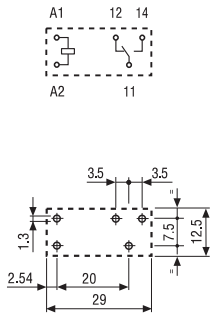
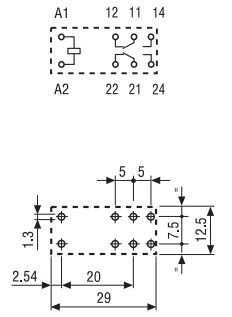
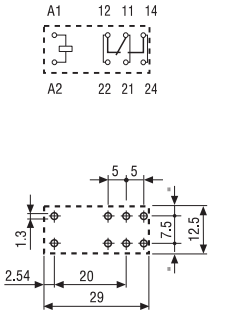
1 o 2 contactos conmutados
Bajo perfil (altura 15.7 mm)
41.31 - 1 contacto 12 A (reticulado 3.5 mm)
41.52 - 2 contactos 8 A (reticulado 5 mm)
41.61 - 1 contacto 16 A (reticulado 5 mm)

Montaje en circuito impreso
- directo o en zócalo
Montaje en carril de 35 mm (EN 60715)
- en zócalos con bornes de jaula o de conexión rápida

- Bobina DC - 400 mW
- 8 mm, 6 kV (1.2/50 µs) entre bobina y contactos
- Contactos sin Cadmio
- Estanco al flux: RT II estándar, (disponible en versión RT III)



Para Cargas de Motores y "Pilot Duty" Homologadas por UL ver "Información Técnica General" página V

	41.31	41.52	41.61
			
	• Reticulado 3.5 mm • 1 contacto 12 A • Montaje en circuito impreso o en zócalo serie 95	• Reticulado 5 mm • 2 contactos 8 A • Montaje en circuito impreso o en zócalo serie 95	• Reticulado 5 mm • 1 contacto 16 A • Montaje en circuito impreso o en zócalo serie 95
			
	Vista parte inferior	Vista parte inferior	Vista parte inferior
Características de los contactos			
Configuración de contactos	1 contacto conmutado	2 contactos conmutados	1 contacto conmutado
Corriente nominal/Máx. corriente instantánea A	12/25	8/15	16/30
Tensión nominal/Máx. tensión de conmutación V AC	250/400	250/400	250/400
Carga nominal en AC1 VA	3000	2000	4000
Carga nominal en AC15 (230 V AC) VA	600	400	750
Motor monofásico (230 V AC) kW	0.5	0.3	0.5
Capacidad de ruptura en DC1: 30/110/220 V A	12/0.3/0.12	8/0.3/0.12	16/0.3/0.12
Carga mínima conmutable mW (V/mA)	300 (5/5)	300 (5/5)	300 (5/5)
Material estándar de los contactos	AgNi	AgNi	AgNi
Características de la bobina			
Tensión nominal V AC (50/60 Hz)	—	—	—
de alimentación (U_N) V DC	12 - 24 - 48 - 60 - 110	12 - 24 - 48 - 60 - 110	12 - 24 - 48 - 60 - 110
Potencia nominal en AC/DC VA (50 Hz)/W	—/0.4	—/0.4	—/0.4
Campo de funcionamiento AC	—	—	—
DC	(0.7...1.5)U_N	(0.7...1.5)U_N	(0.7...1.5)U_N
Tensión de mantenimiento AC/DC	—/0.4U_N	—/0.4 U_N	—/0.4 U_N
Tensión de desconexión AC/DC	—/0.1U_N	—/0.1 U_N	—/0.1 U_N
Características generales			
Vida útil mecánica AC/DC ciclos	—/30·10^6	—/30·10^6	—/30·10^6
Vida útil eléctrica con carga nominal en AC1 ciclos	150 · 10^3	80 · 10^3	70 · 10^3
Tiempo de respuesta: conexión/desconexión ms	5/4	5/4	5/4
Aislamiento entre bobina y contactos (1.2/50 µs) kV	6 (8 mm)	6 (8 mm)	6 (8 mm)
Rigidez dieléctrica entre contactos abiertos V AC	1000	1000	1000
Temperatura ambiente °C	–40...+85	–40...+85	–40...+85
Categoría de protección	RT II	RT II	RT II
Homologaciones (según los tipos)			

Serie 41 - Mini-relé de estado sólido (SSR) para circuito impreso 3 - 5 A

Características

Relé de estado sólido

Montaje en circuito impreso
- directo o en zócalo
Montaje en carril de 35 mm (EN 60715)
- en zócalos con bornes de jaula o de conexión rápida

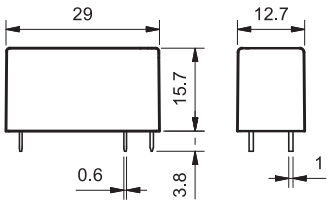
- Circuito singular de salida disponible en:
  - 5 A 24 V DC
  - 3 A 240 V AC
- Silencioso, elevada velocidad de conmutación y vida eléctrica
- Bajo perfil (15.7 mm)
- Lavable: RT III
- Aislamiento entre entrada/salida 2500 V

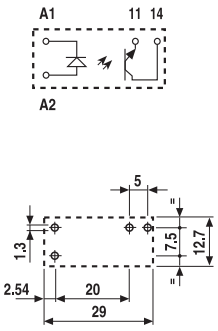
41.81 - 9024

- Corriente de conmutación 5 A, 24 V DC
- Montaje en circuito impreso o en zócalo serie 93

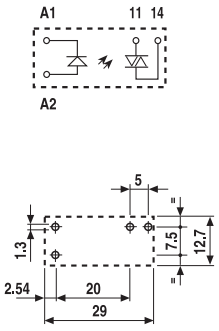
41.81 - 8240

- Corriente de conmutación 3 A, 240 V AC
- Conexión al paso por cero
- Montaje en circuito impreso o en zócalo serie 93





Vista parte inferior



Vista parte inferior

Circuito de salida					
Configuración de contactos		1 NA		1 NA	
Corriente nominal/Máx. corriente instantánea (100 µs)	A	5/40		3/40	
Tensión nominal/Tensión máxima de bloqueo	V	(24/35)DC		(240/275)AC	
Tensión de conmutación	V	(1.5...35)DC		(12...275)AC	
Intensidad mínima de conmutación	mA	1		50	
Máxima corriente residual en salida "OFF"	mA	0.01		1	
Máxima caida de tensión en salida "ON"	V	0.3		1.1	
Circuito de entrada					
Tensión nominal de alimentación	V DC	12	24	12	24
Campo de funcionamiento	V DC	8...17	14...32	8...17	14...32
Absorbimiento nominal	mA	5.5	9	8.8	9
Tensión de desconexión	V DC	4	9	4	9
Impedancia	Ω	1550	2600	1030	2600
Características generales					
Tiempo de respuesta: ON/OFF	ms	0.05/0.25		10/10	
Rigidez dieléctrica entre entrada/salida	V	2500		2500	
Temperatura ambiente	°C	–20...+60		–20...+60	
Categoría de protección		RT III		RT III	
Homologaciones (según los tipos)					

Codificación

Relé electromecánico (EMR)

Ejemplo: serie 41, mini-relé para circuito impreso, 2 contactos conmutados, tensión bobina 24 V DC.

								A	B	C	D		
4	1	.	5	2	.	9	.	0	2	4	.	0	0	1	0

Serie

Tipo
3 = Circuito impreso - reticulado 3.5 mm
5 = Circuito impreso - reticulado 5 mm
6 = Circuito impreso - reticulado 5 mm

Número contactos
1 = 1 contacto conmutado para
41.31, 12 A
41.61, 16 A
2 = 2 contactos conmutados para
41.52, 8 A

Versión de la bobina
9 = DC

Tensión nominal de la bobina
Ver características de la bobina

A: Material des contactos
0 = Estándar AgNi
4 = $AgSnO_2$
5 = AgNi + Au (5 µm)

B: Circuito de contactos
0 = Contacto conmutado
3 = NA

C: Variantes
1 = Ninguna

D: Versiones especiales
0 = Estanco al flux (RT II)
1 = Lavable (RT III)

Selección de características y opciones: sólo son posibles combinaciones en la misma linea.
En **negrita** se muestran las opciones preferentes y con mejor disponibilidad.

Tipo	Versión de bobina	A	B	C	D
41.31	DC	**0** - 4 - 5	**0** - 3	**1**	**0** - 1
41.52	DC	**0** - 5	**0** - 3	**1**	**0** - 1
41.61	DC	**0** - 4	**0** - 3	**1**	**0** - 1

Relé de estado sólido (SSR)

Ejemplo: serie 41, relé de estado sólido (SSR) - 5 A, alimentación 24 V DC.

4	1	.	8	1	.	7	.	0	2	4	.	9	0	2	4

Serie

Tipo
8 = Relé de estado sólido (SSR)

Salida
1 = 1 NA

Circuito de entrada
Ver características de la bobina

Circuito de salida
9024 = 5 A - 24 V DC
8240 = 3 A - 240 V AC

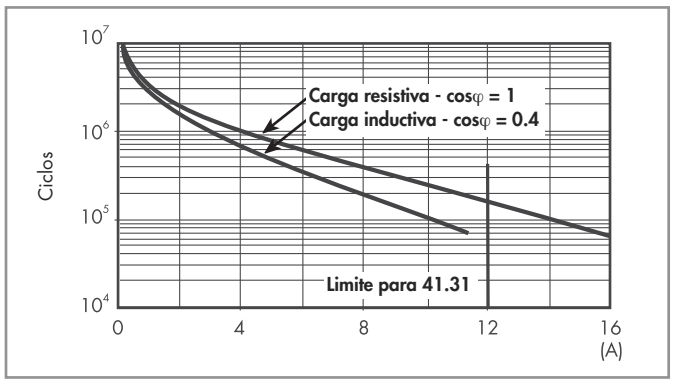
Relé electromecánico

Características generales

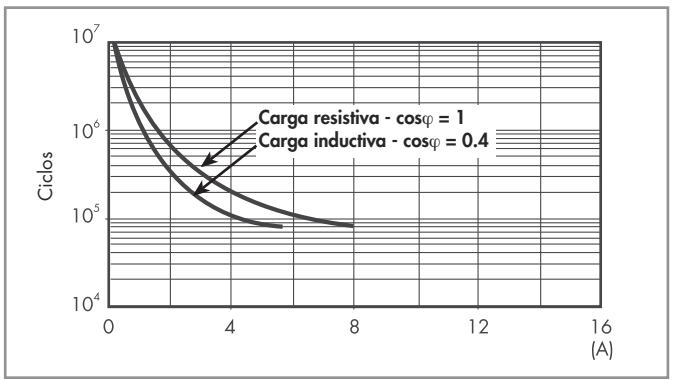
Aislamiento según EN 61810-1						
			1 contacto		**2 contactos**	
Tensión nominal de alimentación		V AC	230/400	230/400		
Tensión nominal de aislamiento		V AC	250	400	250	400
Grado de contaminacion			3	2	3	2
Aislamiento entre bobina y contactos						
Tipo de aislamiento			Reforzado (8 mm)		Reforzado (8 mm)	
Categoria de sobretensión			III		III	
Tensión soportada a los impulsos		kV (1.2/50 µs)	6		6	
Rigidez dieléctrica		V AC	4000		4000	
Aislamiento entre contactos adyacentes						
Tipo de aislamiento			—		Principal	
Categoria de sobretensión			—		III	
Tensión soportada a impulsos		kV (1.2/50 µs)	—		4	
Rigidez dieléctrica		V AC	—		2000	
Aislamiento entre contactos abiertos						
Tipo de desconexión			Microconexión		Microconexión	
Rigidez dieléctrica		V AC/kV (1.2/50 µs)	1000/1.5		1000/1.5	
Inmunidad a las perturbaciones conducidas						
Burst (5...50)ns, 5 kHz, en A1 - A2			EN 61000-4-4		nivel 4 (4 kV)	
Surge (1.2/50 µs) en A1 - A2 (modo diferencial)			EN 61000-4-5		nivel 3 (2 kV)	
Otros datos						
Tiempo de rebotes: NA/NC		ms	2/5			
Resistencia a la vibración (5...55)Hz: NA/NC		g	15/2			
Resistencia al choque		g	16			
Potencia disipada al ambiente	en vacío	W	0.4			
	con carga nominal	W	1.7 (41.31)	1.2 (41.52)	1.8 (41.61)	
Distancia de montaje entre relés en un circuito impreso		mm	≥ 5			

Características de los contactos

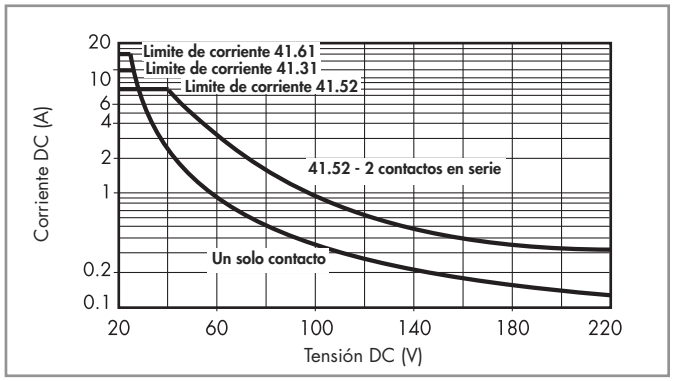
F 41 - Vida útil eléctrica (AC) en función de la carga
Tipos 41.31/61



F 41 - Vida útil eléctrica (AC) en función de la carga
Tipo 41.52



H 41- Máximo poder de corte con cargas en DC1



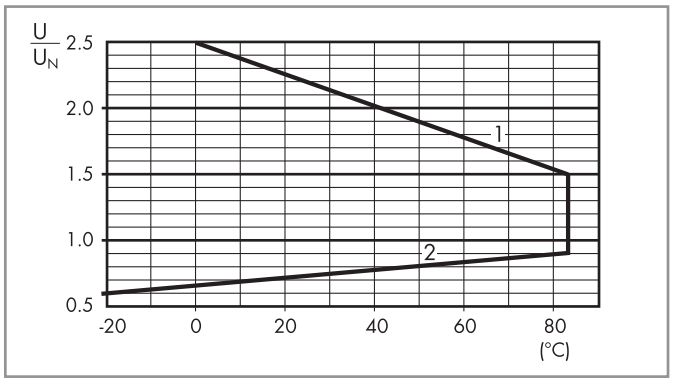
- La vida eléctrica para cargas resistivas en DC1 que tengan valores de tensión y corriente bajo la curva es de ≥ 100 ·10³ ciclos.
- Para las cargas DC13, la colocación de un diodo con polaridad invertida en paralelo con la carga permite obtener una vida eléctrica idéntica a la que se consigue con una carga en DC1. Nota: aumentará el tiempo de desconexión.

Características de la bobina

Valores de la versión DC

Tensión nominal U_N	Código bobina	Campo de funcionamiento U_{min}	Campo de funcionamiento U_{max}	Resistencia R	I Nominal absorbida I con U_N
V		V	V	Ω	mA
12	**9**.012	8.4	18	360	33.3
24	**9**.024	16.8	36	1440	16.7
48	**9**.048	33.6	72	5760	8.3
60	**9**.060	42	90	9000	6.6
110	**9**.110	77	165	24200	4.5

R 41 - Campo de funcionamiento de la bobina DC en función de la temperatura ambiente



1 - Tensión máx. admisible en la bobina.
2 - Tensión de conexión mínima con la bobina a temperatura ambiente.

Relé de estado sólido

Características generales

Otros datos			41.81 - 9024	41.81 - 8240
Potencia disipada al ambiente	en vacío	W	0.25	0.25
	con carga nominal	W	1.75	3.5

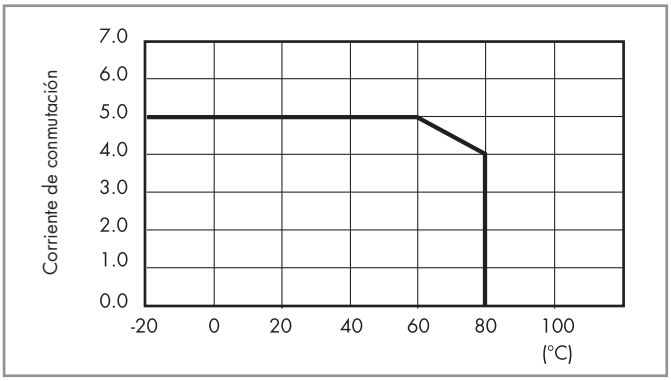
Características del circuito de entrada

Datos circuito de entrada

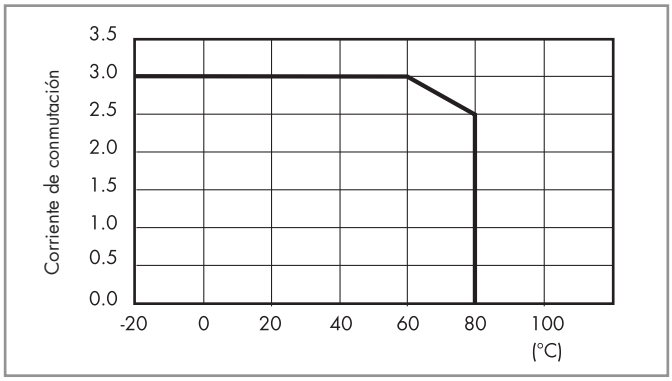
Tensión nominal U_N	Código circuito de entrada	Campo de funcionamiento U_{min}	Campo de funcionamiento U_{max}	Tensión de desconexión	Impedancia	Nominal absorbida I con U_N
V		V	V	V	Ω	mA
12	**7**.012	8	17	4	1550	5.5
24	**7**.024	14	32	9	2600	9

Características del circuito de salida

L 41 - Corriente de conmutación en función de la temperatura ambiente
Salida 5 A DC



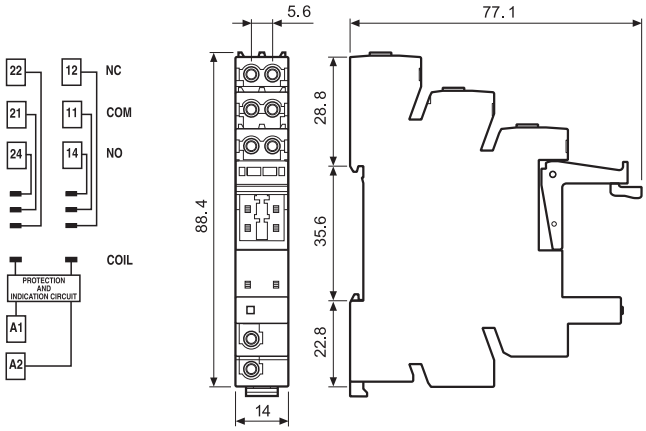
L 41 - Corriente de conmutación en función de la temperatura ambiente
Salida 3 A AC



93.02

Homologaciones (según los tipos):

Zócalo con bornes de jaula montaje en panel o carril 35 mm (EN 60715)			
Tensión nominal		**Tipo de relé**	**Tipo de zócalo**
6 V AC/DC		41.52.9.005.0010	93.02.0.024
12 V AC/DC		41.52.9.012.0010	93.02.0.024
24 V AC/DC		41.52.9.024.0010 o 41.81.7.024.xxxx	93.02.0.024
60 V AC/DC		41.52.9.060.0010	93.02.0.060
(110...125)V AC/DC		41.52.9.110.0010	93.02.0.125
(220...240)V AC/DC		41.52.9.110.0010	93.02.0.240
(230...240)V AC		41.52.9.110.0010	93.02.8.230
6 V DC		41.52.9.005.0010	93.02.7.024
12 V DC		41.52.9.012.0010 o 41.81.7.012.xxxx	93.02.7.024
24 V DC		41.52.9.024.0010 o 41.81.7.024.xxxx	93.02.7.024
48 V DC		41.52.9.048.0010	93.02.7.060
60 V DC		41.52.9.060.0010	93.02.7.060
Accesorios			
Puente de 8 terminales		093.08 (ver página al lado)	
Separador de plástico		093.01 (ver página al lado)	
Juego de etiquetas, 72 unidades		090.72 (ver página al lado)	
Características generales			
Valor nominal		10 A - 250 V	
Rigidez dieléctrica		6 kV (1.2/50 µs) entre bobina y contactos	
Grado de protección		IP 20	
Temperatura ambiente	°C	(–40...+70)°C - ($U_N \leq$ 60 V DC), (–40...+55)°C - ($U_N >$ 60 V DC)	
Par de apriete	Nm	0.5	
Longitud de pelado del cable	mm	8	
Capacidad de conexión de los bornes para zócalo 93.02		hilo rígido	hilo flexible
	mm^2	1x6 / 2x2.5	1x4 / 2x2.5
	AWG	1x10 / 2x14	1x12 / 2x14

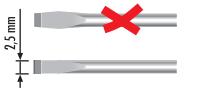


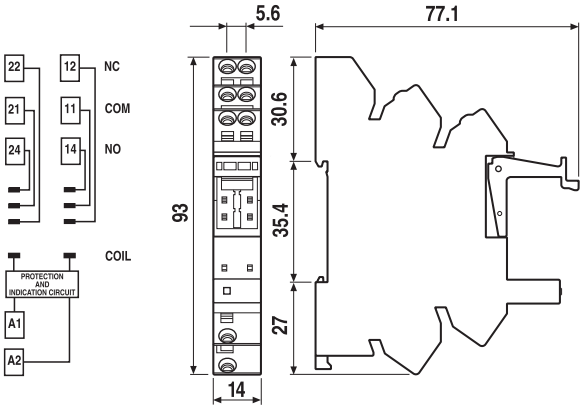
Serie 93 - Zócalos y accesorios para relés serie 41

93.52

Homologaciones (según los tipos):

Zócalo con bornes de conexión rápida montaje en carril de 35 mm (EN 60715)			
Tensión nominal		**Tipo de relé**	**Tipo de zócalo**
6 V AC/DC		41.52.9.005.0010	93.52.0.024
12 V AC/DC		41.52.9.012.0010	93.52.0.024
24 V AC/DC		41.52.9.024.0010 o 41.81.7.024.xxxx	93.52.0.024
60 V AC/DC		41.52.9.060.0010	93.52.0.060
(110...125)V AC/DC		41.52.9.110.0010	93.52.0.125
(220...240)V AC/DC		41.52.9.110.0010	93.52.0.240
(230...240)V AC		41.52.9.110.0010	93.52.8.230
6 V DC		41.52.9.005.0010	93.52.7.024
12 V DC		41.52.9.012.0010 o 41.81.7.012.xxxx	93.52.7.024
24 V DC		41.52.9.024.0010 o 41.81.7.024.xxxx	93.52.7.024
48 V DC		41.52.9.048.0010	93.52.7.060
60 V DC		41.52.9.060.0010	93.52.7.060
Accesorios			
Puente de 8 terminales		093.08 (ver tabla abajo)	
Separador de plástico		093.01 (ver tabla abajo)	
Juego de etiquetas, 72 unidades		090.72 (ver tabla abajo)	
Características generales			
Valor nominal		10 A - 250 V	
Rigidez dieléctrica		6 kV (1.2/50 µs) entre bobina y contactos	
Grado de protección		IP 20	
Temperatura ambiente	°C	(–40...+70)°C - ($U_N \leq$ 60 V DC), (–40...+55)°C - ($U_N >$ 60 V DC)	
Longitud de pelado del cable	mm	8	
Capacidad de conexión de los bornes para zócalo 93.52		hilo rígido	hilo flexible
	mm^2	1x2.5	1x2.5
	AWG	1x14	1x14



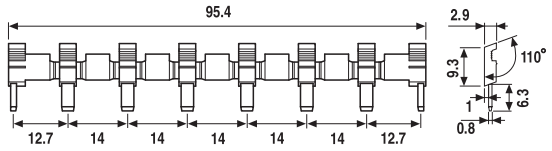


Accesorios

093.08

Homologaciones (según los tipos):

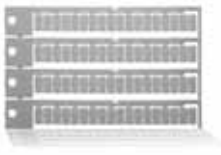
Puente de 8 terminales para zócalos 93.02 y 93.52	093.08 (azul)	093.08.0 (negro)
Valor nominal	10 A - 250 V	



093.01

Separador de plástico para zócalos 93.02 y 93.52	093.01

2 mm de espesor, se utilizal al inicio y al final de un grupo de interface.
Se puede utilizar como separación óptica, pero se tiene que útilizar para:
- separar grupos de interface PLC con diferentes tensiones de alimentación según VDE 0106-101
- puentes recortados con un número inferior a 20 polos.



060.72

Juego de etiquetas de identificación, plástica, para 38.x2 72 unidades, 6x12 mm	060.72

95.13.2

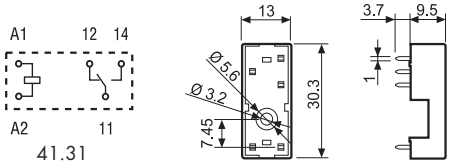
95.15.2

Homologaciones (según los tipos):

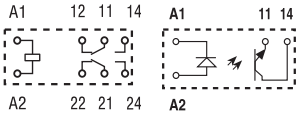
Zócalo para circuito impreso	95.13.2 Azul	95.13.20 Negro	95.15.2 Azul	95.15.20 Negro
Tipo de relé	41.31		41.52, 41.61, 41.81[1]	
Accesorios				
Brida de retención de plástico	095.42			
Características generales				
Valor nominal	10 A - 250 V *			
Rigidez dieléctrica	6 kV (1.2/50 µs) entre bobina y contactos			
Grado de protección	IP 20			
Temperatura ambiente °C	–40...+70			

* Con corrientes >10 A, los terminales de los contactos deben conectarse en paralelo (21 con 11, 24 con 14, 22 con 12).

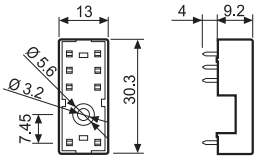
[1] Con relé 41.81 los terminales de contacto NA son los numeros 11 y 14.

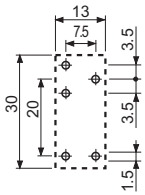


41.31

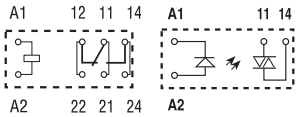


41.52 41.81 - 9024

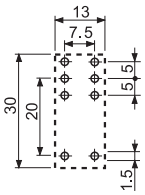




95.13.2
Vista parte inferior



41.61 41.81 - 8240



95.15.2
Vista parte inferior

Código de embalaje

Identificación de la elaboración y de las bridas a través de las últimas tres letras.

Ejemplo:

9	5	.	1	3	.	2	S	L	A

A Embalaje estándar

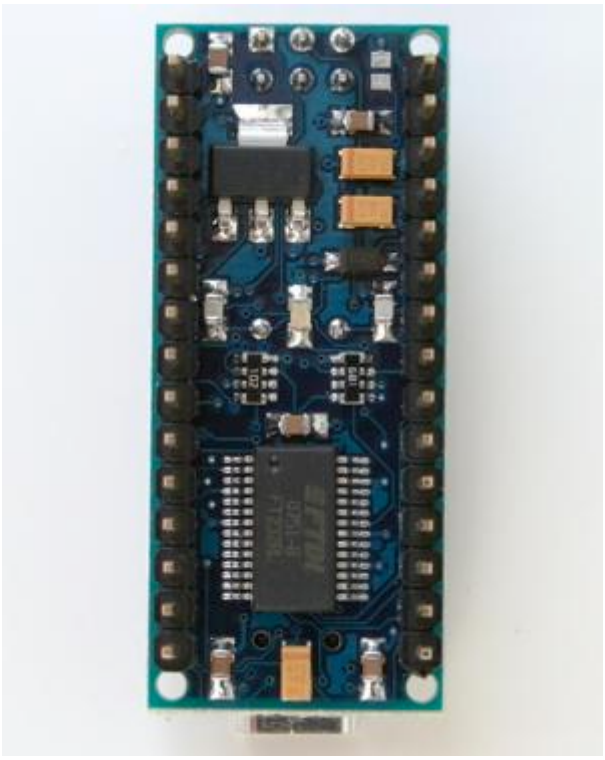
SL Brida de plástico

9	5	.	1	3	.	2			

Sin brida

Arduino Nano

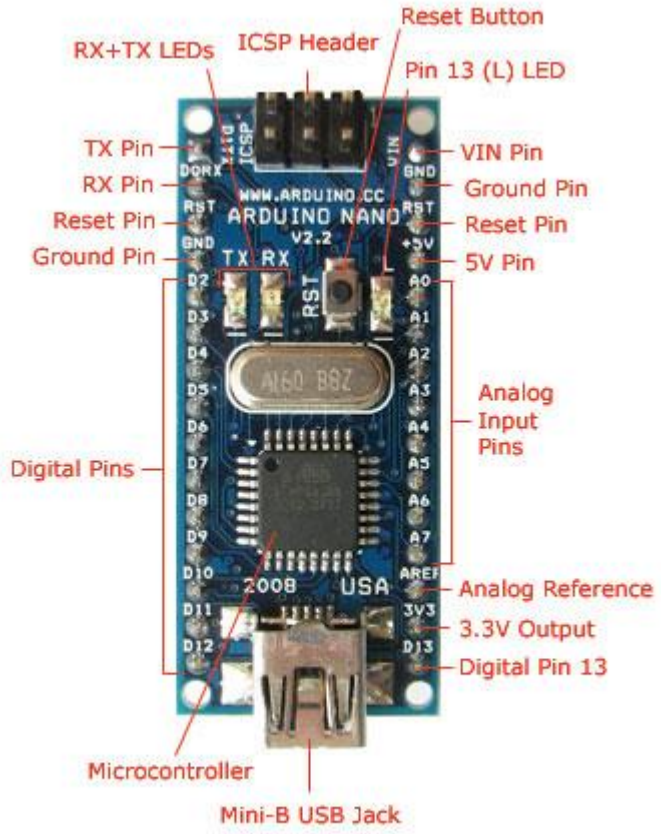
Arduino Nano Front

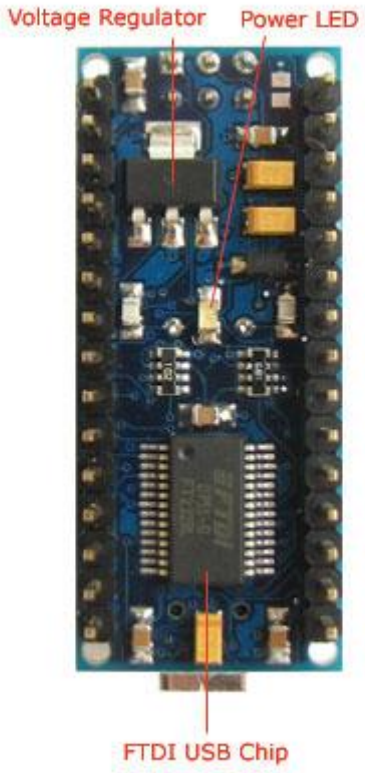


Arduino Nano Rear

Overview

The Arduino Nano is a small, complete, and breadboard-friendly board based on the ATmega328 (Arduino Nano 3.0) or ATmega168 (Arduino Nano 2.x). It has more or less the same functionality of the Arduino Duemilanove, but in a different package. It lacks only a DC power jack, and works with a Mini-B USB cable instead of a standard one. The Nano was designed and is being produced by Gravitech.





Schematic and Design

Arduino Nano 3.0 (ATmega328): schematic, Eagle files.
Arduino Nano 2.3 (ATmega168): manual (pdf), Eagle files. *Note:* since the free version of Eagle does not handle more than 2 layers, and this version of the Nano is 4 layers, it is published here unrouted, so users can open and use it in the free version of Eagle.

Specifications:

Microcontroller	Atmel ATmega168 or ATmega328
Operating Voltage (logic level)	5 V
Input Voltage (recommended)	7-12 V
Input Voltage (limits)	6-20 V
Digital I/O Pins	14 (of which 6 provide PWM output)
Analog Input Pins	8
DC Current per I/O Pin	40 mA
Flash Memory	16 KB (ATmega168) or 32 KB (ATmega328) of which 2 KB used by bootloader
SRAM	1 KB (ATmega168) or 2 KB (ATmega328)
EEPROM	512 bytes (ATmega168) or 1 KB (ATmega328)
Clock Speed	16 MHz
Dimensions	0.73" x 1.70"

Power:

The Arduino Nano can be powered via the Mini-B USB connection, 6-20V unregulated external power supply (pin 30), or 5V regulated external power supply (pin 27). The power source is automatically selected to the highest voltage source.

The FTDI FT232RL chip on the Nano is only powered if the board is being powered over USB. As a result, when running on external (non-USB) power, the 3.3V output (which is supplied by the FTDI chip) is not available and the RX and TX LEDs will flicker if digital pins 0 or 1 are high.

Memory

The ATmega168 has 16 KB of flash memory for storing code (of which 2 KB is used for the bootloader); the ATmega328 has 32 KB, (also with 2 KB used for the bootloader). The ATmega168 has 1 KB of SRAM and 512 bytes of EEPROM (which can be read and written with the EEPROM library); the ATmega328 has 2 KB of SRAM and 1 KB of EEPROM.

Input and Output

Each of the 14 digital pins on the Nano can be used as an input or output, using pinMode(), digitalWrite(), and digitalRead() functions. They operate at 5 volts. Each pin can provide or receive a maximum of 40 mA and has an internal pull-up resistor (disconnected by default) of 20-50 kOhms. In addition, some pins have specialized functions:

- **Serial: 0 (RX) and 1 (TX).** Used to receive (RX) and transmit (TX) TTL serial data. These pins are connected to the corresponding pins of the FTDI USB-to-TTL Serial chip.
- **External Interrupts: 2 and 3.** These pins can be configured to trigger an interrupt on a low value, a rising or falling edge, or a change in value. See the attachInterrupt() function for details.
- **PWM: 3, 5, 6, 9, 10, and 11.** Provide 8-bit PWM output with the analogWrite() function.
- **SPI: 10 (SS), 11 (MOSI), 12 (MISO), 13 (SCK).** These pins support SPI communication, which, although provided by the underlying hardware, is not currently included in the Arduino language.
- **LED: 13.** There is a built-in LED connected to digital pin 13. When the pin is HIGH value, the LED is on, when the pin is LOW, it's off.

The Nano has 8 analog inputs, each of which provide 10 bits of resolution (i.e. 1024 different values). By default they measure from ground to 5 volts, though is it possible to change the upper end of their range using the analogReference() function. Additionally, some pins have specialized functionality:

I²C: 4 (SDA) and 5 (SCL). Support I²C (TWI) communication using the Wire library (documentation on the Wiring website).

There are a couple of other pins on the board:

AREF. Reference voltage for the analog inputs. Used with analogReference().
Reset. Bring this line LOW to reset the microcontroller. Typically used to add a reset button to shields which block the one on the board.

See also the mapping between Arduino pins and ATmega168 ports.

Communication

The Arduino Nano has a number of facilities for communicating with a computer, another Arduino, or other microcontrollers. The ATmega168 and ATmega328 provide UART TTL (5V) serial communication, which is available on digital pins 0 (RX) and 1 (TX). An FTDI FT232RL on the board channels this serial communication over USB and the FTDI drivers (included with the Arduino software) provide a virtual com port to software on the computer. The Arduino software includes a serial monitor which allows simple textual data to be sent to and from the Arduino board. The RX and TX LEDs on the board will flash when data is being transmitted via the FTDI chip and USB connection to the computer (but not for serial communication on pins 0 and 1).
A SoftwareSerial library allows for serial communication on any of the Nano's digital pins.
The ATmega168 and ATmega328 also support I2C (TWI) and SPI communication. The Arduino software includes a Wire library to simplify use of the I2C bus; see the documentation for details. To use the SPI communication, please see the ATmega168 or ATmega328 datasheet.

Programming

The Arduino Nano can be programmed with the Arduino software (download). Select "Arduino Diecimila, Duemilanove, or Nano w/ ATmega168" or "Arduino Duemilanove or Nano w/ ATmega328" from the **Tools**

> **Board** menu (according to the microcontroller on your board). For details, see the reference and tutorials.
The ATmega168 or ATmega328 on the Arduino Nano comes preburned with a bootloader that allows you to upload new code to it without the use of an external hardware programmer. It communicates using the original STK500 protocol (reference, C header files).
You can also bypass the bootloader and program the microcontroller through the ICSP (In-Circuit Serial Programming) header; see these instructions for details.

Automatic (Software) Reset

Rather then requiring a physical press of the reset button before an upload, the Arduino Nano is designed in a way that allows it to be reset by software running on a connected computer. One of the hardware flow control lines (DTR) of the FT232RL is connected to the reset line of the ATmega168 or ATmega328 via a 100 nanofarad capacitor. When this line is asserted (taken low), the reset line drops long enough to reset the chip. The Arduino software uses this capability to allow you to upload code by simply pressing the upload button in the Arduino environment. This means that the bootloader can have a shorter timeout, as the lowering of DTR can be well-coordinated with the start of the upload.
This setup has other implications. When the Nano is connected to either a computer running Mac OS X or Linux, it resets each time a connection is made to it from software (via USB). For the following half-second or so, the bootloader is running on the Nano. While it is programmed to ignore malformed data (i.e. anything besides an upload of new code), it will intercept the first few bytes of data sent to the board after a connection is opened. If a sketch running on the board receives one-time configuration or other data when it first starts, make sure that the software with which it communicates waits a second after opening the connection and before sending this data.