MOSFET degradation dependence on input signal power in a RF power amplifier

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Abstract

Aging produced by both DC and RF stress is experimentally analyzed on a RF CMOS power amplifier. The selected circuit topology allows observing individual NMOS and PMOS transistors degradations, as well as the aging effect on the circuit functionality. A direct relation between DC and RF (gain) parameters has been observed. NMOS degradation (both in mobility and V_{th}) is stronger than that of the PMOS, which identifies the NMOS as the main cause of the RF degradation in this circuit.

Keywords: CMOS, MOSFET degradation, RF power amplifier, RF stress

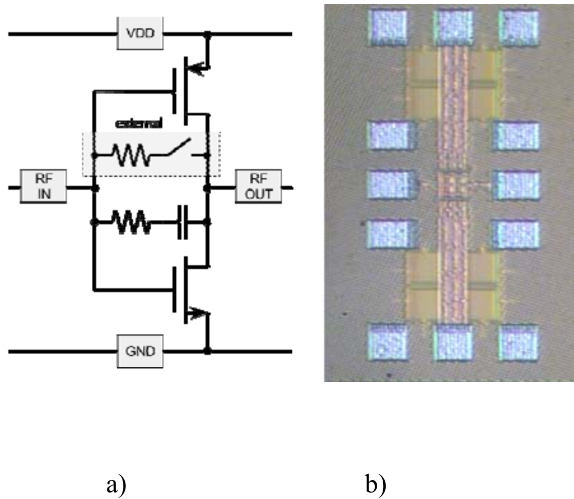
1. Introduction

Aggressive device scaling has increased the relevance of stress-induced MOSFET degradation (due to dielectric aging mechanisms as Hot Carrier Injection, HCI, and Bias Temperature Instability, BTI) on circuit performance [1]. However, experimental observations of the device degradation under circuit operation conditions together with its impact on the circuit performance are not easy to obtain, because of the difficulty to access the transistor terminals once they are embedded in a more complex circuit. This problem is aggravated in radiofrequency (RF) circuits because of the practical impossibility to access internal nodes and the general complexity associated to high-frequency measurements. Thus, most experimental works about aging on RF amplifiers choose one-transistor based-circuits where the access terminals for transistor and circuit are coincident [2, 3, 4]. In other works, the performance degradation of RF circuits containing multiple transistors is simply predicted by means of simulation, based on models of aged transistors that were first experimentally stressed and characterized [5, 6, 7]. The use of transistor models characterized after DC stress alone ignores the contribution of the RF signal component on the circuit degradation, which is particularly relevant in power amplifiers that usually suffer high input powers. In this paper, aging produced by RF stress is experimentally analyzed on a RF power amplifier (PA) nominally operated as class-A, implemented in a CMOS 65 nm technology. The degradation of the circuit transistors and its impact on circuit performance have been evaluated.

2. Samples and experimental setup

A schematic and a picture of the purposely designed and fabricated PA (DUT) in this work are shown in Fig. 1. The topology chosen for the PA is a self-biased complementary current-reuse amplifier. This topology allows observing the individual degradations of the NMOS and PMOS transistors, as well as the aging effect on the circuit functionality, allowing obtaining a realistic reliability relationship between the devices

and circuit. Both NMOS and PMOS W/L are 180µm/60nm, split in 45 fingers. The circuit contains two feedback nets. An external resistive feedback provides self-biasing and sets the PA operating point in the gain region. Therefore this configuration is used for RF characterization and the stress process. This resistive feedback is external so it can be disabled for the individual transistor characterization. A second internal RC feedback provides AC impedance matching. With a nominal supply voltage of V_{DD} = 1.2V, the operating point is set to $V_{IN} = V_{OUT}$ = 520 mV, I_{DC} = 7.3 mA. The non-resonant topology allows a wideband response and power amplification in the range 300 MHz–8 GHz. At 2.45 GHz, the measured gain is S_{21} = 10.3 dB, S_{11}= –13dB, S_{22}=8dB, and the 1dB compression point P_{1dB} is 5dBm.



a) b)

Fig. 1: Topology (a) and picture (b) of the designed and fabricated Power Amplifier (DUT).

A stress-measurement procedure was used to analyze PA aging (setup shown in Fig. 2). The RF stress consists in applying to the DUT an input power (P_{IN}), ranged between -20dBm and 10dBm, at 2.45GHz, with V_{DD}=2.8V. In all cases, the stress duration was 30 minutes. Stress values and duration were chosen to provoke an appreciable damage to the circuit in a reasonable time. Each RF stress was applied to a different circuit, which was characterized at nominal operation conditions before (fresh) and after the accelerated aging. The DC characterization consisted in the measurement of the electrical characteristics of the PMOS and NMOS transistors, as well as the DC transfer curves of the PA circuit (external R disabled), while RF characterization was only done at PA level. A Vector Network Analyzer (VNA) and a Semiconductor Parameter Analyzer (SPA) were used to perform the different measurements, as Fig. 2 indicates.

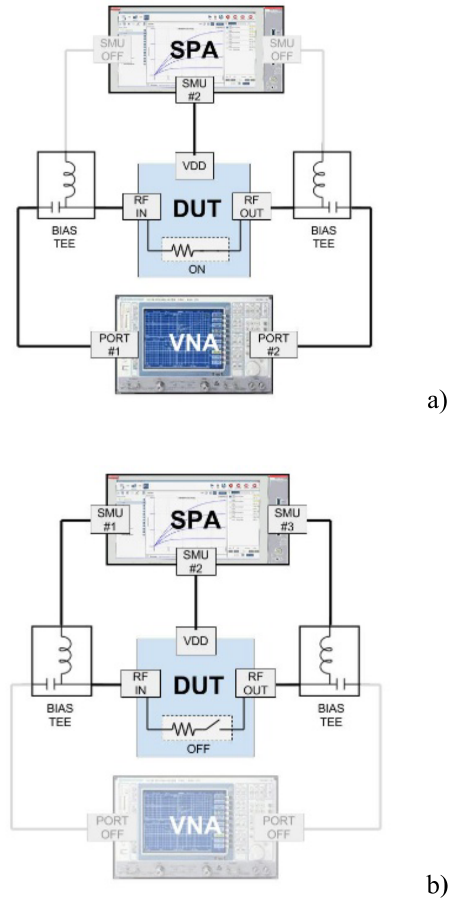


Fig. 2: Set-up used for the stress process and for the RF characterization (a) and for DC characterization (b).

3. Results

For all the stress cases, a decrease of I_{DC} and a shift of the transfer curve to the right are produced (Fig. 3a). Fig. 3b plots the inversion voltage increase, ΔV_{INV}, produced as a consequence of each stress (where the inversion voltage V_{INV} is such that $V_{IN} = V_{OUT} = V_{INV}$, which is the DC self-bias voltage), as well as the decrease in the DC current consumption, ΔI_{DC}, as a function of P_{IN}. The changes in both magnitudes are clearly correlated.

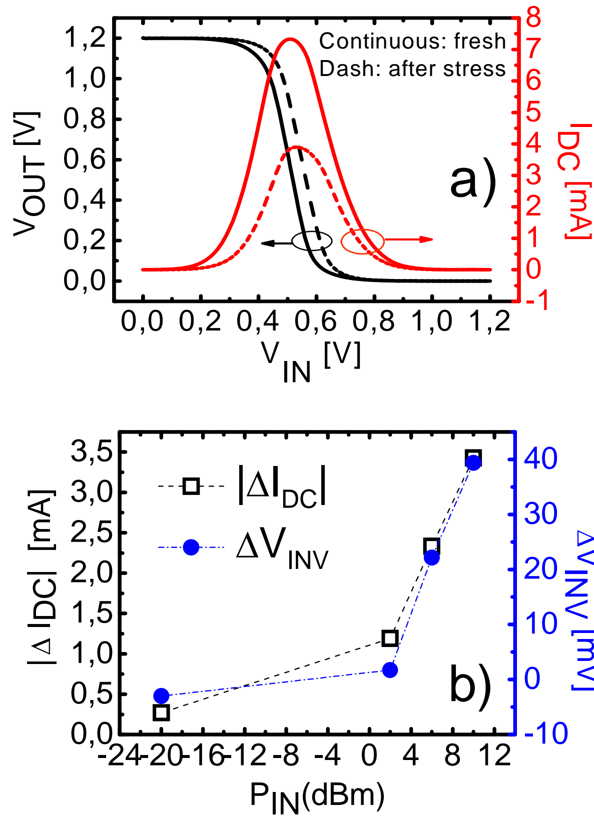


Fig. 3: a) Example of the variation of the inverter transfer curve and I_{DC} before and after a stress of V_{DD}=2.8V and P_{IN}=10dBm at 2.45GHz during 30 minutes. b) $|\Delta I_{DC}|$ and ΔV_{INV} as a function of P_{IN}.

Fig. 4a shows the ΔV_{th} (difference between stressed and fresh V_{th}) for the NMOS and the PMOS, as a function of P_{IN}, where V_{th} has been obtained by using the constant current method. Clearly, the ΔV_{th} increase in the NMOS is larger than in the PMOS and the difference increases with P_{IN}. Fig. 4b shows the relative mobility reduction, $\Delta\mu$, as a function of P_{IN}, which is also larger for the NMOS transistor. The mobility parameter has been obtained by fitting the obtained DC measurements in deep ohmic region to a first order model. This degradation of the transistor parameters produces the observed change in the DC operating point of the PA, which will in consequence result in a degradation of its RF performance. An example of the gain parameter S_{21} measured before and after the stress is shown in Fig. 5a around the 2.45 GHz frequency of interest. A clear difference between the fresh and the stressed PA performance is observed. For this stress, a small degradation of 0.5 dB in the S_{11} parameter was observed (both input (S_{11}) and output (S_{22}) matching parameters have been always below reasonable levels). The impact of PA aging on the circuit gain is quantified in Fig. 5b, where the degradation observed in the S_{21} parameter after the stress application is represented as a function of P_{IN}. The PA gain degradation fits well the degradation in its operating point (I_{DC}) and transistor parameters (V_{th}, μ) observed in Figs. 3 and 4 respectively, and correlates perfectly to an exponential law.

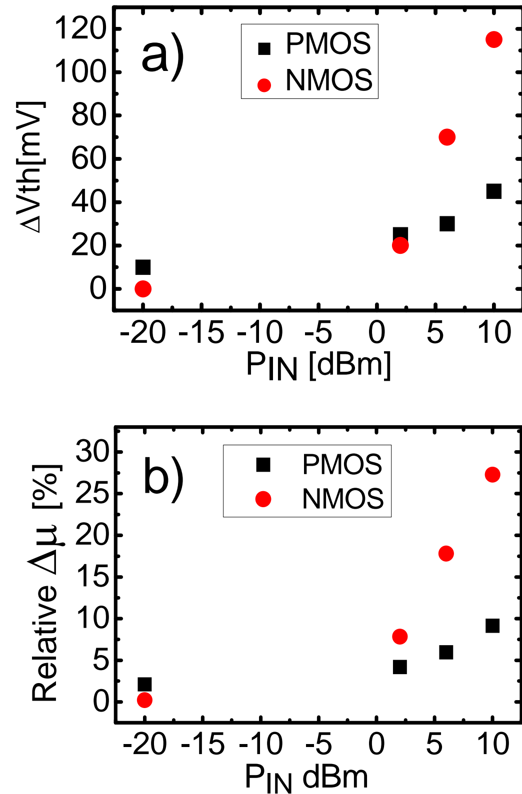


Fig. 4: a) ΔVth of the NMOS and PMOS and b) relative mobility variation, as a function of PIN. Larger ΔVth and relative Δμ for the NMOS transistor indicate that this transistor is more damaged than the PMOS.

Fig. 6 shows the I_{DC} variation as a function of the amplifier gain shift for the different P_{IN}. A linear relationship between the I_{DC} and gain degradation as a consequence of the stress is observed, which confirms experimentally that RF parameters degradation is a direct consequence of the DC degradation. Finally, the relationship between RF performance degradation (gain) and degradation of the transistor parameters (V_{th} and mobility) is shown in Fig. 7. NMOS degradation (both in mobility and V_{th}) is stronger than that of the PMOS, which identifies the NMOS wear out as the main cause of the RF degradation in this circuit.

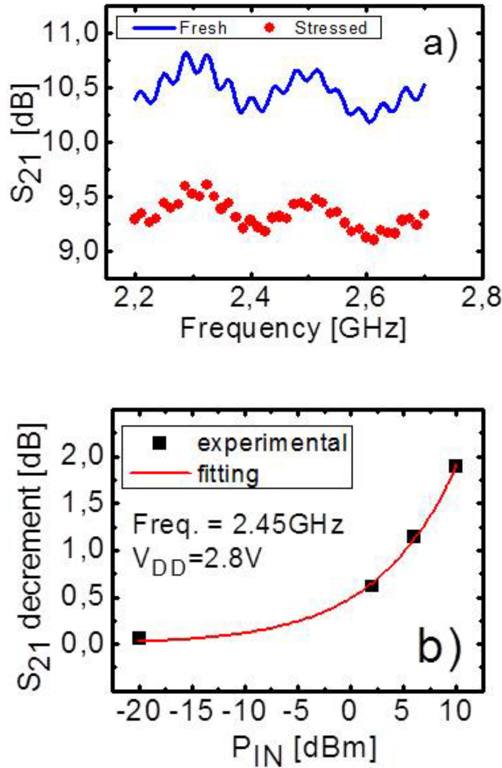


Fig. 5: (a) S_{21} parameter obtained during the RF charact. for a fresh (line) and after a 30min stress of V_{DD}=2.8V and P_{IN}=6dBm (circles), as a function of the freq. around the 2.45GHz range of interest. (b) PA gain variation as a function of P_{IN}.

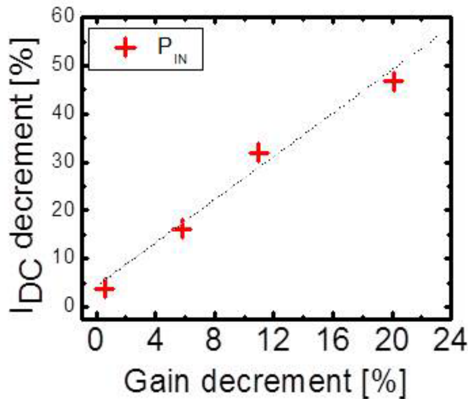


Fig. 6: Relative I_{DC} decrement as a function of relative gain decrease. A linear relation between the I_{DC} and gain decreases is observed.

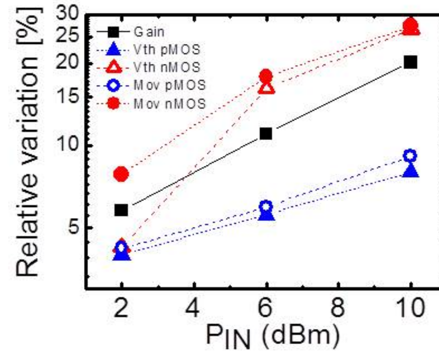


Fig. 7: Relative variation of DC parameters (NMOS and PMOS Vth and mobility) and a RF parameter (gain) as a function of P_{IN}. Larger relative variations are observed for the NMOS transistor, which indicates its relevant role on the circuit aging.

4. Conclusions

MOSFET aging produced by RF stress has been experimentally analyzed on a purposely designed RF power amplifier, whose topology allows observing the individual degradations of the NMOS and PMOS circuit transistors and their impact on the circuit functionality. Transistor aging increases with the RF input signal power, being larger for the NMOS (both in mobility and V_{th}). A direct relation of DC and RF parameters (gain) degradation has been observed, being the NMOS aging the dominant cause of the RF circuit damage.

Acknowledgements

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