A Modulation Strategy to Operate Multilevel Multiphase Diode-Clamped and Active-Clamped DC-AC Converters at Low Frequency Modulation Indices with DC-Link Capacitor Voltage Balance

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***Abstract*—This paper proposes a modulation strategy for multilevel multiphase diode-clamped dc-ac converters (also applicable to other functionally-equivalent topologies) able to keep the dc-link capacitor voltages balanced under passive front ends, low frequency modulation indices (i.e., low number of switching transitions per fundamental cycle), any value of the amplitude modulation index, and any ac-side displacement power factor. A suitable phase voltage pattern with minimum number of switching transitions is presented for the *n*-level three-phase case. Subsequently, it is extended to higher number of switching transitions per fundamental cycle and to higher number of phases. Simulation results with three-, four-, and five- levels, three- and five- phases, and several frequency-modulation-index values are presented to validate the proposed modulation strategy. Experimental results obtained with a four-level three-phase dc-ac converter prototype are also provided. The proposed modulation strategy enables the use of this type of converters in applications where the ac fundamental frequency may be close to the switching frequency, such as in high power systems and variable-speed motor drives.**

***Index Terms*—Active-clamped, capacitor voltage balance, dc-ac conversion, diode-clamped, multilevel, pulsewidth modulation, virtual vector.**

I. Introduction

MULTILEVEL technology is still an attractive research topic in the electrical energy conversion arena due to the inherent system complexity, with increased degrees of freedom, and the opportunities for improvements that this technology offers in terms of converter power rating, efficiency, harmonic distortion, and electromagnetic noise [1], [2].

This paper focuses on multilevel multiphase dc-ac converters with a topology consisting of a set of semiconductor power devices and a single dc link, formed by a series connection of $n-1$ capacitors, giving rise to n accessible dc-link points, as shown in Fig. 1. The popular diode-clamped topology belongs to this category. Other arrangements of semiconductor devices to build the converter legs are also possible, such as in the active-clamped configuration [3]. For all these functionally equivalent topologies, each converter leg can be modelled as a single-pole n-throw switch, as shown in Fig. 1. At every point in time, the ac terminal of each leg is connected to one and only one dc-link terminal, indicated by a solid circle. The operation of such multilevel multiphase dc-ac converters is challenging due to the widely studied dc-link capacitor voltage balancing problem [4]-[29], which is still an active research topic in the recent literature [5]-[8], [10], [11], [13], [15]-[17], [21]-[26].

This problem arises from the occurrence of non-zero inner dc-link currents ($i_{\mathrm{dc}y}$, $y \in \{2, 3, \ldots, n-1\}$, with reference to Fig. 1). The current $i_{\mathrm{dc}y}$ flowing through the inner dc-link point dc_y is typically split into a current flowing through the capacitors below dc_y ($\mathrm{C}_1, \ldots, \mathrm{C}_{y-1}$) and a current flowing through the capacitors above dc_y ($\mathrm{C}_y, \ldots, \mathrm{C}_{n-1}$). A positive (negative) $i_{\mathrm{dc}y}$ will discharge (charge) the capacitors below dc_y and charge (discharge) the capacitors above dc_y. Therefore, an initial capacitor voltage balanced condition will be lost if non-zero

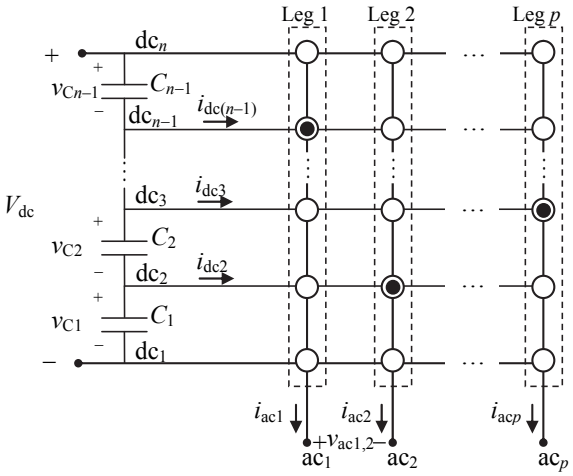

Fig. 1. Functional schematic of an n-level p-leg dc-ac converter.

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i_{dcy} occur. On the other hand, non-zero i_{dcy} are unavoidable if connections of the leg ac terminal to the inner dc-link points are allowed.

Different solutions have been proposed to solve this problem that can be broadly categorized as hardware and software solutions. Hardware solutions introduce additional circuitry to inject/draw additional current into/from the inner dc-link points to compensate the inherent converter i_{dcy} current [4]-[12]. A first approach is to use auxiliary balancing circuits including transistors, diodes, together with inductors [4]-[8] or capacitors [9] or both inductors and capacitors [5]. This typically solves the balancing problem in the full operating range. A second approach consists on relying on an active front-end converter in a back-to-back configuration to aid in the capacitor voltage balancing task [10]-[12]. However, this solution still typically presents a limited balancing capability in some operating regions, especially for more than three-levels.

On the other hand, software solutions do not use additional components to accomplish the balancing task. A first approach is to define a suitable pulsewidth modulation (PWM) strategy, typically modified according to the control action determined by a closed-loop control of the dc-link capacitor voltages [14]-[24], [26]-[29]. A second approach consists in applying predictive control [13], [25]. In all cases, the goal is to maintain an average i_{dcy} equal to zero over a specific period of time. This will ensure that the capacitor voltages are balanced at the beginning and at the end of this period.

Most modulation strategies and predictive controls have been designed to operate with a high number of switching transitions per fundamental cycle. Software solutions based on predictive control are able to keep capacitor voltage balance over the full operating range [13], but they lack full control of the switching frequency and harmonic spectrum, besides being computationally intensive. The modulation strategies can be space-vector-diagram-based [14], [16], [23], [24] or carrier-based [15], [17]-[20] implemented. From a space vector diagram perspective, references [14]-[17] propose traditional modulation strategies based on the nearest-three vectors and rely on a proper selection of the available redundant switching states to accomplish the capacitor voltage balancing task. But this approach has limitations over a wide operating range for more than three levels. To overcome these limitations, modulation strategies employing other arrangements of vectors have been conceived [18]-[20], [23], [24]. This is the case of the modulation proposed in [18] for n-level three-phase converters and extended to any number of phases in [19]. It has been demonstrated that this modulation strategy, under high number of switching transitions per fundamental cycle (i.e., approximately constant phase currents over the switching cycle), achieves capacitor voltage balancing under all operating conditions (all modulation index values and ac-side displacement power factors) in both the linear and overmodulation regions [18]-[20].

However, operating with a low number of switching transitions per fundamental cycle is important in several applications. For instance, it is often necessary in high-power systems, to reduce power semiconductor losses to a level where practical heat sink solutions can be adopted. It is also important in variable-speed motor drives, to be able to achieve the highest speeds for a given maximum switching frequency. Although the application of predictive control with a moderate switching frequency has been demonstrated [25], this technique does not currently allow a full control over the switching frequency and harmonic spectrum to make it suitable for very low switching transitions per fundamental cycle. On the other hand, most of the proposed modulation strategies for multilevel multiphase dc-ac converters with low number of switching transitions per fundamental cycle are implemented through a set of pre-calculated leg-output switching angles and primarily focus on eliminating, minimizing, or mitigating ac voltage low-order harmonic components [26]-[33]. Very few of these studies have analyzed the capacitor voltage balance problem [27]-[29], and almost all of this literature concentrates on the singular case of a three-level three-phase dc-ac converter. In [27], a typical leg output-voltage pattern from selective harmonic elimination (SHE) PWM is applied to a three-level three-phase dc-ac converter and it is modified according to the redundant switching state concept (i.e., modifying the converter ac-side common mode voltage) to regulate the two capacitor voltages. In [28], the regulation of the capacitor voltages is performed introducing small variations of the switching angles defined by the SHE PWM technique. It is important to note that the three-level case is a special case where the capacitor voltage balancing is easier to achieve than for higher levels due to the absence of inner capacitors. The direct extension of the modulation patterns presented for three-levels to converters with higher levels would lead to the collapse of some capacitor voltages, as will be explained in the following section. In [29] the same approach used in [27] based on SHE PWM and redundant switching states is applied to a five-level three-phase converter. However, the approach presents limitations in the maximum applicable modulation index and the regulation capability of the dc-link capacitor voltages. In [32] and [33], a SHE PWM is proposed for a five-level and six-level converter, respectively, which would lead to capacitor voltage unbalance under passive front-ends.

To contribute to fill this gap, the aim of this paper is to prove the feasibility of operating multilevel ($n \geq 3$) and multiphase ($p \geq 3$) dc-ac converters with capacitor voltage balance under passive front-ends, no additional auxiliary circuitry, and low number of switching transitions per fundamental cycle. A general modulation pattern, applicable to systems with $n \geq 3$ and $p \geq 3$ is presented to reach this goal. The modulation pattern is extended from the lowest possible number of switching transitions per fundamental cycle to higher number of transitions.

The paper is organized as follows. Section II presents the proposed modulation pattern with minimum number of switching transitions for multilevel three-phase dc-ac converters. In Section III, this modulation pattern is extended to higher number of switching transitions per fundamental cycle and higher number of phases. Section IV presents

simulation and experimental results to evaluate the performance of the proposed modulation pattern and associated closed-loop capacitor voltage control. Section V discusses the paper findings and the selection of the optimum modulation implementation in practice under different scenarios. Finally, Section V outlines the conclusions.

II. Modulation Pattern for Three-Phase Dc-Ac Converters with Minimum Number of Switching Transitions

This Section presents a novel modulation strategy for multilevel three-phase dc-ac converters capable of guaranteeing capacitor voltage balance with minimum number of switching transitions per fundamental cycle. The discussion starts with the three-level case (already treated in the literature [26]) and then the number of levels is increased until a general solution can be induced. Quarter wave symmetry is assumed in the converter phase voltages in order to avoid even order harmonics and for the sake of simplicity. In the analysis of phase voltage patterns, it will be further assumed that the potential effect of the phase-current fundamental component on capacitor voltage balance is much larger than the effect of the harmonics, since the fundamental component is the most significant phase-current component.

The detailed harmonic analysis of the voltage pattern generated by the proposed modulation strategy is considered to be beyond the scope of this paper due to space constraints. However, total harmonic distortion (THD) and weighted THD (WTHD) plots as a function of the amplitude modulation index are provided as a global measure of the harmonic distortion. In addition, in Section III, the harmonic spectrum of the ac-side voltages and phase currents is presented for a particular case.

A. Three Levels

Fig. 2(a) presents the three-level phase voltage pattern (v_{acx}, with $x \in \{1,2,3\}$, the phase voltage is with reference to point dc_1) with minimum number of switching transitions per fundamental cycle that can produce a phase voltage with adjustable fundamental-component amplitude. Angle α represents the unique degree of freedom that can be used to adjust the fundamental-component amplitude. Fig. 2(a) also depicts a generic (valid for any load displacement power factor) fundamental component of the phase current

$$i_{acx,1} = i^{p}_{acx,1} + i^{q}_{acx,1}, \tag{1}$$

which is decomposed into $i^{p}_{acx,1}$ and $i^{q}_{acx,1}$ components, in-phase and in-quadrature with the fundamental component of the phase voltage, respectively. The solid blue areas represent the charge drawn from (positive areas) or injected into (negative areas) the dc-link midpoint. As can be observed, due to v_{acx} symmetry and the symmetry of the sinus and cosinus functions, the areas cancel out in both $i^{p}_{acx,1}$ and $i^{q}_{acx,1}$. Thus, there is no net charge delivered to the dc-link mid-point, which is the condition to maintain any preexisting capacitor voltage balance. Therefore, the voltage pattern in Fig. 2(a) can be used to guarantee capacitor voltage balance in a three-level three-phase dc–ac converter. Obviously, the voltage of all three phases will be the same but phase-shifted one third of a fundamental cycle one from each other.

In order to correct any possible capacitor dc-link unbalance occurring due to the effect of phase current harmonics, unideal switch behavior, etc., a net positive or negative charge can be injected into the dc-link midpoint through breaking the symmetry of v_{acx} in Fig. 2(a). For instance, under the presence of a non-zero $i^{p}_{acx,1}$, the applied value of α in the positive and negative half cycles could be forced to be different. Alternatively, under the presence of a non-zero $i^{q}_{acx,1}$, the applied value of α in the inner part of the fundamental cycle (close to $\theta = \pi$) could be made different than the value of α in the outer part of the fundamental cycle (close to $\theta = 0$ and $\theta = 2\pi$).

Applying the Fourier series decomposition, the phase voltage in Fig. 2(a) can be expressed as

$$v_{acx} = \frac{V_{dc}}{2} + \sum_{h\ \text{odd}} b_h \cdot \sin(h\theta), \tag{2}$$

where the Fourier series coefficients can be found to be

$$b_h = \frac{2V_{dc}}{h\pi} \cdot \cos\left(h \cdot \left(\frac{\pi}{2} - \alpha\right)\right). \tag{3}$$

Forcing the amplitude of the fundamental component to be

$$b_1 = m_a \cdot \frac{V_{dc}}{\sqrt{3}}, \tag{4}$$

where $m_a \in [0, 2\sqrt{3}/\pi] \approx [0, 1.10]$ is the amplitude modulation index, the value of α can be isolated as a function of m_a as

$$\alpha = \frac{\pi}{2} - \cos^{-1}\left(\frac{m_a \pi}{2\sqrt{3}}\right). \tag{5}$$

Fig. 3(a) plots the resulting normalized value of α as a function of m_a. Fig. 4 presents the total harmonic distortion (THD) and weighted THD (WTHD) of the corresponding line-to-line voltage.

B. Four Levels

Fig. 2(b) presents the four-level phase voltage pattern with minimum number of switching transitions per fundamental cycle that can produce a phase voltage with adjustable fundamental-component amplitude. Angle α represents again the unique degree of freedom that can be used to adjust the fundamental-component amplitude. However, in this case, dc-link capacitor voltage balance is not feasible. The charge withdrawn from the inner dc-link point dc_2 is shown in red with a horizontal hatch pattern, while the charge from dc_3 is shown in green with a vertical hatch pattern. Although with regard to $i^{q}_{acx,1}$, the net charge is zero for both inner dc-link points due to symmetries, this is not the case with regard to $i^{p}_{acx,1}$, where both charges are different from zero, one positive and the other negative. This will lead to the collapse of some capacitor voltages. The problem arises from the fact that the connections to each inner dc-link point (dc_2 and dc_3) are restricted to only one half of the fundamental cycle. In order to compensate the charge injected/drawn and enable capacitor voltage balance, it is necessary to introduce connections in the

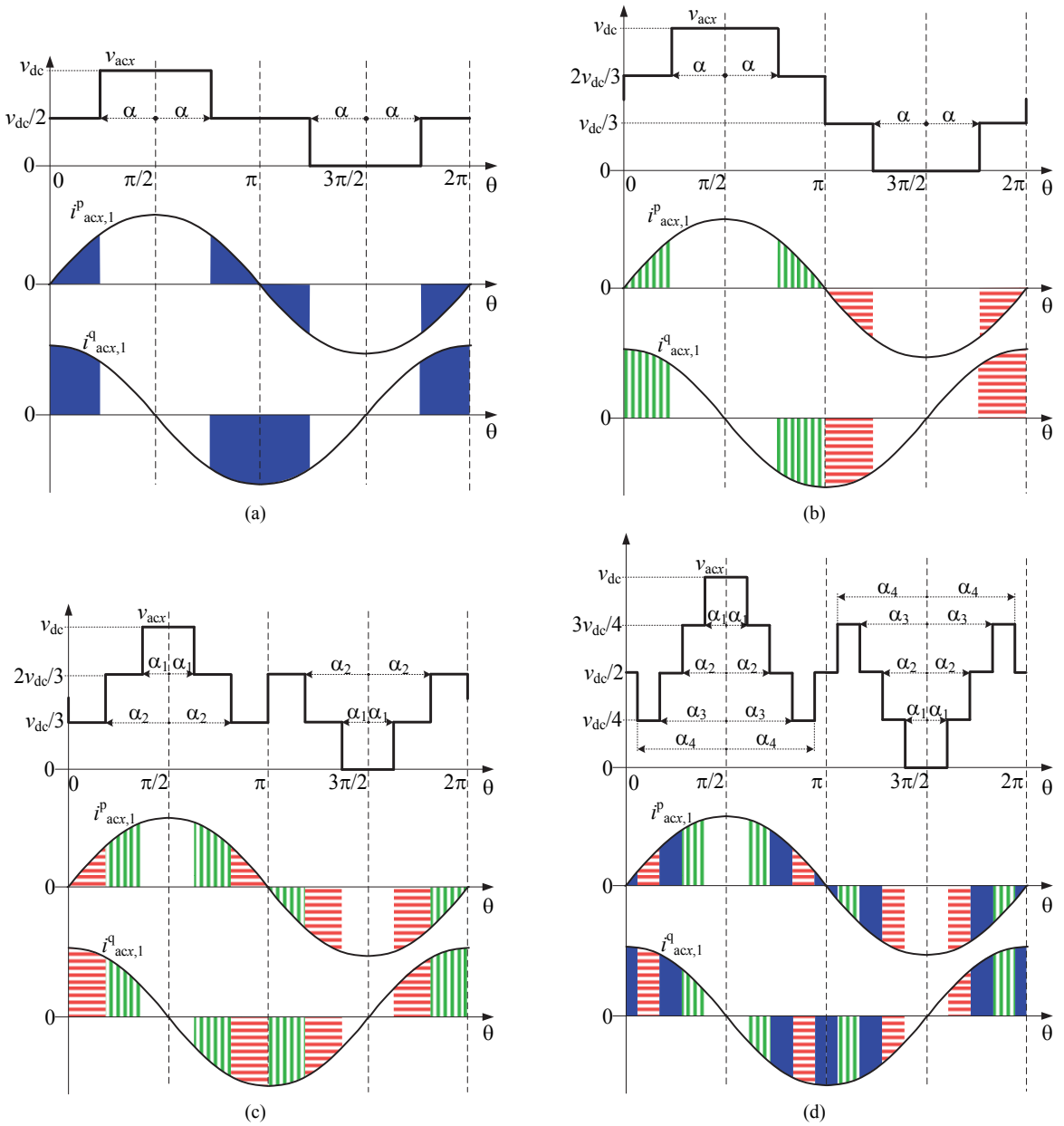

Fig. 2. Three-phase dc-ac converter phase voltage patterns with minimum number of switching transitions per fundamental cycle that can guarantee capacitor voltage balance. (a) Three-level case. (b) Four-level case: basic pattern that cannot guarantee capacitor voltage balance. (c) Four-level case: simplest pattern guaranteeing capacitor voltage balance. (d) Five-level case.

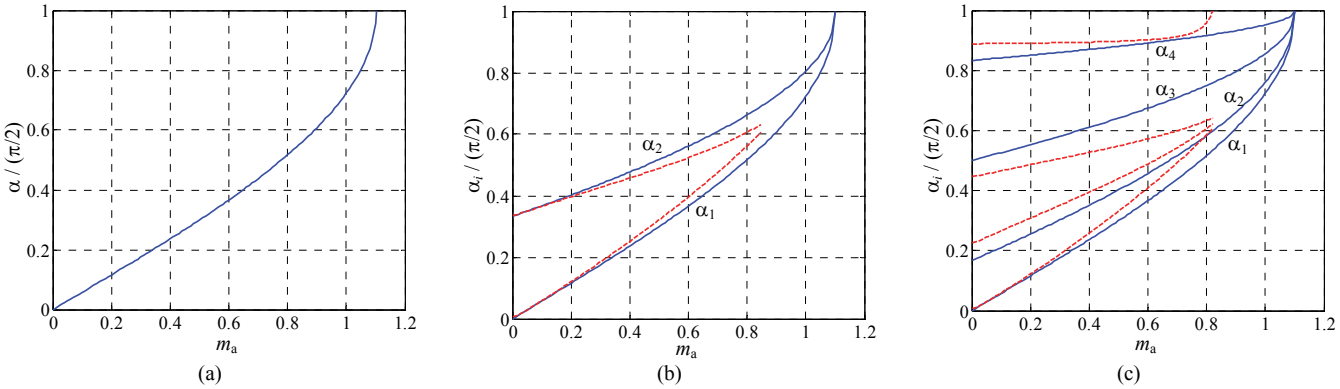

Fig. 3. Switching angles as a function of m_a with the modulation patterns of Fig. 2. Solid blue: values guaranteeing capacitor voltage balance. Dashed red: Values from the open-loop carrier-based modulation strategy illustrated in Fig. 8 with $m_f = 3$. (a) Three-level case (pattern of Fig. 2(a)). (b) Four-level case (pattern of Fig. 2(c)). (c) Five-level case (pattern of Fig. 2(d)).

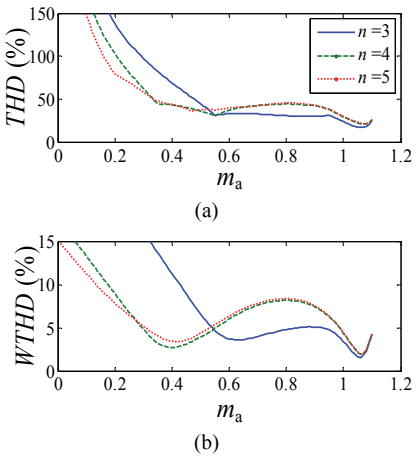

Fig. 4. Three-phase line-to-line voltage harmonic distortion figures as a function of m_a with the modulation patterns of Fig. 2. (a) THD. (b) WTHD.

other half cycle. This can be done with minimum number of switching transitions with the pattern presented in Fig. 2(c). This new pattern presents two degrees of freedom: α_1 and α_2.

As before, green and red areas cancel out with regard to $i^{q}_{acx,1}$. In addition, it can also be observed that a proper selection of angles α_1 and α_2 can force that green and red areas also cancel out with regard to $i^{p}_{acx,1}$, thus guaranteeing capacitor voltage balance.

The phase voltage can be expressed as in (2) with

$$b_h = \frac{4V_{dc}}{3h\pi}\cdot\left[-\frac{1}{2}+\cos\left(h\cdot\left(\frac{\pi}{2}-\alpha_1\right)\right)+\cos\left(h\cdot\left(\frac{\pi}{2}-\alpha_2\right)\right)\right]. \quad (6)$$

Equating the amplitude of the fundamental component to its expression in terms of the modulation index leads to

$$m_a = \frac{4\sqrt{3}}{3\pi}\cdot\left[-\frac{1}{2}+\sin(\alpha_1)+\sin(\alpha_2)\right]. \quad (7)$$

On the other hand, to force that both green and red areas cancel out with regard to $i^{p}_{acx,1}$, it must be verified that

$$\int_{0}^{\frac{\pi}{2}-\alpha_2}\sin(\theta)\cdot d\theta = \int_{\frac{\pi}{2}-\alpha_2}^{\frac{\pi}{2}-\alpha_1}\sin(\theta)\cdot d\theta, \quad (8)$$

which can be reduced to

$$0 = 1+\sin(\alpha_1)-2\sin(\alpha_2). \quad (9)$$

The values of α_1 and α_2 can be determined solving the nonlinear system of equations formed by (7) and (9). Fig. 3(b) plots the resulting normalized value of the two switching angles as a function of m_a. Fig. 4 presents the THD and WTHD of the corresponding line-to-line voltage.

C. Five Levels

The analysis of the five-level case again reveals that connections to the inner dc-link points are necessary in both fundamental half cycles to guarantee capacitor voltage balance. The phase voltage pattern with minimum number of switching transitions verifying this condition is presented in Fig. 2(d). This pattern features four degrees of freedom (α_1, α_2, α_3, and α_4). The charge withdrawn from the inner dc-link point dc_2 is shown in red with a horizontal hatch pattern, while the charge from dc_3 is shown in solid blue, and the charge from dc_4 is shown in green with a vertical hatch pattern. Red, blue, and green areas cancel out with regard to $i^{q}_{acx,1}$. Blue areas also always cancel out with regard to $i^{p}_{acx,1}$. With a proper selection of the switching angles, red and green areas will also cancel out with regard to $i^{p}_{acx,1}$.

The phase voltage can be expressed as in (2) and from equating the amplitude of the fundamental component to its expression in terms of the modulation index, the following expression is obtained

$$m_a = \frac{\sqrt{3}}{\pi}\cdot\left[\sin(\alpha_1)+\sin(\alpha_2)+\sin(\alpha_3)-\sin(\alpha_4)\right]. \quad (10)$$

The condition for capacitor voltage balance is

$$\int_{\frac{\pi}{2}-\alpha_4}^{\frac{\pi}{2}-\alpha_3}\sin(\theta)\cdot d\theta = \int_{\frac{\pi}{2}-\alpha_2}^{\frac{\pi}{2}-\alpha_1}\sin(\theta)\cdot d\theta, \quad (11)$$

which can be reduced to

$$0 = \sin(\alpha_1)-\sin(\alpha_2)-\sin(\alpha_3)+\sin(\alpha_4). \quad (12)$$

Equations (10) and (12) are not enough to fully determine the four independent switching angles. Two additional equations are necessary. These additional equations could be obtained from enforcing the elimination or mitigation of certain phase voltage harmonics, or from other design objectives. However, this is considered to be beyond the scope of this paper. Here, for the sake of simplicity and symmetry, the two additional equations will enforce a phase voltage pattern where the dwell time of each phase voltage step is equal from $\theta = \pi/2+\alpha_2$ to $\theta = 3\pi/2-\alpha_2$; i.e.,

$$\begin{aligned} 2\cdot(\pi/2-\alpha_4) &= \alpha_4-\alpha_3 \\ 2\cdot(\pi/2-\alpha_4) &= \alpha_3-\alpha_2. \end{aligned} \quad (13)$$

Equation (13) also ensures an even distribution of the regulation margin of the different dc-link capacitor voltage control loops.

The values of α_1, α_2, α_3, and α_4 can be determined solving the nonlinear system of equations formed by (10), (12), and (13). Fig. 3(c) plots the resulting normalized value of the four switching angles as a function of m_a. Fig. 4 presents the THD and WTHD of the corresponding line-to-line voltage.

D. Extension to n Levels

From the analysis of the three-, four- and five-level cases in the preceding subsections, the phase voltage pattern for the general n-level case can be induced and is presented in Fig. 5. The pattern features connections to each inner dc-link point in both fundamental half-cycles to be able to guarantee capacitor voltage balance. This is achieved with quarter-wave symmetry and minimum number of switching transitions.

The number of degrees of freedom (independent switching angles) is $n-2+\lfloor(n-3)/2\rfloor$.

III. Extension to Higher Number of Switching Transitions and Higher Number of Phases

Section II has presented the phase voltage pattern for an n-level three-phase dc-ac converter able to keep capacitor voltage balance with minimum number of switching transitions. In this section, the aim is to extend this solution to

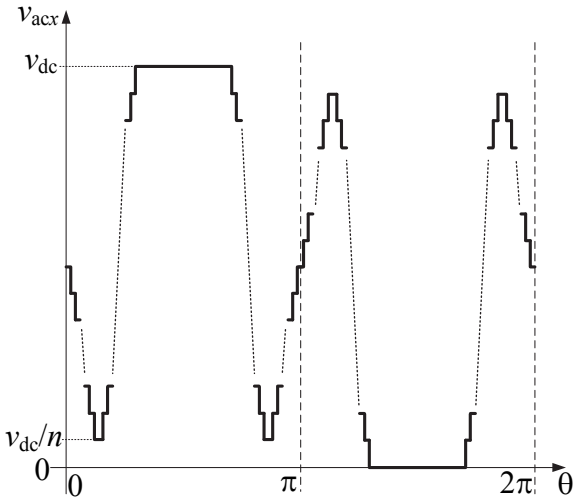

Fig. 5. General n-level three-phase dc-ac converter phase voltage pattern with minimum number of switching transitions that can guarantee capacitor voltage balance. The figure illustrates the odd n case.

a general case. First, phase voltage patterns also guaranteeing capacitor voltage balance but with a higher number of switching transitions per fundamental cycle (and improved harmonic distortion/lower filtering needs) are proposed. Second, the extension of these voltage patterns to any number of converter ac-side phases is also presented.

A. Carrier-Based Implementation of the Modulation Strategy presented in Section II

As will be shown next, the phase voltage pattern of the modulation strategy proposed in Section II can be generated through a specific carrier-based (CB) modulation with suitable parameter values. This will greatly simplify the task of extending the modulation strategy presented in Section II to higher number of switching transitions per fundamental cycle and higher number of phases.

Fig. 6 shows the leg duty ratio pattern of an n-level three-phase dc-ac converter when operated with the PWM strategy in [18], designed to operate with capacitor voltage balance in every switching cycle at switching frequencies much higher than the fundamental frequency. Variable $d_{x,y}$ represents the duty ratio of the ac_x terminal connection to dc-link point dc_y. As presented in [19], this PWM can be carrier-based (CB) implemented through defining a set of modulating waveforms per leg to be compared to a single triangular carrier signal. The ratio of the carrier frequency (f_c) to the fundamental frequency (f_o) is defined as the frequency modulation index ($m_f = f_c / f_o$). Fig. 7 illustrates the modulating waveforms in the case of a four-level three-phase converter. At any point in time, the number of modulating waveforms below the carrier plus one defines the dc-link point number to which the leg ac terminal is connected.

It turns out that the same phase voltage patterns presented in Section II for an n-level three-phase dc-ac converter can be generated by applying this CB modulation strategy with m_f = 3, as can be seen in the four-level-case example of Fig. 8. The phase voltage pattern is the same, but the values of the switching angles, although similar, are not the same. Fig. 3(b)

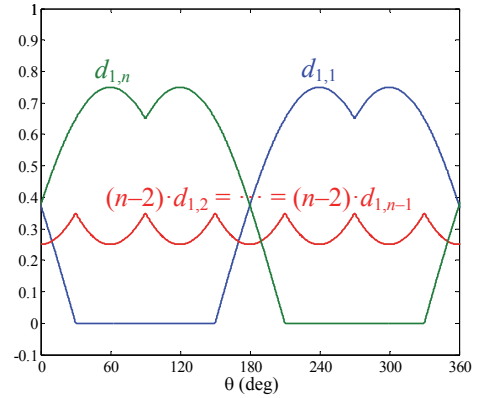

Fig. 6. Leg duty-ratio pattern of the PWM presented in [18] for an n-level three-leg converter at m_a = 0.75. The plotted waveforms correspond to leg 1. The duty ratios for legs 2 and 3 are the same but phase-shifted ±120º.

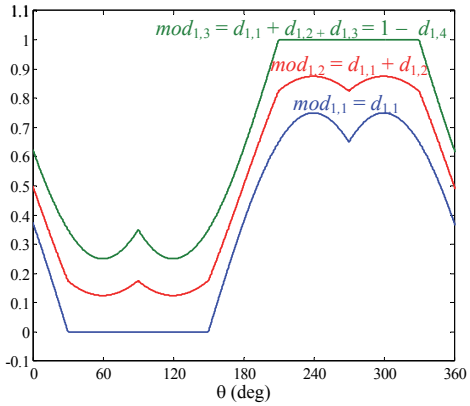

Fig. 7. Modulating waveforms to CB implement the PWM strategy defined in Fig. 6 for a four-level three-phase converter at m_a = 0.75 [19]. The plotted waveforms correspond to leg 1. The modulating waveforms for legs 2 and 3 are the same but phase-shifted ±120º. The triangular carrier signal, not shown here and common to all legs, oscillates between 0 and 1.

and Fig. 3(c) show a comparison of the switching angles computed in Section II (solid blue) to achieve capacitor voltage balance and the switching angles obtained through the CB approach (dashed red) over a limited range of m_a. Since the CB approach does not produce exactly the same angles, it will, in principle, lead to capacitor voltage unbalance. However, this CB modulation strategy can also be combined with a closed-loop capacitor voltage balance control [21], [22], which modifies the modulating signals in order to reach capacitor voltage balance. The introduction of such control allows the correction of the initial switching angles to match the necessary switching angles (solid blue lines in Fig. 3) to preserve capacitor voltage balance. This is illustrated in Fig. 9 for the four-level case of Fig. 8. It should be noted that the modulating signals in Fig. 9 have been modified with reference to Fig. 8 by the closed-loop control, in order to produce the desired switching angles. This closed-loop capacitor voltage balance control is anyway necessary to correct unbalances occurring due to the effect of phase current harmonics, non-idealities in converter behavior (switch behavior mismatch, dwell time perturbations, leakage currents, etc.), or special operating conditions. Thus, introducing such control does not increase the operating complexity. To reach

high values of the modulation index up to the maximum value $m_a = 2\sqrt{3}/\pi \approx 1.10$, it may be necessary to apply proper modulating waveforms corresponding to the overmodulation region as defined, for example, in [20].

The possibility of implementing the presented modulation strategy with this CB approach brings two benefits:

1) It allows a simple implementation of the proposed modulation strategy consistent with the implementation at high m_f values.

2) It easily reveals the proper phase voltage patterns guaranteeing capacitor voltage balance at higher number of switching transitions per fundamental cycle and higher number of phases, by simply modifying the carrier waveform parameters; i.e., the carrier phase-shift and the m_f value.

Regarding this last point, for instance, if the carrier waveform of Fig. 8 is phase shifted 180º, a novel phase voltage pattern capable of guaranteeing capacitor voltage balance results, as shown in Fig. 10. This new phase voltage pattern, presented in Fig. 11 for the n-level case, presents four more switching transitions per fundamental cycle compared to the pattern in Fig. 5, regardless of the value of n.

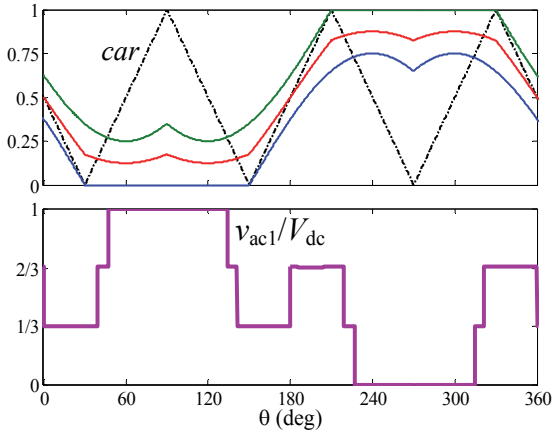

Fig. 8. CB implementation of the modulation pattern in Fig. 2(c) through the CB PWM strategy presented in Fig. 7 ($m_a = 0.75$) with $m_f = 3$.

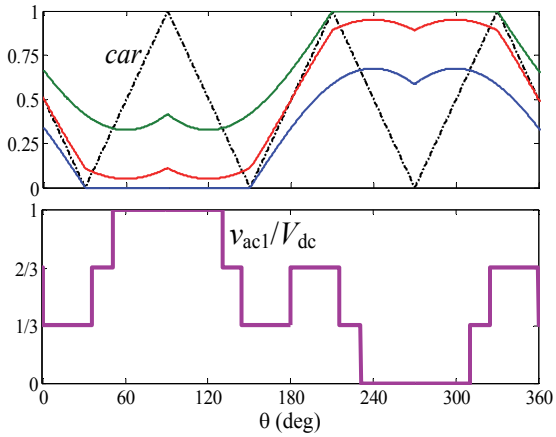

Fig. 9. Steady-state modulating waveforms and phase voltage pattern under the CB approach in Fig. 8 with a closed-loop capacitor voltage balancing control that modifies the modulating waveforms to achieve capacitor voltage balance. The resulting switching angles match those indicated with blue solid lines in Fig. 3(b).

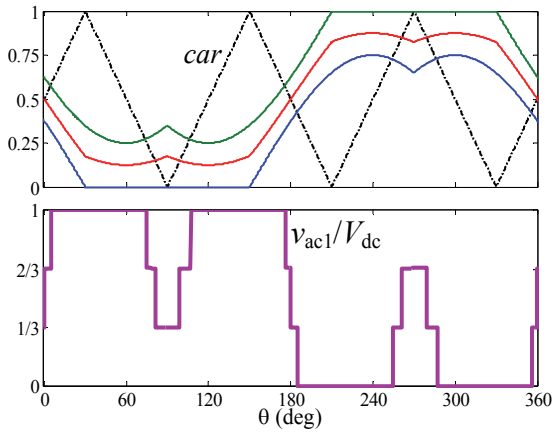

Fig. 10. Alternative modulation pattern obtained by phase-shifting 180º the carrier signal in Fig. 8.

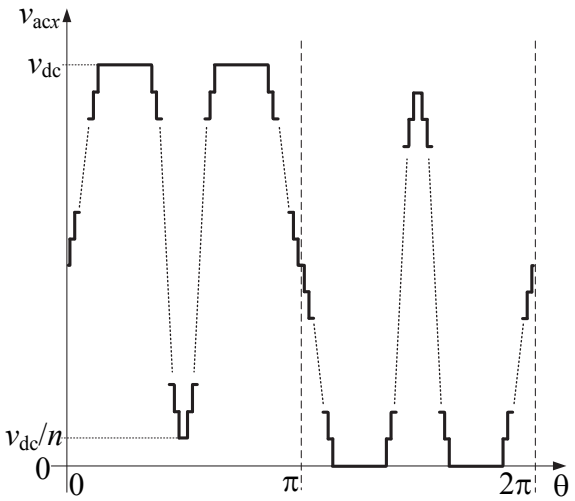

Fig. 11. Alternative n-level three-phase dc-ac converter phase voltage pattern with low number of switching transitions per fundamental cycle that is capable of guaranteeing capacitor voltage balance. The figure illustrates the odd n case.

B. Extension of the Modulation Pattern through Adjusting m_f

In order to produce phase voltage patterns able to keep capacitor voltage balance with higher number of switching transitions per fundamental cycle and/or higher number of phases, it is only necessary to modify the value of m_f. Parameter m_f should be set to an odd integer, multiple of the number of phases. This requires an odd number of phases. For instance, in a three-phase system, the recommended values would be $m_f \in \{3, 9, 15, 21,\ldots\}$. In a five-phase system, the recommended values would be $m_f \in \{5, 15, 25, 35,\ldots\}$. Parameter m_f should be set to an integer multiple of the number of phases, because then, the same voltage waveform is obtained for all phases (although, obviously, with some phase-shift) with a unique carrier signal for all phases. This results in low harmonic distortion compared to other options. On the other hand, m_f should also be an odd integer to force half-wave symmetry in the phase voltage waveform, thus eliminating even-order harmonics.

IV. Simulation and Experimental Results

Simulations have been carried out in MATLAB-Simulink to study the performance of the proposed modulation strategy. The modelled system consists of an n-level p-leg dc-ac converter (as in Fig. 1) that feeds a p-phase load from a single dc-voltage source regulating the value of V_{dc}.

The common simulation parameter values are gathered in Table I. The full dc-voltage is fixed at $V_{dc} = (n-1)\cdot 50$ V. The fundamental frequency is fixed at $f_o = 1$ kHz to emulate the case of a motor drive operating at high speed. Operating with a high fundamental frequency reduces the required size of the dc-link capacitors for a given capacitor voltage ripple specification, which simplifies the experimental prototype implementation. On the other hand, the value of f_o is irrelevant to validate the balancing properties of the proposed modulation strategy. The performance of the system would be analogous if operated with a lower fundamental frequency, higher dc-link capacitance, and the same m_f value. Two possible loads are simulated: a p-phase sinusoidal current source at the fundamental frequency (S load) with amplitude I_L and phase shift φ_L with reference to the fundamental component of the phase voltage; and a wye-connected p-phase series resistive-inductive load (RL load) with per-phase resistance R_L and inductance L_L. Cases with three, four, and five levels and three and five phases have been simulated.

Figs. 12-15 present simulation results under different scenarios. Fig. 12 proves that the open-loop modulation strategies presented in Section II, implemented from a lookup table (LT) with the value of the switching angles as a function of m_a in Fig. 3, maintain the capacitor voltage balance under a sinusoidal phase current at the fundamental frequency with both non-zero in-phase and in-quadrature components; i.e., they produce and average value of the inner dc-link point currents equal to zero. In Fig. 13(a) an RL load is connected to a four-level three-phase converter with the same open-loop modulation strategy of Fig. 12(b). As can be observed, the existence of phase current harmonics induces an increasing capacitor voltage unbalance. This can be easily solved by including a closed-loop capacitor voltage balancing control. Fig. 16 proposes one option to implement such control. Switching angle α_1 is divided into α_{p1} in the positive half-cycle and α_{n1} in the negative half-cycle. The values of α_{p1} and α_{n1} are then determined from the closed-loop control structure of Fig. 16(b) in order to inject/draw the proper charge into/from the inner dc-link points and achieve the command capacitor voltage values v^*_{C1}, v^*_{C2}, and v^*_{C3}. This closed-loop control is different from the control presented in [21]. One of the main differences is that it directly modifies the switching angle values instead of modifying the modulating signals and the resulting variation of the phase voltages is different than in [21]. The use of this closed-loop control allows keeping capacitor voltage balance in the presence of ac phase current harmonics, as shown in Fig. 13(b). It also ensures capacitor voltage control under other converter non-idealities. In Fig. 13(c), the control is tested with satisfactory performance under a step change in command voltages from (v^*_{C1}, v^*_{C2}, v^*_{C3}) = (50, 50, 50) V to (v^*_{C1}, v^*_{C2}, v^*_{C3}) = (47.5, 55, 47.5) V at $t = 5$ ms. Fig. 14 shows how these modulation patterns can also be implemented with the CB modulation strategy defined in [19] together with the closed-loop control presented in [21] and [22]. In Fig. 14(a), a proper performance in a four-level three-phase converter with $m_f = 3$ is verified. The resulting phase voltage pattern is the same as in Fig. 13(b). In Figs. 14(b)-(c), the frequency modulation index is increased to $m_f = 9$ and $m_f = 15$ to show that this CB approach easily allows extending the four-level three-phase modulation strategy to a higher number of switching transitions per fundamental cycle while keeping the capacitor voltage balance. Figs. 14(d)-(f) prove the good performance of the CB approach in a five-level five-phase converter with $m_f = 5$, $m_f = 15$, and $m_f = 25$, respectively. As m_f increases, the converter performance approaches the performance obtained by the corresponding high-m_f PWM strategy [19], as expected.

TABLE I
Simulation Conditions

General	
$V_{dc} = (n-1)\cdot 50$ V	$f_o = 1$ kHz
$C_1 = C_2 = C_3 = 150$ μF	$m_a = 0.75$
Sinusoidal Current Load (S Load)	
$I_L = 6$ A	$\varphi_L = -35°$
Resistive-Inductive Load (RL Load)	
$R_L = 8.25$ Ω	$L_L = 1$ mH
Closed-Loop Control	
$V^*_{C1}=V^*_{C2}=V^*_{C3} = 50$ V	
$G_c(s) = G_{c0}\cdot[1+s/(2\pi)]/[s\cdot[1+s/(100\pi\cdot m_f)]]$	

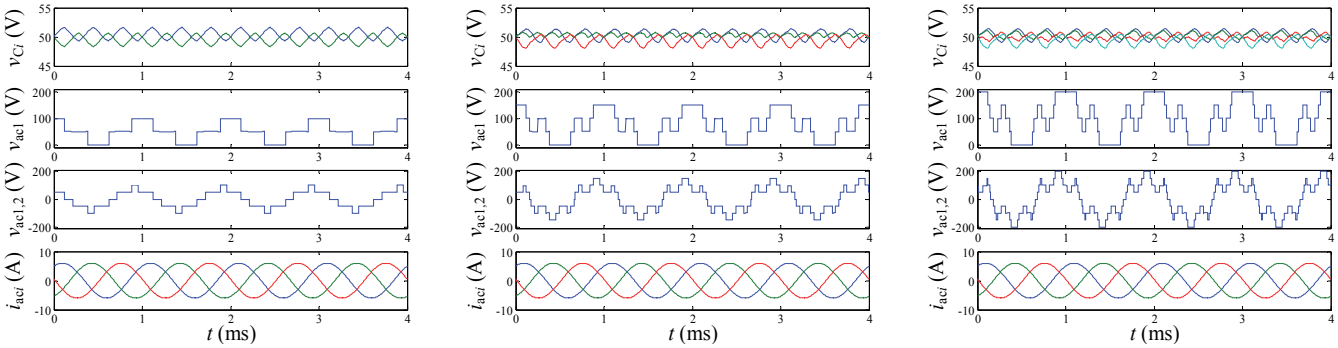

Fig. 12. Simulation results for the dc-link capacitor voltages v_{Ci}, phase voltage v_{ac1}, line-to-line voltage $v_{ac1,2}$, and phase currents i_{aci} in a n-level three-phase (p = 3) dc-ac converter under a LT implementation, S Load, and no closed-loop control ($G_{c0} = 0$). Y-axis range for v_{ac1} and $v_{ac1,2}$ are [-10 V, 210 V] and [-210, 210] V, respectively. Voltages v_{ac1} and $v_{ac1,2}$ present voltage steps equal to the dc-link capacitor voltages, which are all approximately equal to 50 V. The peak value of i_{aci} is 6 A. (a) $n = 3$. (b) $n = 4$. (c) $n = 5$.

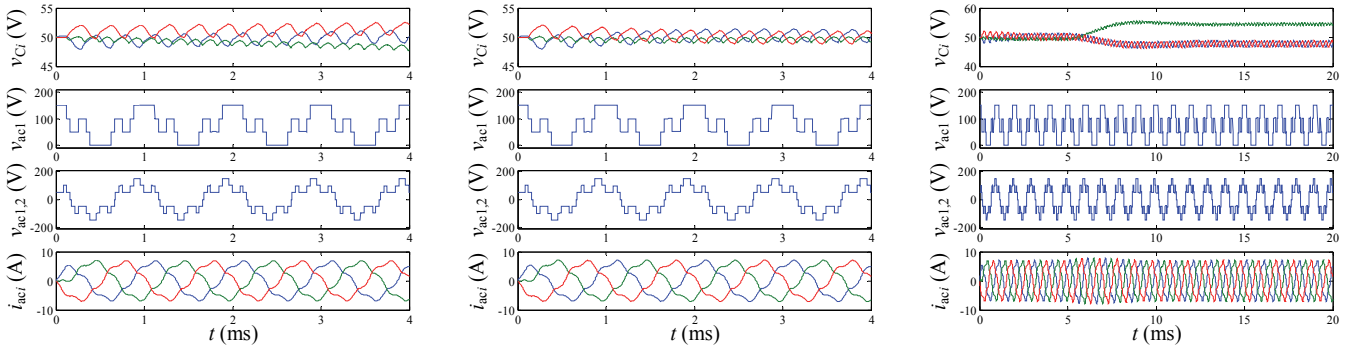

Fig. 13. Simulation results for a four-level three-phase dc-ac converter (n = 4, p = 3) under a LT implementation and RL load. The peak value of the fundamental component of i_{aci} is 6.3 A. (a) G_{c0} = 0 (no closed-loop control). (b) G_{c0} = 0.5. (c) G_{c0} = 0.3, step change in command capacitor voltages at t = 5 ms.

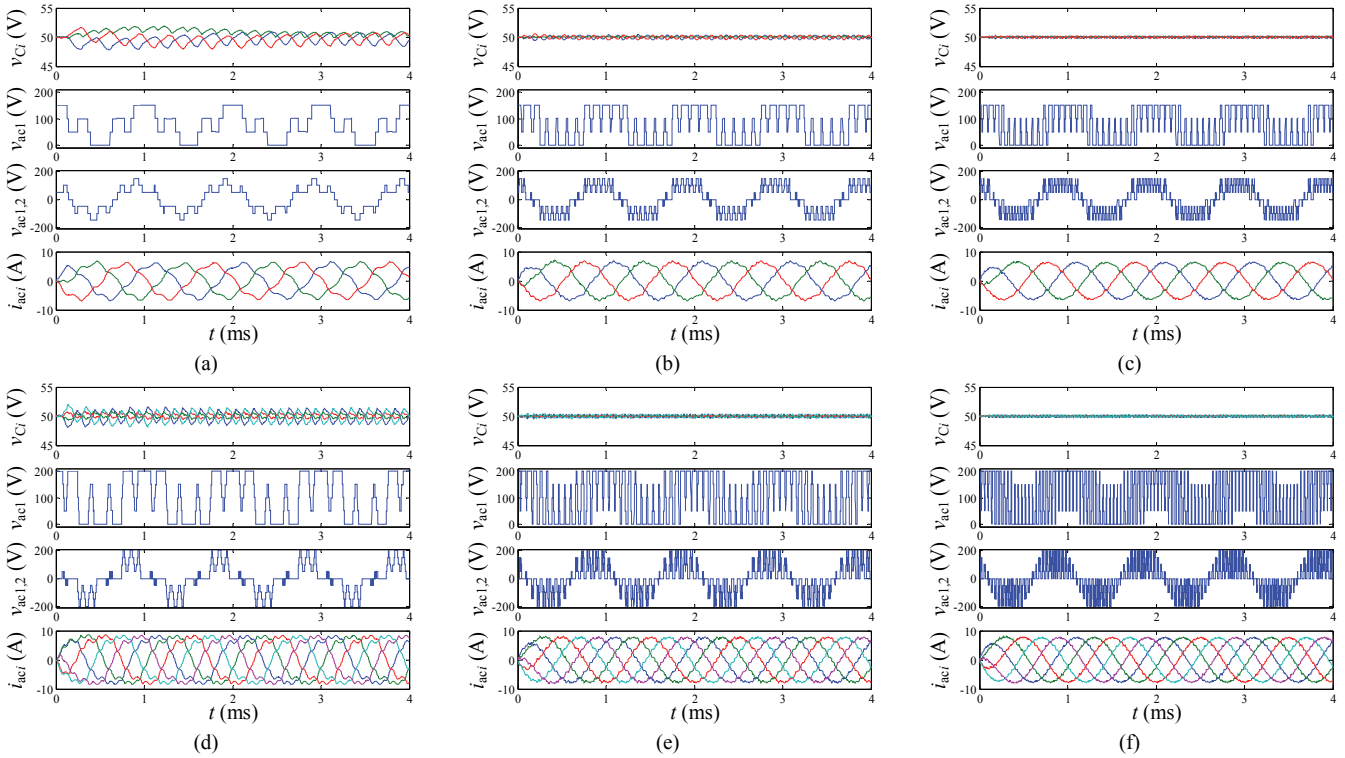

Fig. 14. Simulation results for an n-level p-phase dc-ac converter under a CB implementation and RL load. The peak value of the fundamental component of i_{aci} is 6.3 A in cases (a), (b), and (c), and it is 8.3 A in cases (d), (e), and (f). (a) n = 4, p = 3, m_f = 3, G_{c0} = 1. (b) n = 4, p = 3, m_f = 9, G_{c0} = 0.5. (c) n = 4, p = 3, m_f = 15, G_{c0} = 0.5. (d) n = 5, p = 5, m_f = 5, G_{c0} = 0.5. (e) n = 5, p = 5, m_f = 15, G_{c0} = 0.5. (f) n = 5, p = 5, m_f = 25, G_{c0} = 0.5.

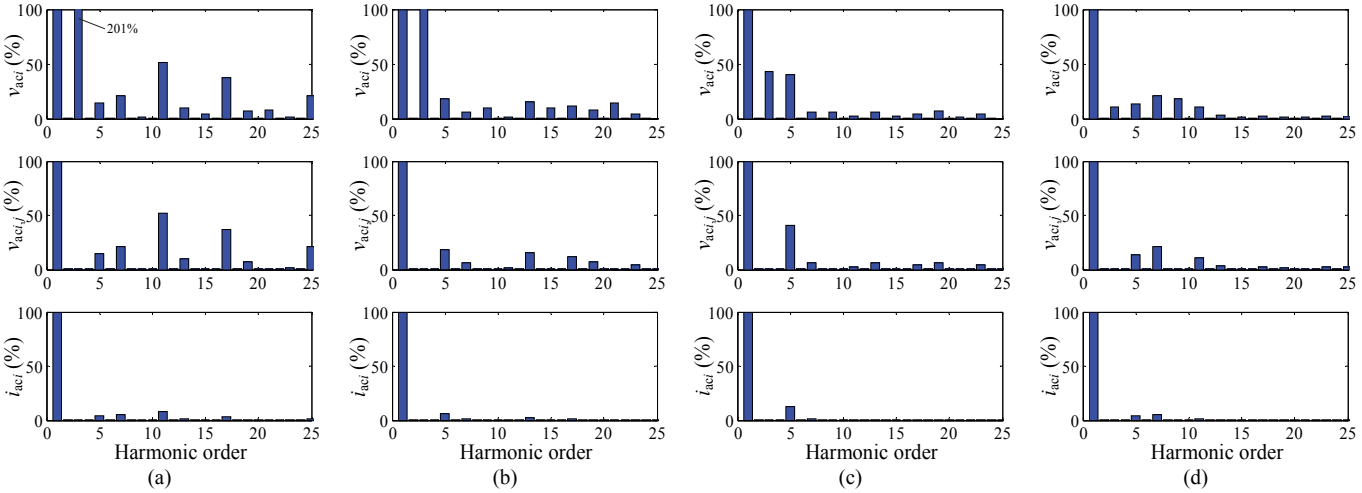

Fig. 15. Harmonic spectrum of phase voltage, line-to-line voltage, and phase current in the conditions of Fig. 13(b) under different amplitude-modulation-index values. (a) m_a = 0.25. (b) m_a = 0.5. (c) m_a = 0.75. (d) m_a = 1.

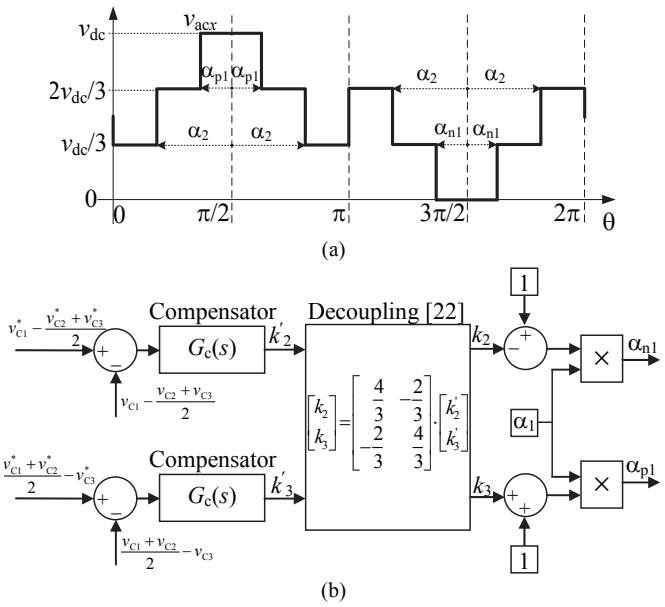

Fig. 16. Closed-loop capacitor voltage balance control for a four-level three-phase dc-ac converter. (a) Phase voltage pattern. (b) Control block diagram.

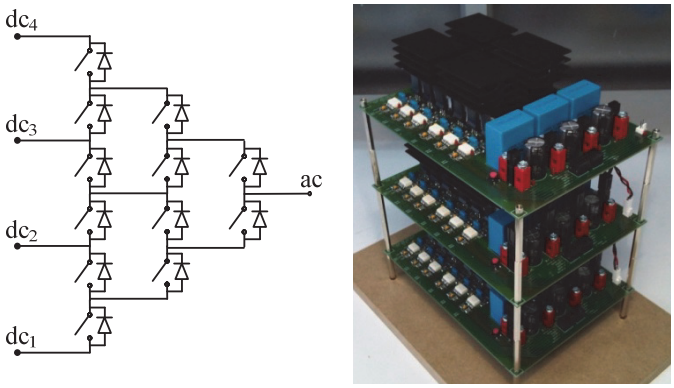

Fig. 17. Experimental prototype. (a) Four-level active-clamped leg topology [3]. (b) Four-level three-phase dc-ac converter with dc-link capacitors.

To illustrate the harmonic performance of the proposed modulation strategy under the worst case conditions (minimum number of switching transitions per fundamental cycle), Fig. 15 presents the harmonic spectrum of phase voltage, line-to-line voltage, and phase current in the conditions of Fig. 13(b) (four-level three-phase converter) under different amplitude-modulation-index values. It can be observed that an appreciable fifth harmonic results in the phase currents. For higher number of converter levels, this low-order harmonic may be mitigated thanks to the availability of extra degrees of freedom in the modulation strategy, as has been discussed in Section II.C. If higher number of switching transitions per fundamental cycle are possible, the appreciable harmonics in line-to-line voltages move towards higher orders, leading to fairly sinusoidal phase currents.

Experiments have also been carried out with a four-level three-phase active-clamped dc-ac converter prototype built upon 100-V metal-oxide semiconductor field-effect transistors (Fig. 17), and controlled with a dSPACE control platform. The experiments have been performed in the conditions of Table I and Fig. 13, unless otherwise specified. Fig. 18(a)-(c) prove the proper performance of the modulation strategy in steady-state over a wide amplitude-modulation-index range (m_a = {0.25, 0.75, 1.05} where the theoretical maximum value of m_a is approximately 1.10, corresponding to six-step operation). The dc-link capacitor voltages are balanced in all cases since the phase voltages present steps with equal amplitude. Fig. 18(d) also verifies the good dynamic performance of the closed-loop control under a step change in the capacitor voltage commands. The experimental results depicted in Fig. 18(b) and Fig. 18(d) corroborate the corresponding simulation results from Fig. 13(b)-(c).

V. Discussion

With the aim of enabling a reduction of switching losses in multilevel multiphase diode-clamped converters, Section II has presented the phase voltage pattern (Fig. 5) with minimum number of switching transitions that allows both adjusting the ac voltage fundamental-component amplitude and keeping the dc-link capacitor voltages balanced. The resulting phase voltage patterns contain more switching transitions than it is typically observed in other multilevel topologies. But this is an unavoidable drawback of diode-clamped topologies to make their operation feasible, since the dc-link capacitor voltages must remain balanced, and simpler phase voltage patterns with lower number of switching transitions would make some capacitor voltages collapse and others increase too much, as discussed in Section II. On the other hand, other multilevel topologies that can operate with simpler phase voltage patterns are able to do so at the expense of requiring energy storage components within the leg. Therefore, there is a tradeoff between switching losses and the size of the required energy storage elements; i.e., diode-clamped topologies have the advantage of a more compact leg implementation at the expense of presenting higher overall switching losses. Section III has extended the phase voltage pattern derived in Section II to higher frequency modulation index values and number of phases, for cases where it is best to operate under these conditions.

The CB modulation approach presented in [19] was conceived to operate diode-clamped multilevel multiphase converters under high m_f values, where the phase currents can be assumed constant over the switching cycle. The analysis presented in the preceding sections has revealed that it also produces proper phase voltage patterns under low m_f values if proper m_f values (odd multiples of the number of phases) and carrier phase-shift values are selected. However, although a proper phase voltage pattern is achieved, the open-loop modulation leads to a wrong value of the switching angles, as observed in Fig. 3. This means that the modulation in [19] initially leads to a significant capacitor voltage unbalance and that a closed-loop control [21] will have to do a substantial effort to recover the balance. Thus, the solution that combines the CB modulation in [19] with the control in [21] is less efficient than using a LT with the correct switching angle values obtained through solving the corresponding system of

nonlinear equations and combined with a closed-loop control to fix minor deviations. This can be seen comparing Fig. 13(b) (LT approach) and Fig. 14(a) (CB approach). The CB approach takes much longer to reach capacitor voltage balance, despite using a compensator gain twice the value used in the LT implementation approach. On the other hand, a simple extension of the CB modulation to the overmodulation region is not obvious, while the approach based on solving the non-linear system of equations easily provides the proper switching angle values for this region.

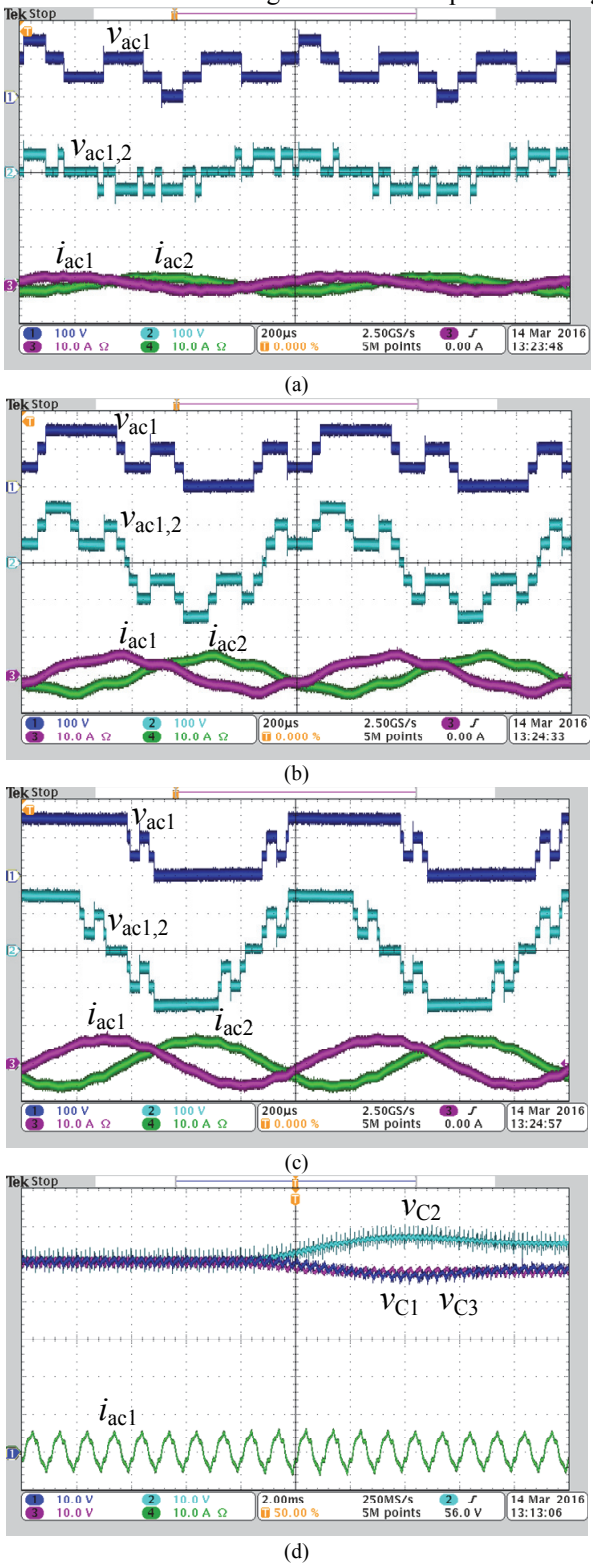

Fig. 18. Experimental results in a four-level three-phase dc-ac converter in the conditions of Table I and Fig. 13 (V_{dc} = 150 V, LT implementation, RL load, and G_{c0} = 0.3). (a) Steady-state with m_a = 0.25. (b) Steady-state with m_a = 0.75. (c) Steady-state with m_a = 1.05. (d) Step change in command capacitor voltages from (v^*_{C1}, v^*_{C2}, v^*_{C3}) = (50, 50, 50) V to (v^*_{C1}, v^*_{C2}, v^*_{C3}) = (47.5, 55, 47.5) V with m_a = 0.75.

Based on the above discussion, it can be concluded that:

1) In constant-fundamental-frequency applications with a low number of switching transitions per fundamental cycle (i.e., constant-and-low m_f applications), the optimal solution from both a performance and implementation simplicity point of view is to use the LT approach.

2) In variable-fundamental-frequency applications (i.e., applications with a range of m_f values, such as for example variable speed motor drives), there are two meaningful options:

2a) Use the LT approach for low m_f values and use the CB approach for high m_f values. This would lead to the best performance.

2b) Use the CB approach for the full m_f range. This would lead to the simplest controller.

VI. Conclusion

This paper has presented a novel modulation strategy for diode-clamped (and functionally equivalent) multilevel three-phase dc-ac converters that is capable of maintaining dc-link capacitor voltage balance with the minimum number of switching transitions per fundamental cycle. Through a CB implementation, the modulation strategy has been extended to higher number of switching transitions per fundamental cycle and higher number of phases, proving that the operation of this converter family in the absence of additional auxiliary balancing hardware is feasible for any number of levels and phases at low frequency modulation indices. In addition, the proposed modulation pattern naturally converges to the modulation strategy proposed in [19] to guarantee capacitor voltage balance under high m_f. This facilitates the use of these converters in applications requiring operation with a low m_f, and in applications with a wide range of operating m_f, including low m_f values, such as in variable-speed motor drives.

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