Insights to Memristive Memory Circuits from Reliability Aspects

Peyman Pouyan, Esteve Amat, Antonio Rubio
Dept. of Electronic Engineering
UPC Barcelona Tech, Barcelona Spain
peyman.pouyan, esteve.amat, antonio.rubio@upc.edu

***Abstract*—The scaling roadmap for realization of more than Moore in semiconductor industry has resulted in emergence of new types of devices, among them, memristive devices seem to be a promising candidate to be applied in various applications such as in memories and neuromorphic chips. However memristive devices face some challenges to be resolved before becoming a mainstream. This paper work analyzes two of the main reliability concerns in design of memristive memories, and proposes circuit solution to enhance the reliability.**

Keywords—Memritor; reliability; process variability; endurance; crossbar; RRAM; reconfiguration; emerging device.

I. INTRODUCTION

The Memristor's discovery goes back to about 40 years ago when the properties of nonlinear circuit theory was being investigated by Professor Leon Chua at university of California Berkeley. Chua proposed the existence of a fourth element called the memory resistor by examining the relationships between charge and flux in resistors, capacitors, and inductors in his paper []. However the Memristor was not given high attention until recently, because the property of a material was, too subtle to make use of it. In 2008 HP presented a manufactured Memristor in titanium dioxide [], which its resistance value could vary according to the current passing through it and could remember that value even after the current was disappeared.

As more research work was done in the field and more devices were showing Memristive-like behavior in 2012 Chu redefined the Memristor device definition as any two terminal device that shows a hysteresis loop in the v-i plane by applying any bipolar periodic voltage or current waveform [], in other words he says "If it is pinched it is a Memristor". Regarding this, various types of non-volatile emerging devices are categorized of being Memristive, devices such as: Resistive Random Access Memories (ReRAM) [], Polymetric Memristor [], Ferroelectric Memristor [], Manganite Memristor and Spintronic []. They can all switch between low and high resistance state, have low power consumption and high scalability, therefore are very good candidates for future nano-scale memories. However these Memristive devices have different characteristics in comparison with each other and reliability is one of the main design considerations in their application for memory systems.

This paper analyzes the reliability concerns in two of the main Memristive types aims to give circuit solution to have more robust Memristive memory.

II. RELIABILITY CONCERNS IN MEMRISTIVE CIRCUITS

Different types of memristive devices have been analyzed from performance metrics in memories [] summarized in table I []. Among them, the resistive and spintronic memristors present promising specifications and therefore has attracted many recent research works [].

Table I. Memory performance metrics in Memristive types

Memristor	On/Off ratio	Access time (ns)	Endurance
Resistive	2000	~10	10^9
Polymetric	100	~25	10^8
Ferroelectric	300	~10	10^{14}
Manganite	100	~100	10^3
Spintronic	5	~10	10^{16}

As highlighted in the table resistive devices have decent on/off ratio, a favorable access time and a limited endurance, which might not be sufficient for embedded memory applications []. On the contrary observe that the spintronic devices have a high endurance value, appropriate access time and a low on/off ratio []. Therefore limited endurance value and low on/off ratio are the two reliability concerns to be considered in memory design with these devices.

The limited endurance value in resistive memristors mainly stems from their conductive filamentary switching characteristics [] that in each switching cycle a filament is created or ruptured to change the resistance value, therefore oxidation in the device electrodes, extra vacancies in the filament or ion deficiency degrade the device along the lifetime. On the other hand the spintronic memristors function based on changing the direction of the spin of electrons and therefore their resistance on/off ratio is small and needs to be considered for a robust memory operation. Moreover since both spintronic and resistive memristors are built in nano-scale dimensions therefore the impact of process variation on them originated from manufacturing step cannot be neglected.

Fig 1 presents an example for two distributions of on and off resistance values in memristive devices. Observe that when the two distributions are close (~2X) and might shift toward each other because of endurance, then the memory cell cannot operate reliably and read errors might occur. We have considered a reference resistance value (Rref) and then have introduced the parameter probability error (Pe), which determines the possibility of false read operation and plotted while sweeping the reference value along the two distributions.

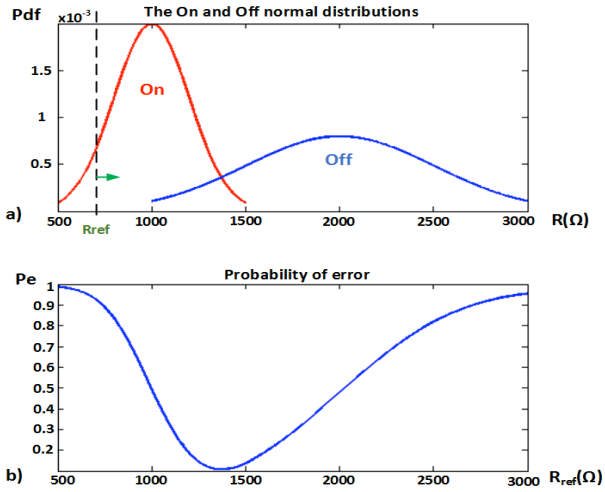
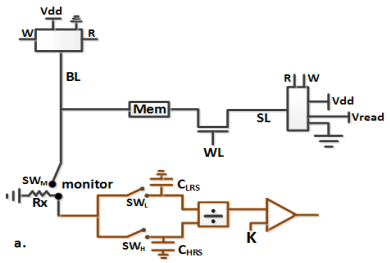


Figure 1. a) The distribution of On and Off resistance values b) The Pe graph in respect to sweeping a reference resistance value

The simultaneous impact of endurance and process variability can deteriorate the memristive memory operation and would reduce the lifetime, making it necessary to develop techniques, which can mitigate some part of their effect. Therefore in [] authors propose two reconfiguring schemes that enhance the memristor memory lifetime by shifting from the faulty unit to a healthy unit. These reconfiguring approaches are based on a dynamic testing of the memristive cells and determining their reliability metric for robust operation.

Fig 2.a presents a measurement technique which can evaluate the memristive cells in accordance with their on and off resistance value. Here the memristive cell is considered to be constructed with a resistive memristor in a 1T1R structure. Applying the appropriate signals through the peripherals would switch the memristive between the on and off resistance values and it would check the on/off ratio. If the memristive cell does not pass the test it is considered a faulty cell and the memory would reconfigure itself in accordance with its position. Fig 2.b presents an example for simulation of this sensing scheme in HSPICE and by utilizing the Standford RRAM model []. Note that this memristive cell presents an on off resistance ratio (~23) and can be operated reliably.



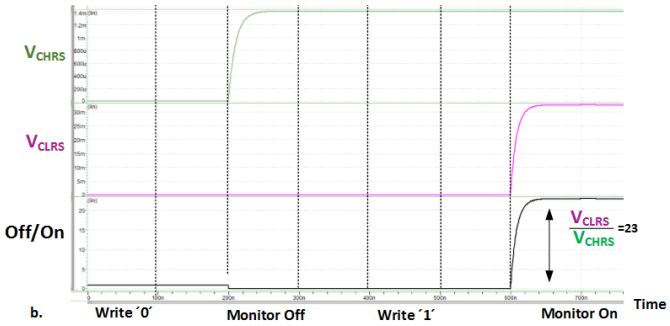


Figure 2. a) Testing circuit to monitor HRS and LRS values in crossbar implementation b) circuit simulation waveforms in HSPICE

III. Conclusion

In this paper, first, we have remarked some of the important reliability concerns in memristive devices to be applied in memories, such as the low on/off ratio and endurance. Then we have introduced a measurement mechanism to evaluate memristive devices and reconfigure the memory according to functional and reliable cells.

Acknowledgment

This work is funded by the Spanish MINECO and ERDF (TEC2013-45638-C3-2-R).

References

[1] www.ITRS.net

[2] H.-S. P. Wong, *et. al*, "Metal–Oxide RRAM," *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, 2012.

[3] L.O. Chua, "Memristor-The missing circuit element," *IEEE Transaction on Circuit Theory*, vol. 18, pp. 507-519,1971.

[4] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found.," *Nature*, vol. 453, no. 7191, pp. 80–3, 2008.

[5] B. R. Field-, D. Ielmini, "Modeling the Universal Set / Reset Characteristics of Filament Growth," *IEEE TED*, vol. 58, no. 12, pp. 4309–4317, 2011.

[6] S. Deora, *et. al*, "Ac Variability and Endurance Measurement for Resistive Switching Memories," *IEEE TDMR*, vol. 14, no. 1, pp. 300–303, 2013.

[7] B. Chen, *et. al*, "Physical mechanisms of endurance degradation in TMO-RRAM," *Proc IEDM*, pp. 12.3.1–12.3.4, 2011.

[8] Pouyan, E.Amat, A.Rubio; "Statistical Lifetime Analysis of Memristive Crossbar Matrix", to be appeared at *DTIS,* 2015.

[9] S. Hamdioui, S. Member, M. Taouil, and S. Member, "Testing Open Defects in Memristor-Based Memories," vol. 64, no. 1, pp. 247–259, 2015.

[10] S. Kannan, J. Rajendran, R. Karri, and O. Sinanoglu, "Sneak-Path Testing of Crossbar-Based Nonvolatile," vol. 12, no. 3, pp. 413–426, 2013.

[11] "Standford RRAM model" [on line], https://nano.stanford.edu/stanford-rram-model

[12] "HSPICE 2012", www.synopsys.com