

A Method for Real-Time Generation of Slew-rate Limited Envelopes in Envelope Tracking Transmitters

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Abstract — This paper shows a method for generating slew-rate limited envelopes in order to accomplish the slew-rate restrictions of the envelope driver in envelope tracking transmitters. The proposed algorithm can run in real-time and it is implemented in a digital front-end of a Software Radio system. Simulation results and conclusions are provided to validate the methodology. Moreover, experimental results of an FPGA implementation are also provided.

Index Terms — Efficient power amplifiers, envelope tracking, slew-rate.

I. INTRODUCTION

Current communications standards enhancing high data rates by means of multicarrier and spectrally efficient modulation schemes (i.e. OFDM-based modulations) require Power Amplifiers (PAs) handling signals that present high Peak-to-Average Power Ratios (PAPRs): this means a trade-off between linearity and efficiency [1]. Currently, to enhance power efficiency in power amplifiers (PA), power-supply control architectures are being used. Thanks to the capabilities offered by current digital signal processors, these architectures offer a great potential for high efficiency operation. The PA drain supply modulation is carried out using techniques such as envelope elimination and restoration (EER) and envelope tracking (ET) in conjunction with digital predistortion (DPD). From the implementation point of view, ET amplification systems (see Fig. 1) are very attractive techniques aimed at improving efficiency.

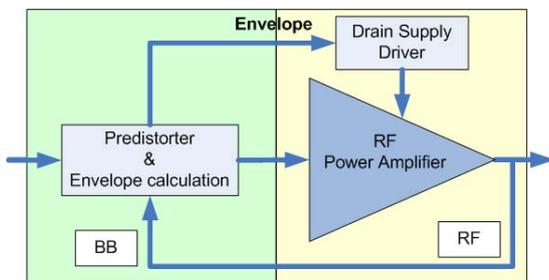


Fig 1. ET amplifier structure.

ET can be applied in conventional transmitters based on RF linear amplification topologies by only substituting the conventional static supply for a dynamic one. This dynamic supply can be considered as an envelope power amplifier. Its role is to efficiently supply the required voltages and currents to the RF transistor drain at the speed imposed by the changes of the RF envelope [1].

The scope of this paper is to present a new method for generating suitable signals (in terms of envelope speed and bandwidth) for exciting the envelope amplifier, critically limited by its slew-rate.

II. ENVELOPE DRIVER REQUIREMENTS

In OFDM-based modulations the envelope bandwidth is around 3-4 times the bandwidth of the baseband complex modulated signal. Then, one of the main challenges in ET envelope drivers is to supply the power required by the transistor at the same speed of the signal envelope. In recent works, some solutions based in iteratively reducing the bandwidth envelope [2] or reducing the PAPR [3] were shown. Our proposal is to generate a slew-rate reduced version of the RF signal envelope, because the typical speed restriction in power devices, as is the case of power supplies, is the slew-rate. This is a particular problem in DC-DC suppliers, where the necessary (for filtering purposes) output inductor has the unwanted effect of reducing the slew-rate.

III. PROPOSED METHOD FOR GENERATING SLEW-RATE LIMITED ENVELOPES

A. Definition of the functioning of the proposed algorithm

The purpose is to generate a slew-rate limited signal $E_s(t)$, that will show a slower envelope of the true RF envelope $E(t)$. Therefore, the following requirements must be accomplished:

i) The amplitude of the slower envelope has to be always higher than the RF signal envelope. It has to behave as an instantaneous upper bound of the true envelope, so this means $E_s(t) > E(t)$.

ii) It has to be able to track the limited slew-rate of the envelope amplifier.

iii) It has to be implementable in real-time in a digital signal processor such as an FPGA device.

The proposed method basically consist in taking the sampled value of the modulated envelope $E(n)$ (generated by the same digital signal processor that is used for running this algorithm, at time $t=nT_s$) and to generate $E_s(n)$ according to the present and future values of the envelope: $E(n+1)$, $E(n+2)$, etc. $E_s(n)$ is the slow envelope to be obtained processing the actual $E(n)$. The dynamic range is normalized to 1, so $0 < E(n) < 1$ and $0 < E_s(n) < 1$, and Δ_M is defined as the maximum increment of $E_s(n)$ allowed by the slew-rate restriction of the envelope amplifier. For a proper functioning of the algorithm the following considerations must be taken into account:

i) At each time n , the $E_s(n)$ increase or decrease cannot be higher than the restriction imposed by the maximum slope (thus the slew-rate) that the envelope amplifier is able to track.

ii) The inequality $E_s(n) > E(n)$ has to be accomplished at each n , so we need to know the future values of the envelope: $E(n+1)$, $E(n+2)$, ..., $E(n+N)$, being N the integer approximation of $1/\Delta_M$ and thus to ensure that after N times the inequality $E_s(n+N) > E(n+N)$ will be reached.

iii) Then, $E_s(n)$ is smothered by means of a low-pass filter, and this filtered envelope is called $E_{sf}(n)$.

iv) Finally, $E_{sf}(n)$ and the actual envelope $E(n)$ are time aligned and $E_{sf}(n)$ is send to the digital-to-analog converter (DAC) resulting in $E_{sf}(t)$.

B. Mathematical formulation of the algorithm

At time n the generated envelope, $E_s(n)$, must be at least $E(n+1) - \Delta_M$ in order to accomplish $E_s(n+1) > E(n+1)$, similarly, $E_s(n)$ must be at least $E(n+2) - 2\Delta_M$ in order to accomplish $E_s(n+2) > E(n+2)$, and so on. All these restrictions can be mathematically expressed as:

First, the minimum value allowed for $E_s(n)$ at time n , $y(n)$, is calculated. The inequality $E_s(n+i) > E(n+i)$ ($i=0,1\dots N$) can be achieved accomplishing the Δ_M restriction explained before. This is expressed by means of the following expression:

$$\begin{aligned} y(n) &= \max_{i=0,1,\dots,N} \{E(n+i) - i \cdot \Delta_M\} = \\ &= \max \left\{ E(n), E(n+1) - \Delta_M, E(n+2) - 2 \cdot \Delta_M, \dots \right. \\ &\quad \left. \dots, E(n+N-1) - (N-1) \cdot \Delta_M, E(n+N) - 1 \right\} \end{aligned} \quad (1)$$

Second, since the maximum value that can decrease the slow envelope (at each iteration/sample) is Δ_M , then $E_s(n)$ is chosen considering the maximum value between $y(n)$ or the

boundary for decreasing $E_s(n)$ that is defined as the previous value $E_s(n-1)$ minus Δ_M . Therefore $E_s(n)$ is defined as:

$$E_s(n) = \max\{y(n), E_s(n-1) - \Delta_M\} \quad (2)$$

For calculating the slow envelope some samples of the envelope must be known in advance, so the developed algorithm is not causal. For solving this it is necessary to apply a delay of N samples between the true envelope $E(n)$ and the slew-rate limited one, $E_s(n)$. Therefore, the previous equations defining the following remain:

$$\begin{aligned} \text{i)} \quad y(n-N) &= \max_{i=0,1,\dots,N} \{E(n-N+i) - i \cdot \Delta_M\} \\ \text{ii)} \quad E_s(n-N) &= \max\{y(n-N), E_s(n-N-1) - \Delta_M\} \end{aligned} \quad (3)$$

So, the modulated complex baseband signal has to be delayed also N samples to be aligned with the generated slew-rate limited envelope $E_s(n)$.

IV. SIMULATION RESULTS: MATLAB

Some simulation results, obtained considering an OFDM test signal, are shown in Fig. 2 and Fig. 3. There is a trade-off between the ability of $E_{sf}(t)$ for tracking the RF signal envelope and the efficiency improvement. We define the efficiency improvement (EI) as the relation between the power consumption when the power supply of the PA is static and the power consumption in the case of an envelope amplifier excited by the signal $E_{sf}(t)$. As it is shown in Fig. 4, envelopes with less slew-rate correspond to a decrease in the amplifier efficiency.

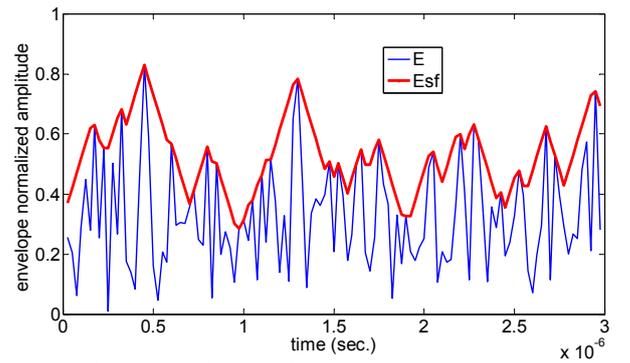


Fig. 2. Envelopes: $E(t)$ (blue) and $E_{sf}(t)$ (red).

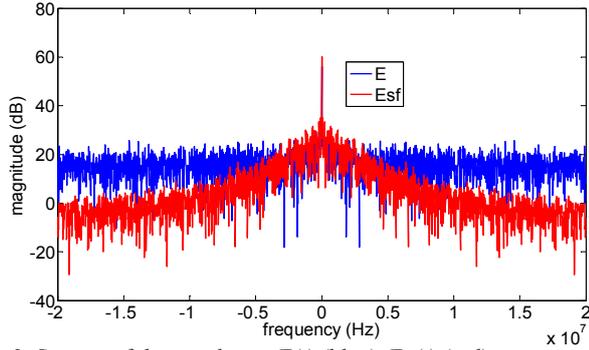


Fig. 3. Spectra of the envelopes: $E(t)$ (blue), $E_{sf}(t)$ (red).

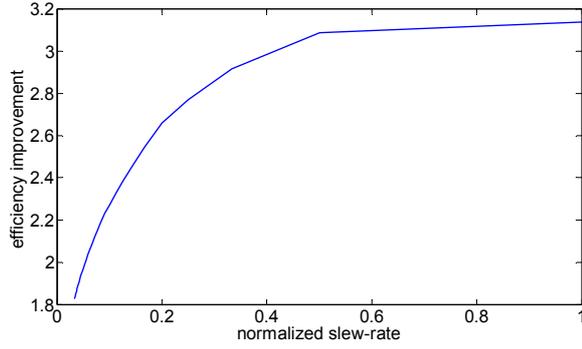


Fig. 4. RF amplifier efficiency improvement, EI, as a function of the envelope slew-rate.

Moreover, analyzing the EI evolution as a function of the slew-rate changes (see Fig. 4), an interesting conclusion can be established: a change in the normalized slew-rate values from 0.5 to 1 has little effect in the efficiency improvement. Therefore, increasing the envelope amplifier speed within this range slightly improves efficiency.

IV. FPGA IMPLEMENTATION

A. Implementation blocks

As an example, the developed slew-rate reduction algorithm has been implemented in the case of $N=10$, so this corresponds to $\Delta_M=0,1$ and this means a generated envelope with a maximum slew-rate of $A \frac{0.1}{T_s}$, being T_s the sampling

time and A the conversion factor from the numerical samples to the voltage at the DACs outputs. In our case, the DACs output signal voltage is $\pm 1V$ and the sampling clock is 40 MHz, so these correspond to a maximum slew-rate at the DACs output of $4 [V/\mu s]$.

Basically the implementation consists in the connection of two types of elemental blocks. A first type responsible for doing the delay of each envelope sample and then to add Δ_M (see Fig. 5) and another type for doing the

comparison between signals to finally select the bigger one, by means of a multiplexor, (see Fig. 6).

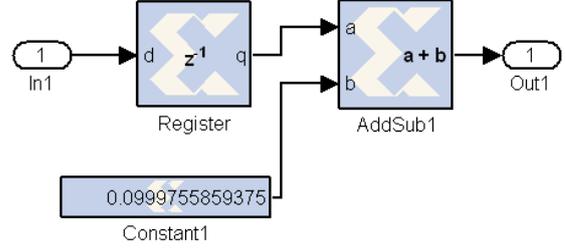


Fig. 5. FPGA block type-1: delay+addition/subtraction.

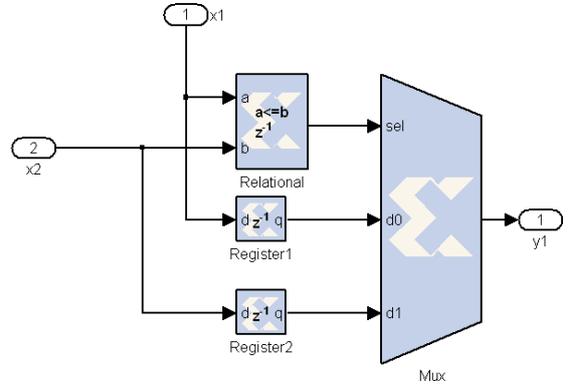


Fig. 6. FPGA block type-2: comparator+mux.

B. FPGA implementation results

Fig. 7 shows the schematic diagram of the implementation in the case on $N=10$ ($\Delta_M=0.1$). A total of 10 blocks of type-1 and 8 blocks of type-2 have been used. The algorithm has been implemented by using Xilinx System Generator software, and tested in a Nallatech board (this includes a XC4VSX35 and two 14 bits DACs running at 40 MHz).

Fig. 8 plots the real envelope $E(n)$ (yellow), the envelope bound $y(n)$ (blue) and the slow envelope $E_s(n)$ (red) in the case of an OFDM modulated signal. The DACs output signals are captured by using an oscilloscope and shown in Fig.9

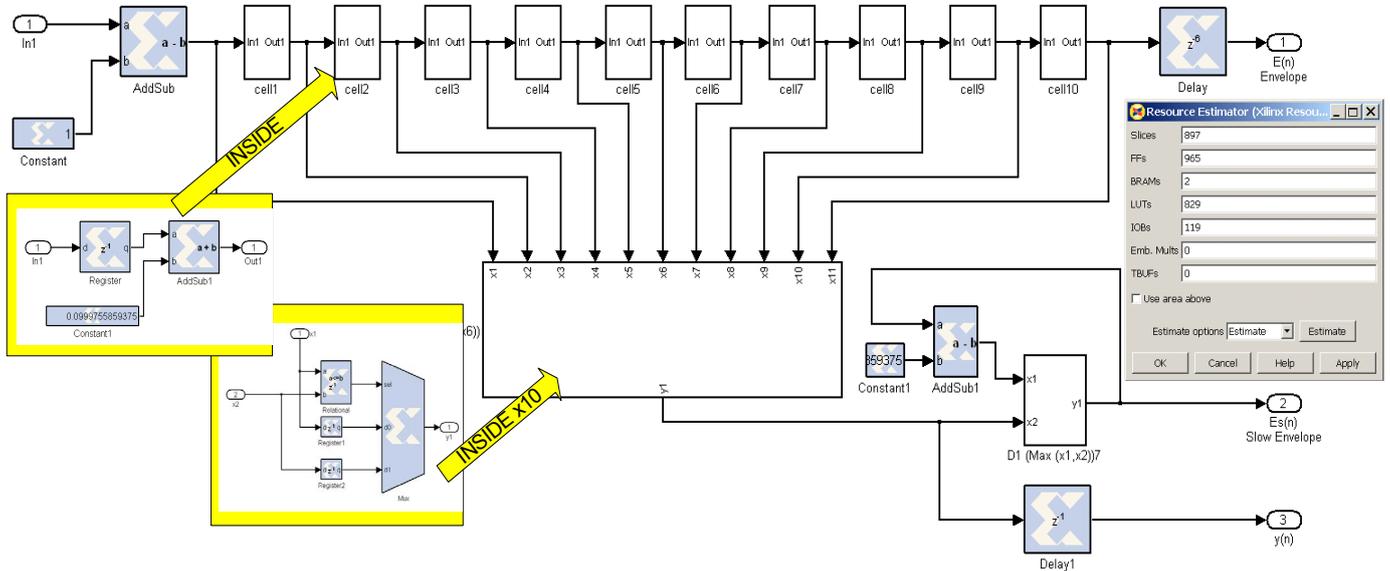


Fig. 7. FPGA implementation blocks.

VI. Conclusion

The developed algorithm has been implemented and tested in a FPGA device. The results obtained show the proposed method is suitable for calculating in real-time slew-rate limited envelopes that are an upper bound of the true envelope. This is useful in envelope tracking amplifiers in order to solve the slew-rate limitation found in drain wideband power amplifiers.

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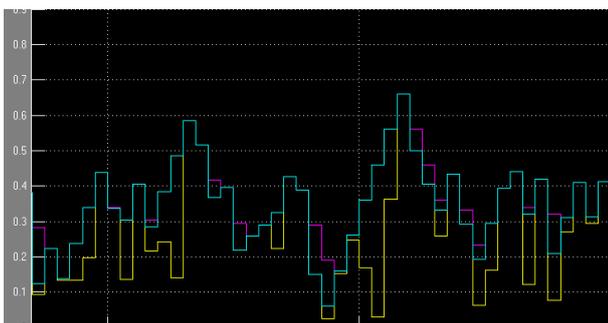


Fig. 8. FPGA generated envelopes: simulation.



Fig. 9. FPGA generated envelopes: DACs outputs ($E_s(n)$ in red, and $E(n)$ in violet).