Implementation Issues in FPGA-Controlled Polar Transmitters

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***Abstract* — This paper presents a digital platform to generate, linearize and adjust complex baseband and intermediate frequency signals for operating in both envelope tracking and polar transmitters. The closed-loop nature of this field programmable gate array (FPGA)-based set-up allows introducing control strategies to overcome or mitigate some of the unwanted distortion arising from maladjustments in the aforementioned efficient transmitters. Real-time adaptive digital predistortion is also provided to improve the overall linearity of the system. In a first approach, memoryless predistortion has been considered; however, additional look-up-tables can be easily included to compensate for memory effects.**

I. Introduction

Reducing energy consumption and enhancing power efficiency is nowadays one of the common objectives in all Electrical Engineering research areas. It is well known that the power amplifier (PA) is one of the most power hungry devices in radiocommunications. Therefore, operating with linear Class-A PAs at significant power back-off levels, to guarantee the desired linearity when amplifying non-constant envelope modulated signals, is no longer a desirable solution since it results power inefficient. In a classical Cartesian transmitter with static supply, the PA has to linearly amplify a carrier signal which is both phase and amplitude modulated and usually presenting significant peak-to-average power ratios (PAPRs). This implies that for having linear amplification it is necessary to use extremely inefficient class A or AB PAs.

Power supply control architectures with great potential for high-efficiency operation such as: polar transmitters (PTs), envelope elimination and restoration (EE&R) or envelope tracking (ET) systems; have been revived thanks to current high-speed digital signal processors which substitute their analog counterparts, subjected to tolerances and periodic adjustments. In a PT [1],[2], the envelope of the modulated signal has to be generated or detected - following the EE&R concept - for properly controlling the RF PA drain bias.

Therefore, the envelope and phase information of the modulated signal are sent separately and only combined together in the final RF PA. This could result in a very high efficient operation since the RF PA has to handle only a phase modulated - constant in amplitude – signal, and thus the use of switched-mode PAs, such as class D-1, class E, class F or F-1, is permitted. While unlike in PT, a simple adaptation of the device power capability (dynamic supply) is forced in ET systems [3]-[5]. Both are usually implemented in conjunction with digital predistortion (DPD) linearization to compensate for possible nonlinear distortion in the amplification process.

The aim of this paper is to describe the implementation of an FPGA-based subsystem, capable not only of generating the necessary baseband (BB) and intermediate frequency (IF) signals in a PT, but also of monitoring and controlling some of the critical issues compromising its ideal behavior. This signal processing platform, consisting of a Virtex-4 processor connected to two analog-to-digital converters (ADCs) and two digital-to-analog converters (DACs) of 14 bits each; has to be able of compensating, in real-time, for the most usual mismatches found in this type of architecture.

Therefore, in Section II, the whole BB and IF transmitter set-up is presented, emphasizing the procedure to generate the envelope and the phase modulated IF signal. The solution to critical time misalignments between the envelope and the phase signal paths, together with the compensation for nonlinear distortion by means of DPD, are also described in this section. In Section III a brief description of the RF PA is given and finally, in Section IV, measured results are provided as a validation of the proposed implementation.

II. Implementation Issues in a Real-Time FPGA-Controlled Polar Transmitter

A. FPGA Baseband and IF Setup

Fig. 1 shows the block diagram of the proposed versatile FPGA platform for controlling the correct functioning of both ET and PTs. It includes a variable delay to synchronize both polar components of the transmitted signal and a DPD unit to compensate for the nonlinear effects generated in the RF PA. In general, typical digital signal processing platforms are composed by only two DACs. Therefore, if one DAC is used for the envelope of the signal, the other will be used to transmit: a) the original BB signal modulated at IF, in the case of ET systems, or; b) an IF phase-modulated signal with constant envelope, in the case of PTs.

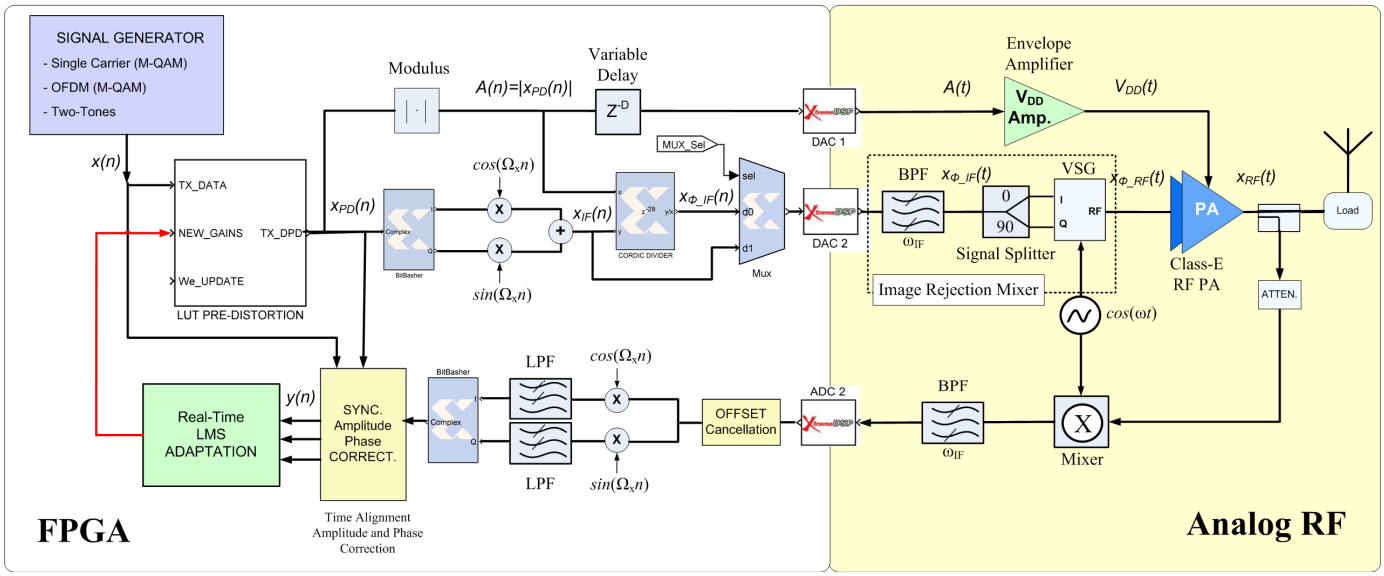

Fig. 1. Block diagram of a Polar Transmitter with real-time adaptive digital predistortion

As it can be observed in Fig. 1, the complex baseband signal to be transmitted ($x[n]$) is generated by the same FPGA responsible for the closed-loop control. Then, DPD is applied by multiplying the original signal to be transmitted by a complex gain stored in a look-up table (LUT), as it is described in (1); and whose values are updated real-time and without interrupting the transmission [6].

$$x_{PD}[n] = f_{PD}\left(x[n]\right) = x[n]\cdot G^{*}_{LUT}\left(\left|x[n]\right|\right) \qquad (1)$$

with $G^{*}_{LUT}(\cdot)$ being the complex gain and $x_{PD}[n]$ the complex predistorted signal at baseband that can be expressed as

$$x_{PD}[n] = x^{I}_{PD}[n] + jx^{Q}_{PD}[n] = A[n]e^{j\phi[n]}$$
$$A[n] = \sqrt{\left(x^{I}_{PD}[n]\right)^2 + \left(x^{Q}_{PD}[n]\right)^2};\ \phi[n] = \operatorname{arctg}\left(\frac{x^{Q}_{PD}[n]}{x^{I}_{PD}[n]}\right) \qquad (2)$$

The envelope of the signal, A[n], is sent to DAC-1, while the predistorted baseband signal is then modulated digitally at the IF frequency ($x_{IF}[n]$), as shown in Fig. 1.

$$x_{IF}[n] = x^{I}_{PD}[n]\cos\left(\Omega_{IF}n\right) - x^{Q}_{PD}[n]\sin\left(\Omega_{IF}n\right)$$
$$= \mathrm{Re}\left\{A[n]e^{j\phi[n]}e^{j\Omega_{IF}n}\right\} = A[n]\cos\left(\Omega_{IF}n + \phi[n]\right) \qquad (3)$$

By controlling a multiplexer is then possible to select the signal to be sent to DAC-2. This flexible FPGA configuration permits selecting the IF modulated signal ($x_{IF}[n]$) in the case of performing ET or; in the case of PT, it is possible to send the phase-modulated signal with constant envelope ($x_{\phi\_IF}[n]$), described in (4),

$$x_{\phi\_IF}[n] = K\frac{x_{IF}[n]}{A[n]} = K\cos\left(\Omega_{IF}n + \phi[n]\right) \qquad (4)$$

where $\Omega_{IF} = \omega_{IF}/f_s$, and with K and f_s being a constant value and the sampling frequency, respectively. The normalization in (4) is performed in the FPGA by means of a Coordinate Rotation Digital Computer (CORDIC) algorithm.

B. *Delay Compensation*

One of the critical issues that degrades the correct performance of PTs, are time delay mismatches between the envelope and the phase modulated signal. The effect of this envelope and phase modulated signal misalignment can be appreciated in both time (see Fig. 2) and frequency domain, where it appears as significant spectral regrowth of the modulated signal (or IMD products in case of a two-tone test).

Considering τ the necessary delay applied to the envelope to align it with the phase modulated signal, the resulting RF signal after efficient amplification is defined as,

$$x_{RF}(t) = f\left(V_{DD}(t-\tau), x_{\phi\_RF}(t)\right)$$
$$= B(t)\cos\left(\omega_{RF}t + \phi(t)\right) \qquad (5)$$

Where $V_{DD}(t)$ is the envelope after amplification (Fig. 1) and B(t) is the resulting modulated amplitude of the RF signal. The delay is calculated and set at baseband. The resolution of the variable delay used to synchronize both signals is a natural number multiple of the sampling period (T_s).

$$\tau = D\cdot T_s\ [\text{seg.}];\ D\in\mathbb{N} \qquad (6)$$

In order to automatically determine the optimum delay, it is possible to carry out a two-tone test with a frequency separation of Δf and then, after sweeping (using a digital counter) for all N possible delays, with $N = T_s\cdot\Delta f/2$, just keep the delay that minimizes both the IMD_3 and the NMSE.

$$\tau_{opt} = D_{opt}T_s \rightarrow \min\left\{\text{IMD3}\,\&\,\text{NMSE}\right\};\tau = [0,\ldots N-1] \qquad (7)$$

Fig. 2 shows the envelope ($V_{DD}(t)$), the phase modulated signal ($x_{\phi\_RF}(t)$) and the resulting output combination ($x_{RF}(t)$), of a two-tone test signal with $\Delta f = 0.3125\,\text{MHz}$, with and without time alignment.

C. Digital Predistortion Linearization

The modulating stage in a PT, consisting of a switched-mode PA, presents nonlinear V_{DD}-$|x_{RF}|$ characteristics [9] as the ones depicted in Fig. 3. A real-time DPD, based in a Cartesian complex product, has been implemented in the FPGA to compensate both AM-AM and AM-PM characteristics. The whole polar transmitter is treated as a black box, without specifying if the nonlinear behavior comes from the envelope amplifier or from the RF PA. As the phase modulated IF signal is always normalized in level, the control over the output amplitude component is made through the drain biasing component. Apart from nonlinear and memory effects, which arise when combining both polar components of the signal at RF, the relation of this combination can be seen as a product:

$$x_{RF}(t) = f\left(V_{DD}(t), x_{\phi\_RF}(t)\right) \propto V_{DD}(t) \cdot x_{\phi\_RF}(t) \quad (8)$$

Despite the DPD limitations to compensate for nonlinear distortion when it is already in saturation, the closed-loop nature of the DPD allows performing gain control.

III. RF Setup: Efficient Class-E PA

For the RF final stage, a GaN (Gallium Nitride) HEMT-based class-E PA at 900 MHz was designed. This switch-mode operating class, invented by Nathan and Alan Sokal in 1975 [7], has become one of the most popular configurations with proved high efficiency results [7],[8]. In the search for maximum efficiency, the selected transistor technology is a key factor. Here, the GaN HEMT technology was selected, considering not only the capability of these devices to manage high power densities but also other outstanding characteristics (high f_t, low input capacitance, manageable output capacitance and low on resistance, R_{ds}) that make them nearly ideal when implementing switched-mode PAs.

The chosen transistor is a 15 W CGH35015 device from Cree. In the designed transmission line topology [8], open-circuit conditions at second and third harmonics were forced, while the load at the fundamental frequency was adjusted around the theoretical value in (9) with the aid of load-pull simulations. The power added efficiency (PAE) was maximized, trying to force a nearly constant profile from medium to high V_{DD} values, in order to avoid reductions in the average efficiency figures when handling high PAPR envelope signals.

$$Z_{net} \approx \frac{0.28015}{\omega \cdot C_{ds}} e^{j49.0524^\circ} \quad (9)$$

A PAE above 70% was measured at V_{GS} = -2.8V and for a drain biasing voltage range from 20 to 35 V. The characterized V_{DD}-$|x_{RF}|$ profiles are shown in Fig. 3.

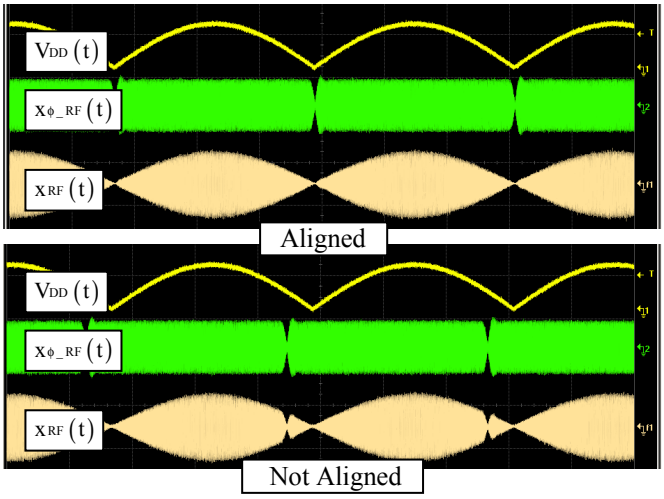

Fig. 2. Measured time-domain waveforms of a two-tone test.

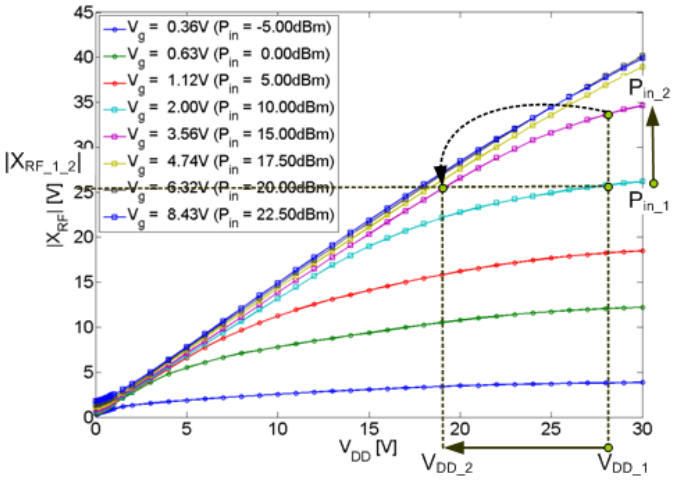

Fig. 3. V_{DD}-$|x_{RF}|$ characteristics for a 15 W GaN HEMT PA.

IV. Experimental Test of the FPGA-Controlled PT

Due to current limitations with the available envelope amplifier, only signals with bandwidths below 1.5 MHz at baseband may be handled. Fig. 4 shows the linearization performance of the DPD considering two-tone with $\Delta f = 0.3125\,\text{MHz}$. At this frequency spacing, no memory effects are introduced by the envelope amplifier. In such conditions, with only half dB of back off, it was possible to improve the IMD_3 around 12 dB and IMD_5 around 9 dB.

Fig. 5 and Fig. 6 show both linearized and unlinearized 16-QAM output spectra with 1.5 MHz bandwidth. Fixing the desired level of output power, we have considered two different RF input power levels, similar to P_{in_1} and P_{in_2} in Fig. 3. As it can be observed in Fig. 6, the linearization performance obtained with P_{in_2} is quite remarkable, since it was obtained by increasing 4 dB the RF input power (P_{in_2}= P_{in_1}+ 4 dB), and thus changing the gain characteristic (see Fig. 3). For a given output power, the measured ACP improvement in the case of P_{in_1} after DPD was: 3.7 dB in the lower channel and 0.5 dB in the upper channel.

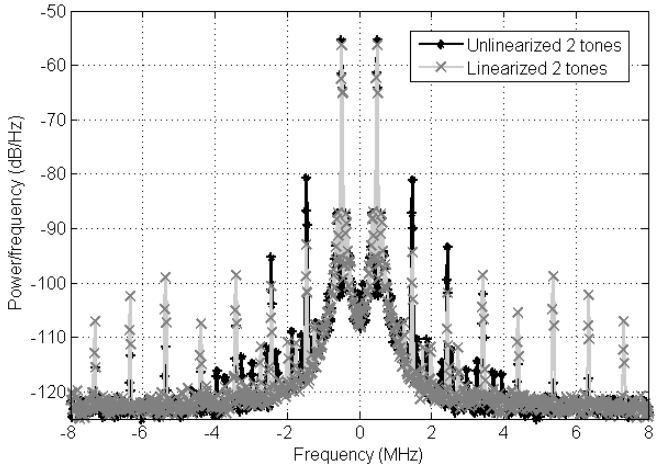

Fig. 4. Two-tone test output.

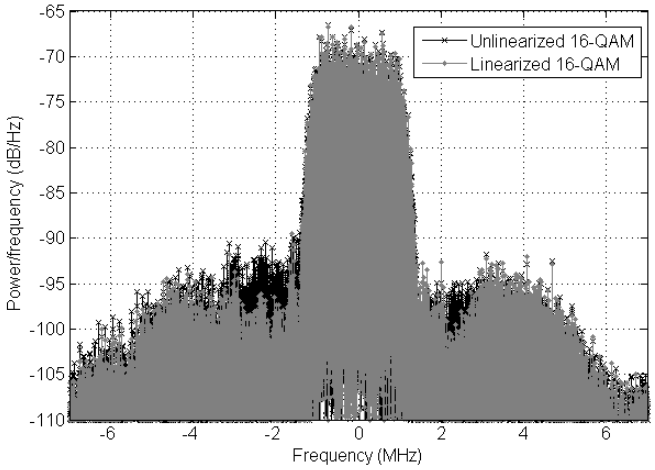

Fig. 5. 16-QAM output power spectra in the case of P_{in_1}.

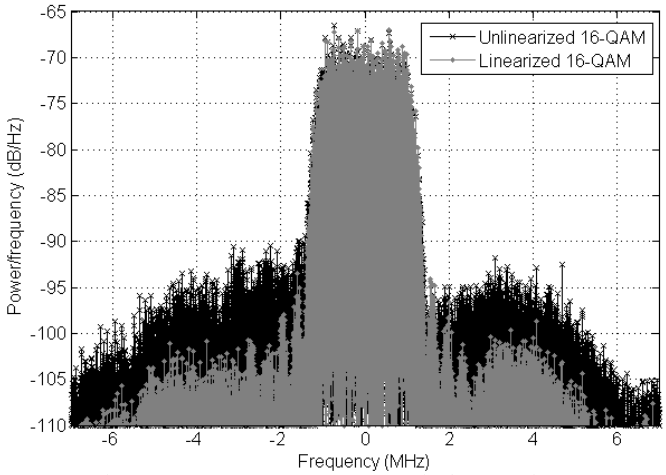

Fig. 6. 16-QAM output power spectra in the case of P_{in_2}.

However, in the case of P_{in_2} and according to (8), the maximum voltage in the envelope (i.e. V_{DD_1} or V_{DD_2} in Fig. 3) was decreased, going from 28 V to 16.4 V; while the resulting ACP improvement was: 8.4 dB in the lower channel and 5.8 dB in the upper channel. Therefore, fixing the output power, the desired ACP levels were met at the expenses of some degradation in the PAE. Moreover, the output power of the system can be determined and controlled at baseband by just fixing the predistortion gain.

IV. Conclusion

An FPGA-based versatile platform for real-time generation, synchronization and linearization of modulated signals to be transmitted in both ET systems and PTs, has been presented and tested. Since only memoryless predistortion was considered, the nonlinear distortion and memory effects introduced by the envelope amplifier were hardly compensated. However, the real-time, close-loop, DPD can be also used for gain control, since by fixing the AM-AM point where the RF output is to be taken, it trades-off the envelope V_{DD} and the RF P_{in} to obtain the desired output. The real-time adaptation mechanism also guarantees robustness against eventual mismatches.

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