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**Regular paper**

**Phase Opposition Disposition PWM  
Strategy and Hardware in the Loop  
Validation for a 3-SM Modular  
Multilevel Converter**



*This paper focuses on the carrier disposition Pulse Width Modulation (PWM) strategies for Modular Multilevel Converters (MMC). The authors propose a new Phase Opposition Disposition PWM (PODPWM) scheme applicable regardless of the converter's sub-modules number. Moreover, a capacitor voltage sorting algorithm is synthesized aiming to ensure the converter's balanced operation. Simulation results of a 3.6 MVA, 3-SM-MMC are presented and discussed. In addition, a Hardware In the Loop (HIL) validation of the proposed PODPWM has been made using Field Programmable Gate Array (FPGA) target. The actual power system (the 3-SM-MMC and the 3-phase RL load) is then replaced by its real-time emulator. The latter is interfaced to the PODPWM control under test and both are implemented and run altogether in the same Xilinx XC7Z020 Zynq FPGA device. The obtained real-time HIL emulation results are presented and compared to the offline simulation results.*

**Keywords:** Modular multilevel converter, Pulse Width Modulation, circulating current, active balance, Real-time Emulator, Hardware In the Loop

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## **1. Introduction**

The Modular Multilevel Converter (MMC) was proposed by R. Marquardt in 2001 [1]. MMC topology has proved to be an attractive alternative in high voltage applications such as HVDC transmissions [2]. It is made by a serial connection of identical DC-choppers called Sub-Modules (SM), with flying capacitors that stand for independent DC sources. The output voltage is obtained by a control of the state of sub-modules switches with taking into account the capacitors voltage balance and the circulating current, which are the main issues of this topology [3].

Many research studies have been dedicated to the modulation of the MMC converter. The modularity and simple implementation of PWM-based modulation strategies make them the most suitable for MMC converters [4]. In this paper three Carrier Disposition CDPWM strategies are considered: Phase Disposition PWM (PDPWM), Alternative Phase Opposition Disposition PWM (APODPWM) and Phase Opposition Disposition PWM (PODPWM). Previous researches [5] demonstrated that when used for MMC modulation, PDPWM yields to better voltage and current THD performances considering the higher number of the generated voltage levels. PODPWM and APODPWM performances can be enhanced using an output filter. Furthermore, lower circulating current and inductor voltage are obtained with PODPWM and APODPWM techniques considering the achieved balance

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between the DC bus and the converter's leg voltage. However, in [6], it is shown that PODPWM technique is applicable only when the number of sub-modules per arm is even. In this paper, the authors propose an original implementation of the PODPWM for MMC converters that remains valid regardless of the converter's sub-modules number. The proposed modulation scheme is used to control a 3-phase MMC converter with 3 sub-modules in each arm. Such converter will be referred to as a 3-SM MMC converter. Simulation results of a 3.6 MVA, 3-SM-MMC are presented and discussed.

To make a first realistic validation and provide first experimental operating guarantees of the proposed PODPWM strategy before the implementation of the whole experimental platform, a Hardware-In-the-Loop (HIL) validation is made [7]. To this aim, an FPGA-based real-time emulator of the actual power system composed of the 3-SM MMC and the 3-phase RL load is developed by implementing their dynamic models in Field Programmable Gate Array (FPGA) target. The HIL validation is carried out by interfacing the PODPWM controller under test to the developed real-time emulator. The interfacing here is fully digital since the controller and the real-time emulator are both implemented and run altogether in the same FPGA device.

The general operation principles and the modulation strategies for MMC converters are introduced in Section 2, outlining the limits of the existing PODPWM modulation strategy. In Section 3, a new PODPWM implementation scheme is proposed. The proposed modulation strategy is simulated on a 3,6MVA 3-SM MMC converter, firstly with perfect DC sources then while using a capacitor as a voltage source for each sub-module. Finally, the HIL validation of the proposed PODPWM implementation is presented.

## 2. Operation principle and modulation strategies for MMC converters

### 2.1. Operation principle of MMC converter

The topology of a three-phase MMC is depicted in fig.1. One leg converter consists of a connection of two arms. Each arm is a series connection of  $N$  identical sub-modules (SM) and an inductor  $L$ . Each SM contains a half bridge converter and one capacitor  $C$  as shown in fig.1-b. For a given SM in the upper arm (respectively lower arm), the output voltage  $U_{SM\_Ui}(t)$  (respectively  $U_{SM\_Li}(t)$ ) is given by

$$\begin{cases} U_{SM\_Ui}(t) = SC_{Ui} U_{c\_Ui}(t) \\ U_{SM\_Li}(t) = SC_{Li} U_{c\_Li}(t) \end{cases} \quad (1)$$

where  $SC_{Ui}$  (respectively  $SC_{Li}$ ) is the modulation function of the  $i^{\text{th}}$  SM in the upper arm (respectively the  $i^{\text{th}}$  SM in the lower arm) and  $U_{c\_Ui}(t)$  (respectively  $U_{c\_Li}(t)$ ) is the corresponding flying capacitor voltage.  $SC_{Ui}$  and  $SC_{Li}$  are equal to 1 when the SM's upper switch is ON and the SM's lower switch is OFF, and are equal to 0 when the SM's upper switch is OFF and the lower switch is ON.

Under full balance conditions, we can write

$$U_{C\_Ui}(t) = U_{C\_Li}(t) = U_C(t) = \frac{V_{dc}}{N} \quad (2)$$

where  $N$  is the number of sub-modules per arm.

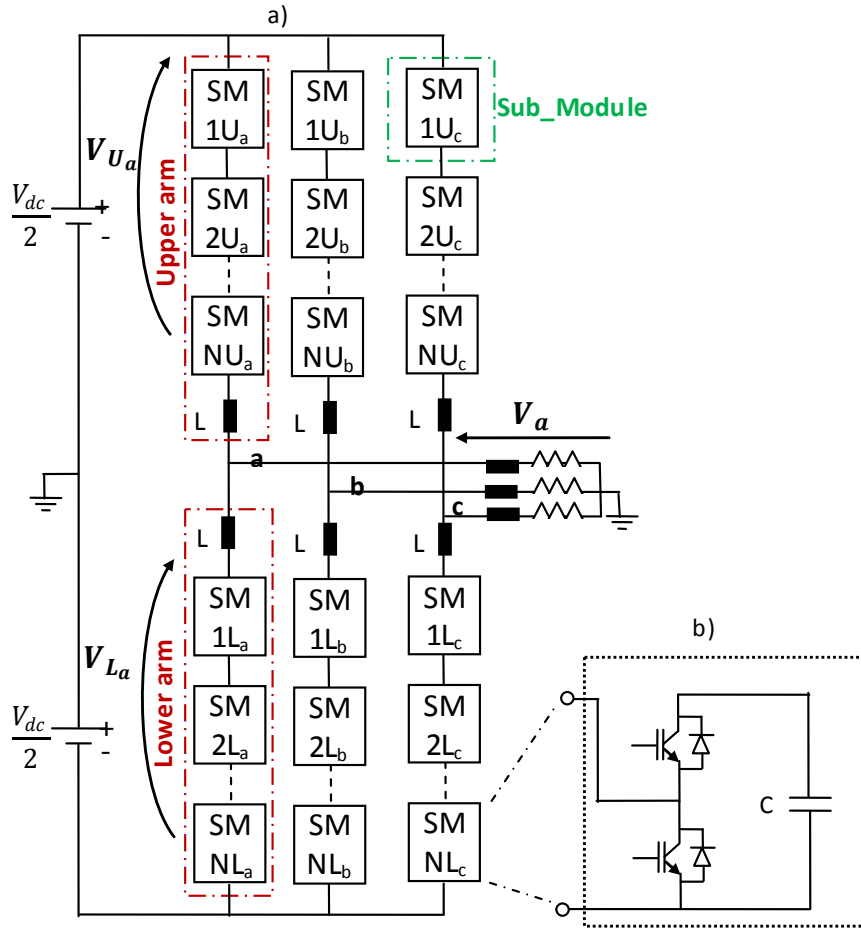


Fig. 1. Modular Multilevel Converter a) N-SM MMC b) Topology of a single sub-module SM

Consequently,

$$\begin{cases} U_{Ux}(t) = \sum_{i=1}^N U_{SM\_Ui_x}(t) = \sum_{i=1}^N SC_{Ui_x} \cdot \frac{V_{dc}}{N} = \frac{n_{U_x}}{N} V_{dc} \\ U_{Lx}(t) = \sum_{i=1}^N U_{SM\_Li_x}(t) = \sum_{i=1}^N SC_{Li_x} \cdot \frac{V_{dc}}{N} = \frac{n_{L_x}}{N} V_{dc} \end{cases} \quad (3)$$

where  $x$  denotes phase  $a$ ,  $b$  or  $c$ ,  $U_{Ux}(t)$  and  $U_{Lx}(t)$  denote respectively phase  $x$  upper and lower arm voltages and  $n_{U_x}$  and  $n_{L_x}$  are the number of the ON-stated SM of phase  $x$  upper and lower arm respectively.

Kirchhoff's voltage law for phase  $a$  can be expressed as

$$V_a - \frac{V_{dc}}{2} + U_{U_a} + L \frac{di_{U_a}}{dt} = 0 \quad (4)$$

$$V_a + \frac{V_{dc}}{2} - U_{L_a} - L \frac{di_{L_a}}{dt} = 0 \quad (5)$$

The subtraction of (5) from (4) gives:

$$\frac{V_{dc} - U_{L_a} - U_{U_a}}{2} = L \frac{d}{dt} \left( \frac{i_{U_a} + i_{L_a}}{2} \right) = L \frac{di_{za}}{dt} \quad (6)$$

where  $i_{za}$  is defined as phase  $a$  circulating current.

Under balance condition operation, the converter output current is equally split among the two corresponding arms.

Therefore, phase  $a$  output current can be written as

$$i_a = \frac{i_{U_a} - i_{L_a}}{2} \quad (7)$$

and  $i_{za}$ , which results from the voltage difference between the DC bus and the sum of the upper and lower arms voltages, is given by

$$\begin{cases} i_{za} = 0 \\ V_{dc} = U_{L_a} + L \frac{di_{L_a}}{dt} + U_{U_a} + L \frac{di_{U_a}}{dt} = U_{L_a} + U_{U_a} + 2L \frac{di_{za}}{dt} = U_{U_a} + U_{L_a} \end{cases} \quad (8)$$

Moreover, from (3) and (8), one can write:

$$n_{U_a} + n_{L_a} = N \quad (9)$$

Thus, for a balanced MMC converter operation, the modulation strategy and algorithm control has to ensure that  $N$  SMs among the  $2N$  available ones are switched ON.

## 2.2. PWM strategies for MMC converters

PWM based modulation strategies are widely used in multilevel converters modulation [8]. The association of each triangular carrier to a particular SM goes along with the nature of modularity and scalability for MMC converters [4]. However, the influence of the carriers' disposition on the MMC converter is still not deeply investigated. Basically, their arrangement directly influences the number of the output voltage levels [9]. This criterion was used to classify modulation strategies into two main categories:  $N+1$  and  $2N+1$  modulations. The first category lead to  $N+1$  voltage levels and the second one lead to  $2N+1$  voltage levels.

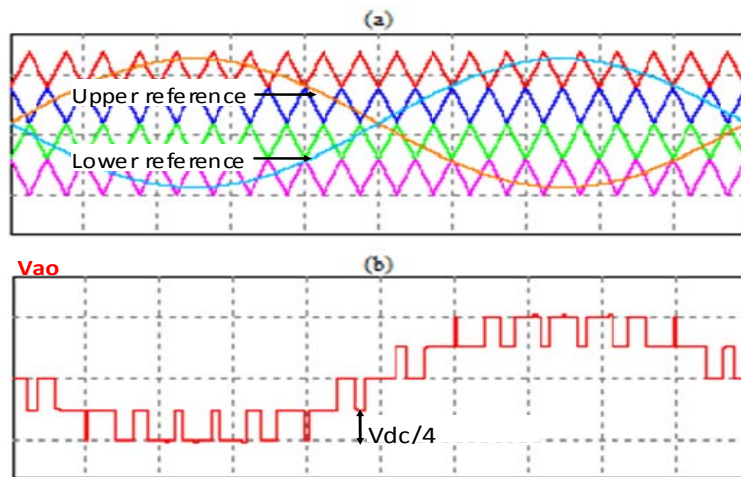
In the following, analysis of one example of each of these two PWM categories is carried out based on a comparison of their output performances.

### *(N+1) modulation*

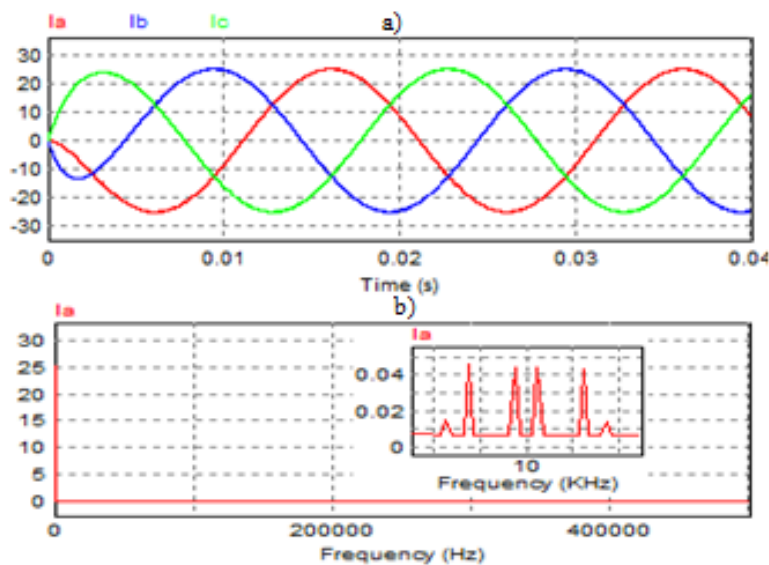
An  $(N+1)$  modulated MMC converter is able to generate  $(N+1)$  voltage levels. Fig.2 shows the Alternative Phase Opposition Disposition PWM (APODPWM). Neighbored carriers are  $180^\circ$  phase shifted. For a 4-SM MMC converter, simple output voltage presents 5 levels, as shown in fig.2 b).

The symmetry of the carriers and reference voltages disposition in  $(N+1)$  modulation strategies guarantees that  $N$  SMs are ON switched [9]. Consequently, according to equations (4) and (5),  $(N+1)$  modulation strategies lead to a low inductor voltage and a negligible MMC circulating current.

Fig.3 gives the three line currents for a 4-SM MMC converter with:  $V_{dc}=600$  V,  $L=100$   $\mu$ H,  $f_{sw}=10$  kHz,  $R_{load}=10$   $\Omega$  and  $L_{load}=11,5$  mH. Line current amplitude is equal to 25 A. Line  $a$  current spectrum presented on fig.5 shows that first harmonics appear around 10 kHz with maximum amplitude equal to 0.045A, which is lower than 0.18% of the fundamental magnitude. The THDi is equal to 0.36%

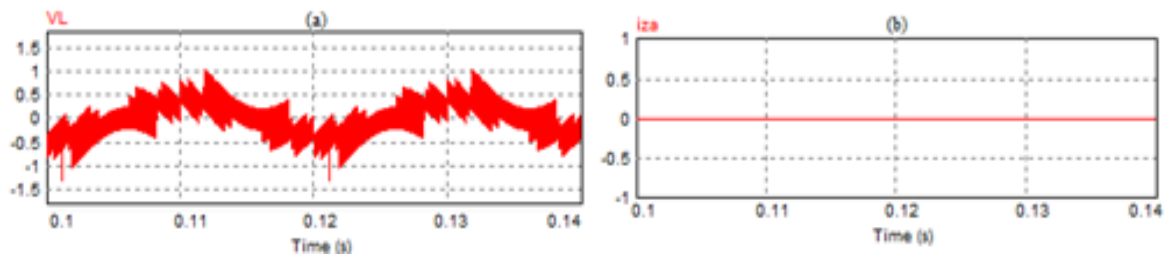


**Fig. 2.** (N+1) modulation strategy: APODPWM;N=4 a) carriers disposition b) Simple output voltage: 5 voltage levels



**Fig. 3.** 4-SM MMC APODPWM modulated converter: line currents (10A/div) a) Time analysis b) Line a spectral analysis

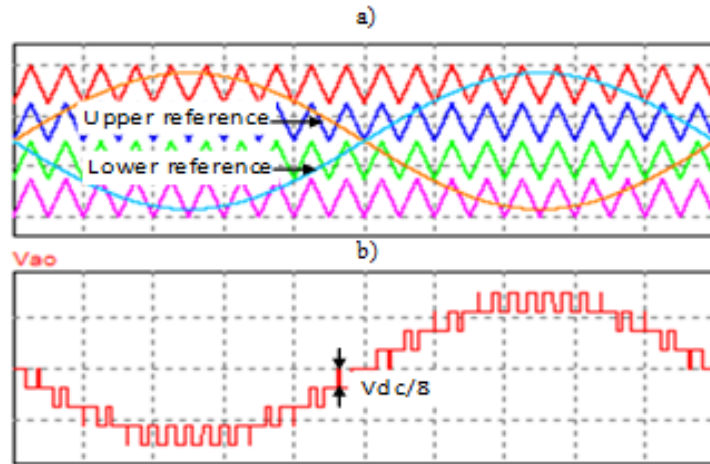
Fig.4 gives leg a steady state inductor voltage and circulating current. The inductor voltage, which is the difference between the phase-leg voltage and the DC side voltage, has a high frequency component that is related to the capacitors' charge and discharge [10]. Due to the small difference between the DC side voltage and the phase-leg voltage for APODPWM, the magnitude of the resulting circulating current is nearly equal to zero.



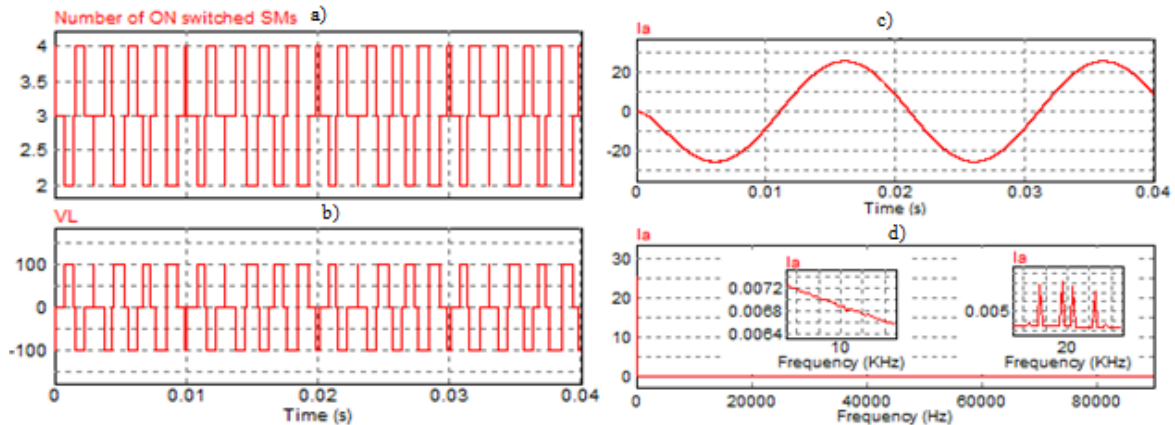
**Fig. 4.** APODPWM modulation strategy for a 4-SM MMC converter  $V_{dc}=600$  V;  $L=100$   $\mu$ H,  $f_{sw}=10$  kHz a) inductor voltage (2.10-2V/div) b) Leg a circulating current  $i_{za}$

*(2N+1) modulation*

MMC converter controlled with  $(2N+1)$  modulation strategies is able to generate  $2N+1$  voltage levels. Fig.5 shows the Phase Disposition (PDPWM) strategy used for a 4-SM MMC converter. The converter's output voltage has 9 voltage levels. Due to the asymmetry of the carriers disposition, the number of ON switched SMs varies between  $N$ ,  $N-1$  and  $N+1$ , as shown in fig.6-a and the inductor's voltage is equal to  $0$ ,  $+V_{dc}/2N$  or  $-V_{dc}/2N$  as shown in fig.6-b. First harmonics appear at 20kHz with maximum amplitude equal to 8mA.

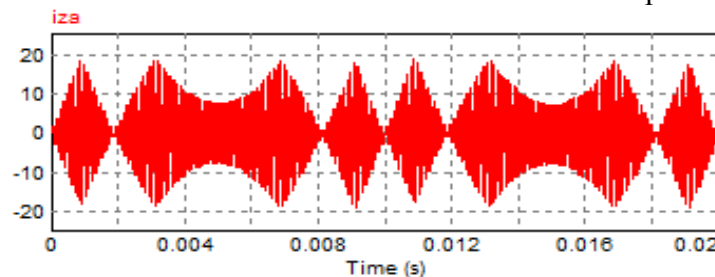


**Fig. 5.**  $2N+1$  modulation strategy: PDPWM a) carriers disposition b) leg  $a$  output voltage: 9 levels



**Fig. 6.** PDPWM modulation strategy for a 3-SM MMC a) Number of inserted SMs b) leg  $a$  upper arm inductor voltage c) Line  $a$  current temporal analysis b) Line  $a$  current spectral analysis

As the number of ON switched SMs is not always equal to  $N$ , the circulating current increases dramatically and reaches 20A (fig.7). However, the increase of the output voltage levels improves THDv with a 5% rate and THDi with 77% rate compared to APODPWM.

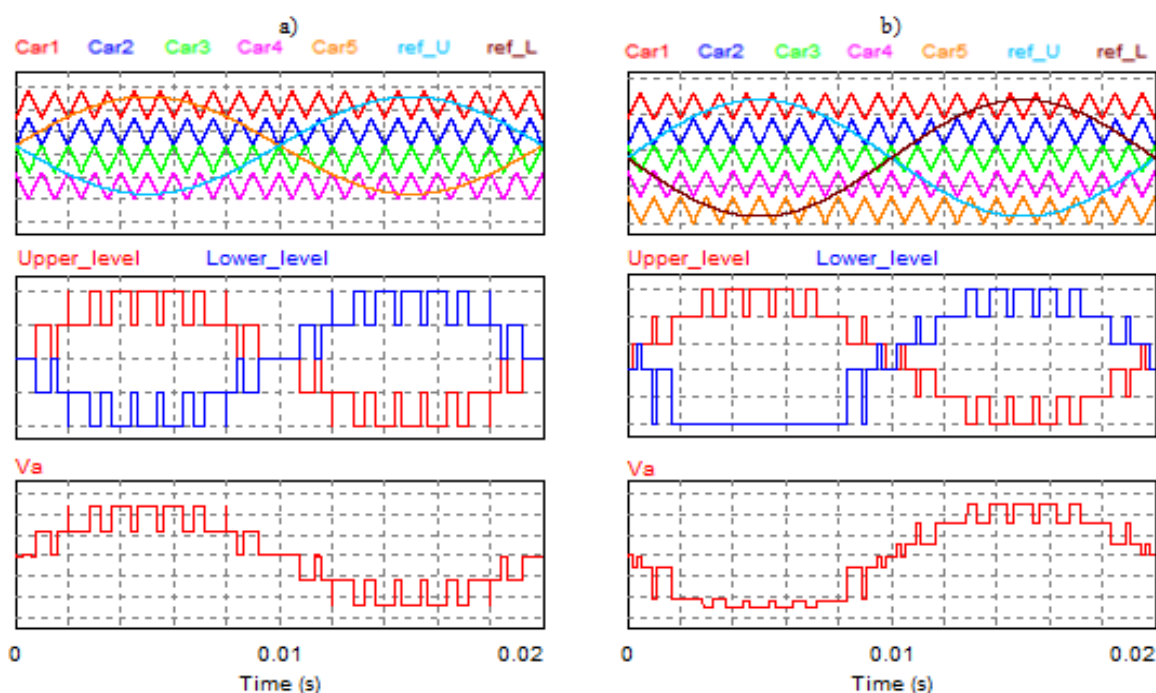


**Fig. 7.** Leg  $a$  circulating current under PDPWM modulation strategy

### 2.3. Limits of existing PODPWM strategy for MMC converters

The disposition of the references and carriers is the key element towards the possibility to apply the PODPWM according to the number of sub-modules.

For example, PODPWM proposed in [8] is based on the comparison of  $N$  carriers with the upper arm reference to generate the upper arm control signals, and the comparison of the same carriers with the lower arm reference to generate lower arm control signals. This strategy is only effective when sub-modules number is even. However, the strategy is limited when the sub-modules number is odd. In fact, with this disposition, it is impossible to define the carriers' phases so that they are symmetric according to the average value of the reference signal. The asymmetry causes an imbalance in the upper and lower levels. Fig. 8 shows upper PODPWM output voltages when applied for a 4-SM and 5-SM MMC converter.



**Fig. 8.** PODPWM modulation strategy for a)4-SM MMC converter b)5-SM MMC converter

### 3. Proposed PODPWM strategy implementation for MMC converter

Basically, the PODPWM (Phase Opposition Disposition PWM) strategy is a  $(N+1)$  modulation type since in this case, an  $N$ -SM MMC converter generates an output voltage with  $N+1$  levels. However, in [10], the authors confirm that this PWM strategy is limited since it is only applicable for MMC converters when the number of sub-modules in each arm is even.

In this paper, we propose a PODPWM modulation strategy for MMC converter independently of its sub-modules numbers. Simulations tests are carried out with a 3-SM MMC converter. The capacitance of each SM is equal to 6 mF. The DC bus is equal to 3600V. Two 100 $\mu$ H inductors are used in the arm inductors to ensure an equal distribution of the line current among the two arms. The carrier frequency is equal to 10 kHz, thus switching period equal to 100 $\mu$ s. The MMC converter is connected to an RL load where R is equal to 10 $\Omega$  and L is equal to 11.5mH.



### 3.1. Converter control principal

In this paragraph, flying capacitors are replaced by perfect DC sources, each equal to  $V_{dc}/3$ . The issue of flying capacitors balance is investigated in the next paragraph.

The idea is to consider each branch of the MMC converter as an independent cascaded multilevel converter. Hence, the MMC topology is equivalent to a series connection of 2 independent cascaded multilevel converters. The same approach is applied to the modulation block. Rather than using the same carriers for upper and lower sub-modules, the proposed PODPWM assigns a carrier for each SM and a reference for each arm. The control signal of each SM results from the comparison of its carrier and its corresponding reference. PODPWM, presented on fig. 9, is designed as follows:

- All three carriers for the upper arm are identical: initial phase angle is 0 and the magnitude is equal to  $\frac{V_{dc}}{N}$ . These three carriers are vertically shifted with  $\frac{V_{dc}}{N}$ , forming 3 contiguous bands varying from 0 to  $V_{dc}$ . They are compared with a sinusoidal reference  $V_{ref\_U}$  defined as follows:

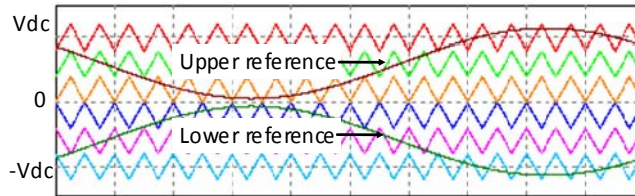
$$V_{ref\_U}(t) = \frac{V_{dc}}{2} + m \frac{V_{dc}}{2} \cos(2\pi ft) \quad (10)$$

where  $V_{dc}$  is the DC bus,  $m$  is the modulation depth and  $f$  is the reference frequency

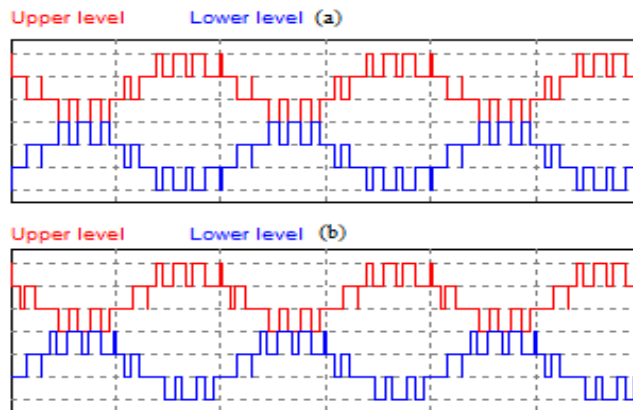
- All three carriers for the lower arm defined with  $180^\circ$  initial phase and  $-\frac{V_{dc}}{N}$  magnitude, forming 3 contiguous bands varying from  $-V_{dc}$  to 0. The so generated carriers are compared with a sinusoidal reference  $V_{ref\_L}$  defined by:

$$V_{ref\_L}(t) = -\frac{V_{dc}}{2} + m \frac{V_{dc}}{2} \cos(2\pi ft) \quad (11)$$

One can note that both references and carriers are symmetrical according to the 0 voltage level. Hence, the proposed PODPWM is equivalent to two PDPWM modulation blocks which are symmetrical according to the 0 voltage level (fig.10).



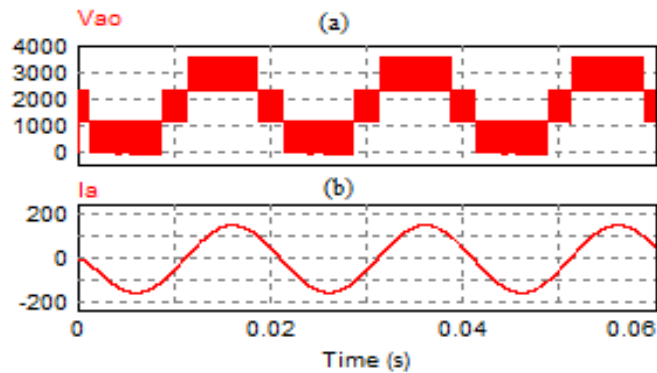
**Fig. 9** Proposed PODPWM for a 3-SM MMC converter



**Fig. 10** Upper and lower arms voltage levels a) PODPWM b)PDPWM

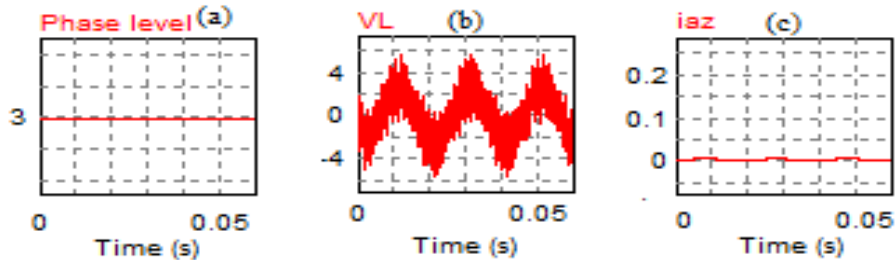


Leg a output voltage presented in fig. 11 shows the expected 4 voltage levels. The output current is sinusoidal with THDi equal to 0.36%.



**Fig. 11** 3-SM MMC converter a) Simple output voltage b) Line current

Fig.12-a) shows that for a 3-SM MMC converter, the number of switched ON SMs is continually equal to 3. Therefore, the DC bus-leg balance condition defined in (9) is verified, leading to a sensitive reduction of the inductor voltage as shown in fig.12-b.

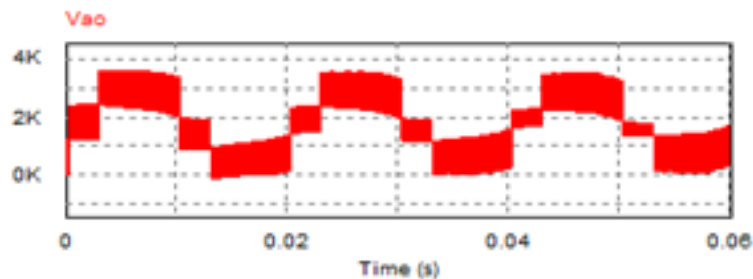


**Fig.12.** 3-SM MMC converter leg characteristics a)Number of ON switched SMs b) Inductor voltage c) circulating current

### 3.2. Flying capacitors voltage balance issue

When perfect DC sources are replaced with flying capacitors, output leg voltages are unbalanced, as shown on fig.13.

However, for an MMC converter, the same voltage level can be obtained with different configurations of the sub-modules control signals. This degree of freedom can be exploited to perform the flying capacitors voltage balance.



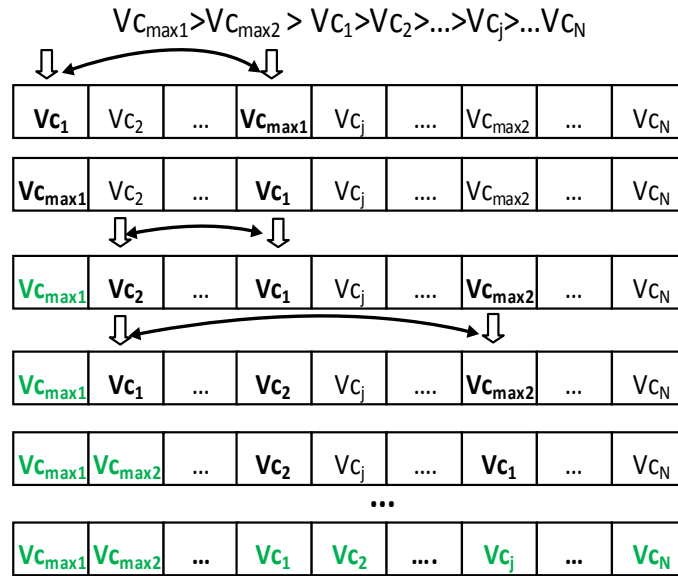
**Fig. 13** Leg a output voltage of MMC without balancing algorithm

In fact, PODPWM carriers are not assigned to specific SMs. They are used to determine the required voltage level for upper and lower arms. It is to mention that the arms of each leg are controlled separately, but the number of ON switched SM in both arms together is equal to N. For a 3-SM MMC converter, each arm can generate 4 voltage levels: 0, 1, 2 and

3. If voltage level is equal to 0 (respectively 3), all control signals have to be equal to 0 (respectively 1). However, many combinations are available to achieve voltage level 1 and 2. This extra degree of freedom is used to perform flying capacitors voltage balance. If voltage level is equal to 1, the switched ON SM is the one with the most charged or discharged flying capacitor, depending on the current sign. Likewise, if voltage level is equal to 2, the SMs with the most charged or discharged flying capacitors are switched ON. This strategy is extendable to N number of sub-modules. A sorting algorithm is implemented in order to determine the priority degree for each flying capacitor. For an N-SM MMC converter, the sorting algorithm is as follows:

- Measured flying capacitors voltages of each branch are stored in an array with N cells.
- We suppose that array's first cell contains the greatest value. We browse the cells from 2 to N with comparing the value of each cell with value n°1. If value n°1 is less than value n° X, cells 1 and X switch values.
- The same algorithm is applied for the next (N-1) cells.

The sorting algorithm output is an array of N cells, containing the N capacitors voltages sorted from greatest to lowest. The sorting algorithm is depicted on fig.14 and fig. 15 shows the overall block diagram of the proposed method, applied to one single arm.



**Fig. 14** Sorting algorithm for an N-SM MMC

The converter's output voltages are shown on fig. 16. Line to line output voltage shows the expected voltage levels. However, when a zoom is applied on the different levels, an error equal to 100V appears. This error corresponds to the flying capacitors voltages. Fig. 17 shows the flying capacitors voltages of the upper and lower arms of leg *a*. The error varies between 100V and 51V which respectively represents 4.16% and 2.1% of the initial voltage.

Line to line output voltage shows the expected voltage levels. However, when a zoom is applied on the different levels, an error equal to 100V appears. This error corresponds to the flying capacitors voltages. Fig. 17 shows the flying capacitors voltages of the upper and lower arms of leg *a*. The error varies between 40V and 22V which respectively represents 3.33% and 1.8% of the initial voltage.

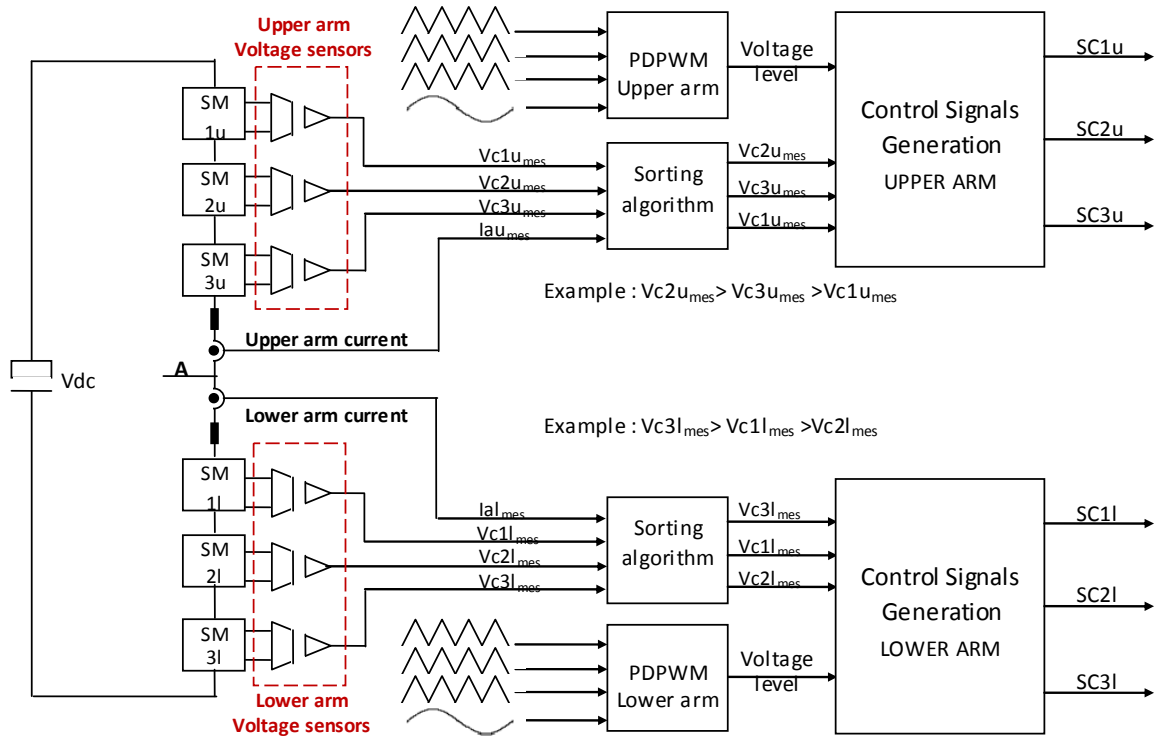


Fig. 15. Block diagram of the proposed algorithm applied for one leg

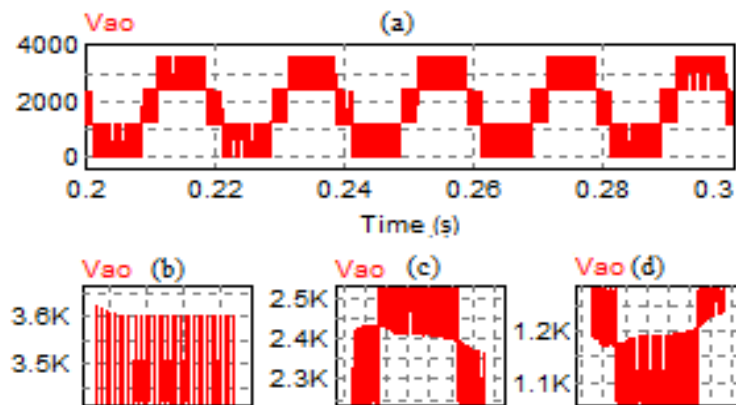


Fig. 16. Three-SM MMC converter output voltage a) output voltage b) zoom on the 3600V level c) zoom on the 2400V level d) zoom on the 1200V level

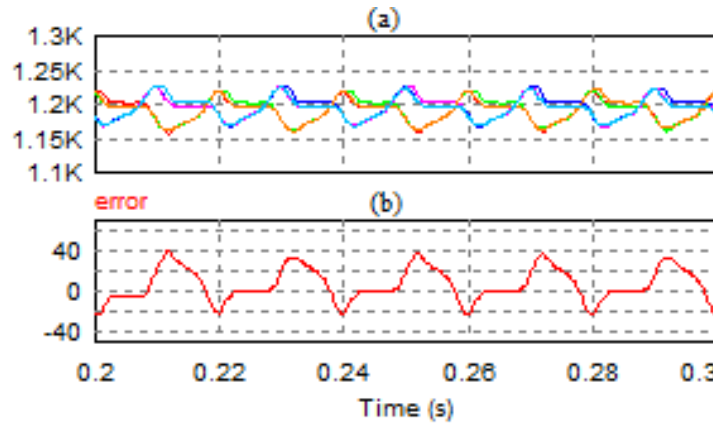
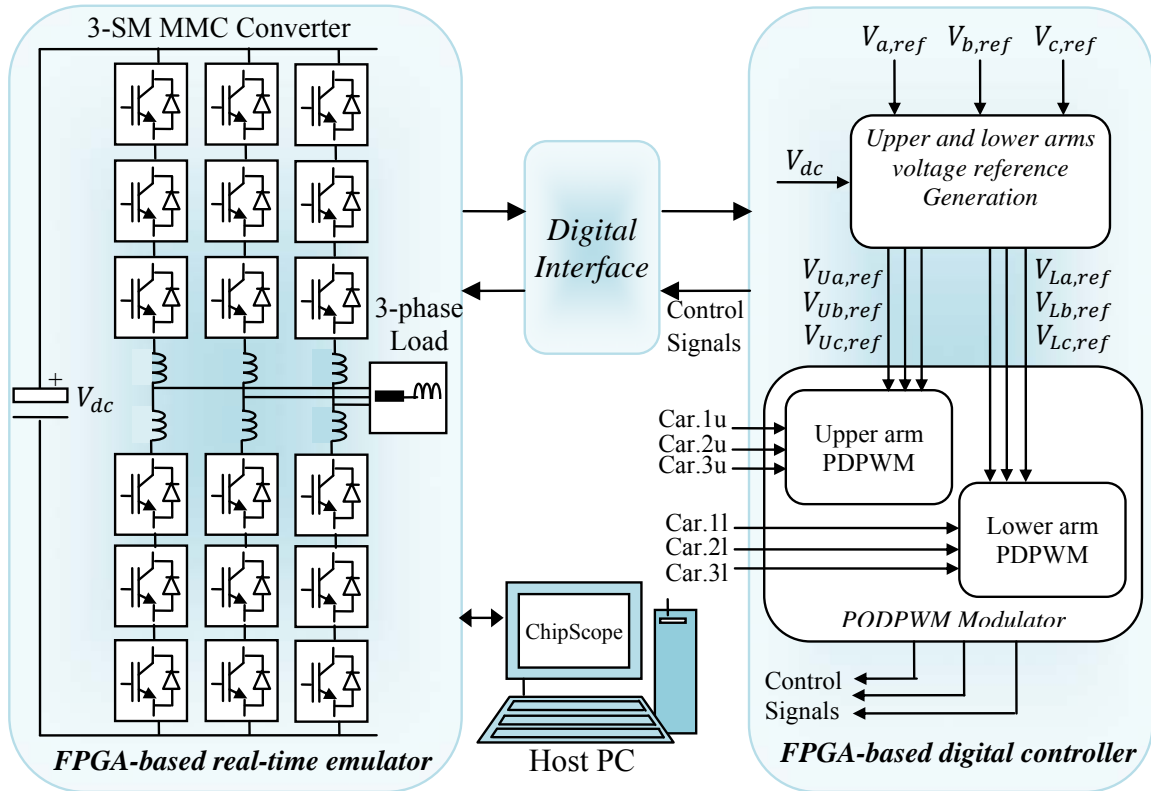


Fig. 17. Voltage balance outputs a) Leg a flying capacitors voltages b) error on the capacitor voltage of the first sub module of leg a upper arm.

#### 4. Hardware In the Loop (HIL) validation of the proposed PODPWM

The objective here is to efficiently test the proposed PODPWM strategy and verify its functionalities in real-time prior to installation and commissioning. The developed system is presented in Fig. 18. It consists of two main parts: the emulated power system under control and the PODPWM controller under test. The emulator and its controller have been implemented on the Xilinx XC7Z020 Zynq FPGA device. The data transfer between them is ensured by a digital interface. To debug and to view the internal signals running in FPGA, the ChipScope analyzer has been used [11].



**Fig.18.** Structure of the developed system

##### 4.1. Emulated power system

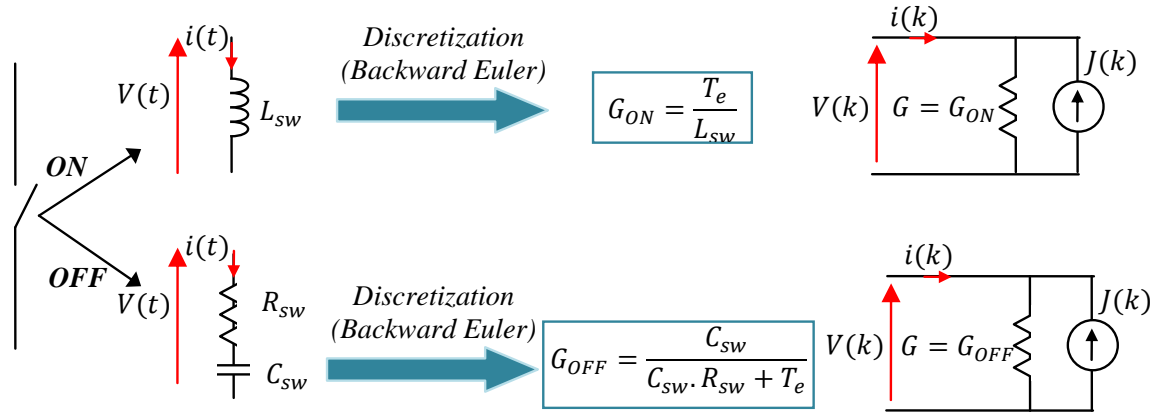
The emulated power system is composed of the DC bus voltage, the 3-SM MMC converter with perfect DC sources in each sub-module and the 3-phase RL load.

The 3-SM MMC modeling has been achieved based on the two-valued ADC equivalent switch model. This approach is privileged since it allows representing each switch individually which allows a more accurate modeling of switching dynamics (See Fig. 19).

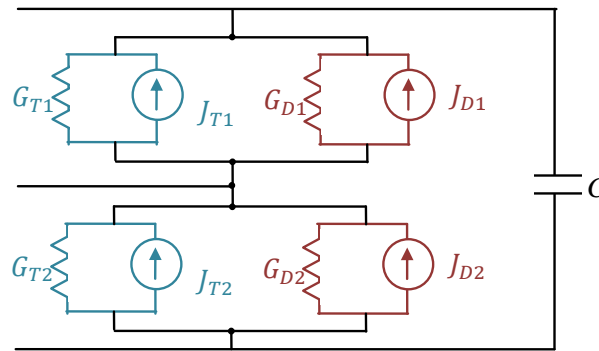
Basically, an ADC equivalent model consists in representing a power switch by a small inductance ( $L_{sw}$ ) when the switch state is ON and by a small capacitance ( $C_{sw}$ ) when it is OFF, [12]. To solve the problem of overshoots and oscillations during commutations (due to LC circuit), a resistance ( $R_{sw}$ ) is placed in series with the capacitance which acts as a damping element, [13]. After the discretization of the L-circuit and the RC circuit, a common equivalent circuit for each switch is extracted. This circuit is composed of a dependent current source in parallel with a conductance. The value of this current source

depends on the switch state. However, the value of the switch conductance is chosen so as to be the same in both ON/OFF states. The main reason is to extract a constant conductance matrix (that gathers all the conductances of the converter). Fig. 20 shows the obtained ADC-based equivalent model of a sub-module. It is made by the association of the ADC-based model of each switch.

To extract the overall electrical equations representing the 3-SM MMC converter, its equivalent ADC circuit is firstly determined by replacing each sub-module by its equivalent ADC model. Then, the relations between voltages and currents of the whole 3 SM MMC are extracted from this circuit by applying the Modified Nodal Analysis (MNA) method [12].



**Fig. 19** ADC equivalent circuit of a power switch



**Fig. 20** ADC equivalent circuit of a sub-module

#### 4.2. HIL emulation results

In the following, authors present the obtained HIL emulation results. Fig.21 presents the disposition of the references and carriers of the proposed PODPWM strategy. Fig. 22 shows the real-time waveforms of the line voltages  $V_{ao}$ ,  $V_{bo}$  and  $V_{co}$ . Fig.23 gives the real-time waveforms of the line currents  $I_a$ ,  $I_b$  and  $I_c$ . These responses are obtained for  $V_{dc}=600$  V,  $L=100 \mu\text{H}$ ,  $f_{sw}=10$  kHz,  $R_{load}=10 \Omega$  and  $L_{load}=11,5$  mH. As it can be seen from these figures, the HIL emulation results are similar to those of offline simulation results. The proposed PODPWM strategy is then validated in real-time. The obtained results demonstrate also that the developed real-time emulator can be used efficiently for testing advanced MMC control strategies and the evaluation of their performance in HIL context.

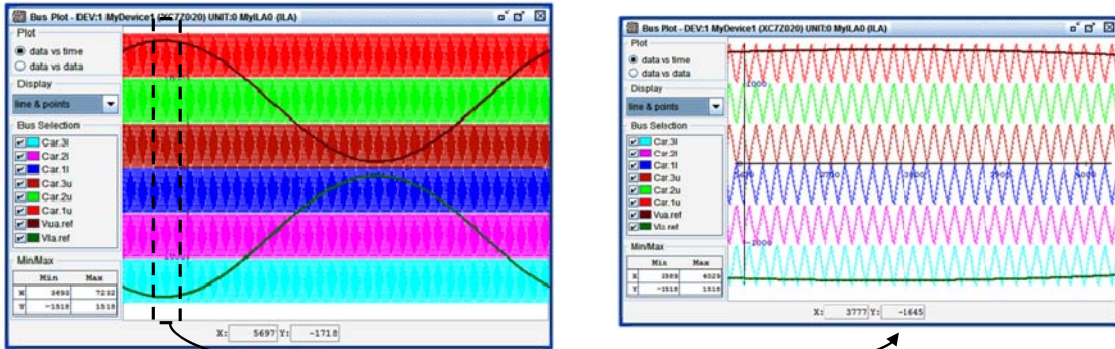


Fig. 21. Real-time waveforms of the references and carriers of the proposed PODPWM

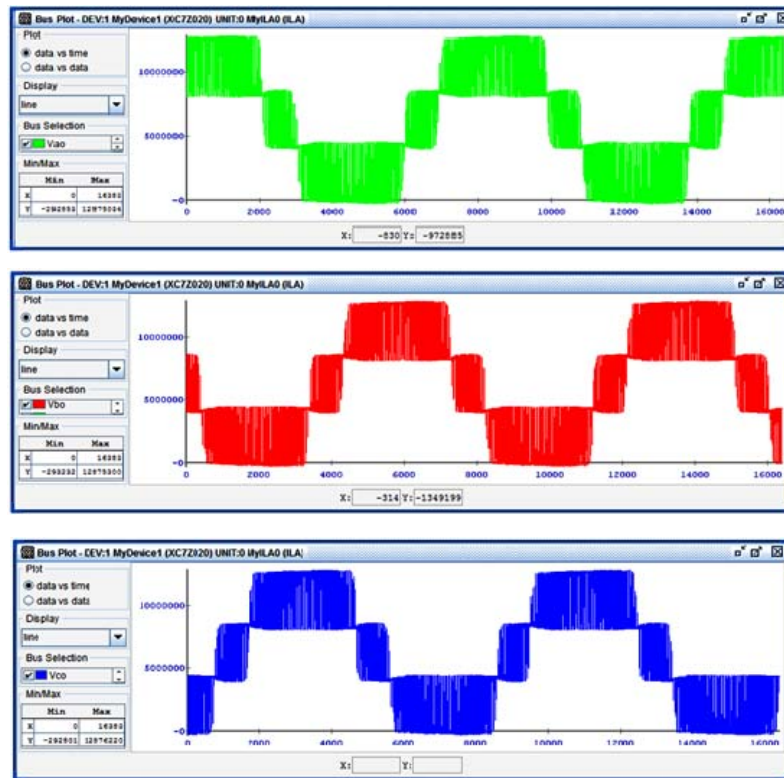


Fig. 22. Real-time waveforms of the line voltages

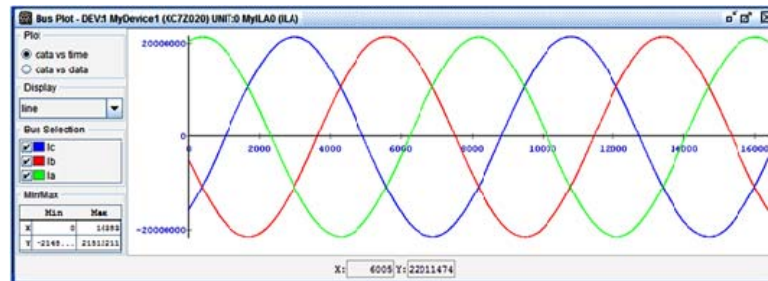


Fig. 23. Real-time waveform of the line currents

## 5. Conclusion

This paper presented a comparison between PDPWM and APODPWM strategies applied for a three-phase 3-SM MMC converter. The comparison showed that the current and voltage THDs are lower for the PDPWM since the voltage levels is almost the double



then with the APODPWM. However, the circulating current and the inductor voltage obtained with the APODPWM is less than the ones obtained with the PDPWM. In fact, the carriers' disposition in the first modulation strategy allows exactly  $N$  sub modules to be switched ON, among the  $2N$  available ones. Thus, the DC bus and the leg voltage are balanced which tremendously reduced the circulating current. Then, we proposed for the considered MMC converter a Phase Opposition Disposition PWM strategy. The flying capacitors voltages are balanced by implementing a sorting algorithm, extendable for  $N$  sub-modules per arm. Simulation results of a 3.6 MVA, 3 sub-modules MMC converter based system are presented to validate the effectiveness of the proposed control. The PODPWM is then validated using the Hardware In the Loop platform. The open loop emulation results are presented and compared to the simulation ones.

## References

- [1] R. Marquardt, "Current rectification circuit for voltage source inverters with separate energy stores replaces phase blocks with energy storing capacitors," DE10103031A1.
- [2] J. Liang, A. Nami, F. Dijkhuizen, P. Tenca, and J. Sastry, "Current source modular multilevel converter for HVDC and FACTS," in 2013 15th European Conference on Power Electronics and Applications (EPE), 2013, pp. 1–10.
- [3] Q. Tu, Z. Xu, and L. Xu, "Reduced Switching-Frequency Modulation and Circulating Current Suppression for Modular Multilevel Converters," *IEEE Trans. Power Deliv.*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.
- [4] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, "Analysis of the Phase-Shifted Carrier Modulation for Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 297–310, Jan. 2015.
- [5] S. Fan, K. Zhang, J. Xiong, and Y. Xue, "An Improved Control System for Modular Multilevel Converters with New Modulation Strategy and Voltage Balancing Control," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 358–371, Jan. 2015.
- [6] X. Liu, A. Lindemann, and H. Amiri, "Theoretical and experimental comparison of different control strategies for modular multilevel converters," in 2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL), 2014, pp. 1–9.
- [7] A. Hasanzadeh, C.S. Edrington, N. Stroupe, T. Bevis, "Real-Time Emulation of a High-Speed Microturbine Permanent-Magnet Synchronous Generator Using Multiplatform Hardware-in-the- Loop Realization," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 6, pp.3109-3118, June 2014.
- [8] T. J. Hammons, D. Woodford, J. Loughtan, M. Chamia, J. Donahoe, D. Povh, B. Bisewski, and W. Long, "Role of HVDC transmission in future energy development," *IEEE Power Eng. Rev.*, vol. 20, no. 2, pp. 10–25, Feb. 2000.
- [9] X. Liu, A. Lindemann, and H. Amiri, "Theoretical and experimental comparison of different control strategies for modular multilevel converters," in 2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL), 2014, pp. 1–9.
- [10] X. Yang, J. Li, X. Wang, W. Fan, and T. Q. Zheng, "Circulating Current Model of Modular Multilevel Converter," in *Power and Energy Engineering Conference (APPEEC), 2011 Asia-Pacific*, 2011, pp. 1–6.
- [11] Xilinx online documentation available online at <http://www.xilinx.com>
- [12] P. Pejovic and D. Maksimovic, "A Method for Fast Time-Domain Simulation of Networks with Switches," *IEEE Transactions on Power Electronics*, vol. 9, no. 4, pp. 449–456, 1994.
- [13] M. Dagbagi, A. Hemdani, L. Idkhajine, M. W. Naouar, E. Monmasson, and I. Slama-Belkhodja: "ADC-based Embedded Real-Time Simulator of a Power Converter Implemented in a Low Cost FPGA: Application to a Fault-Tolerant Control of a Grid-Connected Voltage Source Rectifier". *IEEE Transaction on Industrial Electronics*, vol. 63, No. 2, pp. 1179-1190, January 2016.