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VLSI Hybrid DC-DC Regulator

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***Abstract*— Hybrid DC-DC regulators are structures that combine both a linear voltage regulator and a switching DC-DC converter. The main objective of this hybrid topology is to converge, in a single circuit topology, the best of both alternatives: a small voltage output ripple, which is a common characteristic of linear regulator circuits, and good energy efficiency, as in switching alternatives. While the linear regulator fixes the required output voltage to a fixed value with negligible steady-state ripple without the necessity of an output capacitor, the switching converter is devoted to drive most of the load current. In addition, the linear one supplies the required current when the load changes at transient intervals. Current paper deals with the design of an on-chip hybrid converter for low output currents. The design has been designed and tested with simulations using a standard 180 nm CMOS technology. The simulation results presented in the paper shows suitable performance of the design.**

Keywords*— *Voltage linear regulator; DC-DC converter; hybrid regulator; CMOS technology; VLSI design; first-generation current conveyor (CCI).

I. INTRODUCTION

Linear voltage regulators have been structures widely used for decades [1]. Their advantages are clear: On one hand, thanks to their line regulation, output ripple voltage can be minimized; on the other, thanks to their load regulation, their transient response can be good enough to supply load with high slew rate currents. However, as a main problem, they suffer from low power efficiency, especially due to the voltage drop at the series-pass transistor, which has to be also large to drive high output currents.

In order to avoid this problem, the alternative used for a long time is also clear: Switching DC-DC power converters [2]. They have, as main advantage, their high efficiency that, although not being 100% due to the omnipresent circuit losses, it is near this optimal value. However, as it is well known, compared with the first ones, they present some important problems as their complexity, they are prone to produce electromagnetic interferences to neighboring circuits, and they require bulky capacitors to reduce output voltage ripple.

In order to converge in a single structure the advantages of both aforementioned alternatives, minimizing the problems associated to them, hybrid DC-DC regulators can be a good option. They embed, in a compact circuit topology, a linear voltage regulator and a switching converter in order to implement the DC/DC voltage regulator. This third alternative preserves the well-known advantages of the two previous ones; that is to say, they achieve both fast wideband ripple-free regulation (by virtue of the linear regulator), with moderately high power efficiency (by virtue of the switching regulator). In addition, as the control subsystem is based on a hysteretic control (implemented using an analog comparator), it is simple but with good high-frequency response.

These hybrid structures are of strong interest when power supplies are required to drive large output currents and, at the same time, they present fast response to load variations as in modern microprocessors systems [3] or in envelope power-supply modulators for wideband adaptive supply of RF power amplifiers (RFPA) [4].

The paper presents a CMOS design of a DC-DC regulator based on a linear-assisted topology devoted for an on-chip application. This particular design must guarantee the electric power supply for a critical load that needs a constant supply value of 1.1 V, and a load current from 0 to 15 mA. In particular, it consists of a continuous time filter for MEMS signal filtering with its central-frequency and quality-factor control loops. The range of the regulator input voltage is from 1.6 V to 1.8 V.

The paper is organized as follows: section II presents the circuit architecture, section III shows some simulation results and finally concluding remarks are discussed in Section IV.

II. ARCHITECTURE

The circuit consists of a linear regulator that supplies a constant output voltage V_{out} to the load R_L. The aim is to reduce the dissipated power in the series-pass transistor by, as far as possible, reduce the current through this regulator. Thus a buck switching power converter is connected in parallel. This converter will provide most of the current to the load (i.e. improving efficiency) while the linear regulator will be the responsible of keeping good line and load regulations. This idea was first presented and analyzed in [5] but it required a clock signal for the switching converter.

The proposed configuration in this paper was first presented in [6] and it is improved in many aspects here. The proposed circuit in this work is shown in Fig. 1.

In a first approximation, consider a comparator (*CMP)* without hysteresis. If the load current is below a limit current or I_γ, the output of *CMP* is held low. Thus, the switching converter will be disabled and the current through inductor L

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will be zero. As a result of this, the linear regulator, which is implemented by means of and operational amplifier (OA), supplies all the required current (I_{lin}) by the load R_L (I_{load}). However, when the load current increases slightly beyond this limit current I_γ, the comparator output will switch to high, switching on transistor M_P and increasing the current through the inductor (I_{ind}) linearly. Then, I_{lin} will decrease also linearly until it is below the reference current I_γ. At this moment, the comparator switches its output from high to low, switching off M_P and, as a consequence, decreasing I_{ind}. Then, as I_{ind} decreases and the linear regulator current becomes higher than the reference current ($I_{lin}>I_\gamma$), *CMP* switches from low to high, repeating the cycle again. Notice that, in order to limit the switching frequency to avoid increasing the switching losses significantly, it is convenient to add a hysteresis to the analog comparator *CMP*.

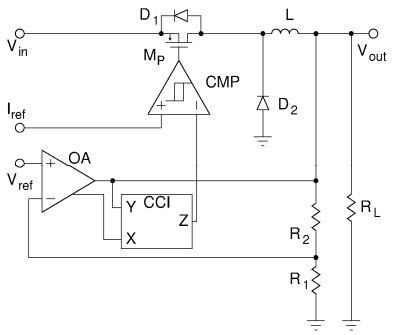

Fig. 1. Schematics of the complete hybrid DC-DC converter. The lower output of the operational amplifier is its secondary output, which has the same conductance divided by 200 than its primary output.

Note that the exact switching points (that is, the hysteresis) of the comparator are only important to fix an exact switching frequency but they do not strongly affect line or voltage regulations. Thus, high precision circuits are not required for this task.

As an additional advantage, it is important to highlight that typical low-pass filtering capacitors at the output terminal of switching converters (which can be large in some applications), are not necessary in this structure as the linear regulator implements an efficient low-pass filtering function [7].

The circuit has been designed using UMC 180 nm Mixed-Signal/RF CMOS technology with a 1.8 *V* power supply voltage, double well and normal and low threshold voltage MOS transistors. All devices are integrated on-chip except the off-chip inductor of the switching converter.

A. Complete VLSI System

Fig. 1 shows the complete schematics of the hybrid DC-DC regulator which consists of an operational amplifier (OA) as the linear regulator, and, on the other hand, a power PMOSFET switch (M_P) with its corresponding protection diode (D_1), an off-chip inductor (L) and a diode (D_2) as the switching converter. In addition, a first-generation current conveyor (*CCI*) as a current sensor, a hysteric current comparator (*CMP*) as the control circuit of the switching converter, and a resistive voltage divider (R_1 and R_2) as the output voltage sensor complete the schematic.

Operation of the design is as follows. The resistive voltage divider, composed of resistors R_1 and R_2, divides the output voltage and feds it back to the operational amplifier. Then, the amplifier fixes the output of the converter to a stable voltage that depends on the reference voltage V_{ref}, as long as amplifier gain and bandwidth is enough to compensate load and line variations. In order to sense the linear regulator output current, it is sensed using SENSEFET technique [8]. The output current of the amplifier is also copied and divided by 200 by connecting a secondary output of the amplifier to *X* port of the CCI. This secondary output is an AB output stage identical to the principal output and it is connected to the same input node but its transistors 200 are times narrower. Thus, as the CCI copies the voltage from its *Y* terminal to its *X* terminal and as output conductance of the secondary output of the amplifier is 200 times smaller than the impedance at its principal output, current driven by *X* terminal is 200 times smaller than the current driven by the output of the linear regulator. This current can be used to sense the amount of current supplied by the linear regulator. Note that a simpler CCI can be used instead of a more complex CCII because it is not necessary an exact copy of the linear regulator current, and a 0.5% current driven to port *Y* is not a problem for the correct behavior of the system.

Current driven at *X* port is copied by the CCI at its *Z* port, which in turn is fed to the hysteresis current comparator negative input. Then, this magnitude is compared with a reference current so that the PMOSFET power switch (M_P) is controlled to work for large output currents ($i_{reg}(t)>I_\gamma$), and it is opened for small output currents ($i_{reg}(t)<I_\gamma$).

B. Voltage Linear Regulator

The implementation of the CMOS linear regulator is shown in Fig. 2. It consists of a Miller OTA voltage amplifier (M_1~M_7) with a level shifter (M_8~M_{11}), and a primary (M_{12}~M_{13}) and a secondary (M_{14}~M_{15}) class AB output stages. The latter transistors are 200 times narrower than transistors at the principal output stage. Thus, when V'_{out} is set to the same voltage as V_{out}, the output current supplied by the secondary output stage is 200 times smaller than the output current supplied by the primary output stage. It should be noted that, in order to increase the available voltage range of the amplifier, transistors M_{12}~M_{15} are low threshold voltage transistors. As the output voltage is closer to V_{in} than to ground, the NMOS transistor (M_{13}) that connects the output to V_{in} is the most critical one and its gate-to-source voltage (V_{GS13}) must be minimized while PMOS transistor M_{14} gate-to-source voltage (V_{GS14}) may be higher without compromising the performance of the converter.

C. Current Detector

To detect the current driven by the linear regulator a SENSEFET structure has been used. To get a proportional current to the linear regulator output current, the voltage at the primary output of the operational amplifier is copied to its secondary output. This process is performed by a first generation current conveyor (CCI) [9]. The most important

drawback of this kind of current conveyor is the finite impedance of input *Y* that sinks the same current as sunk at input *X*, thus, distorting the exact measure of the output current of the operational amplifier. To overcome this problem, a second generation current conveyor (CCII) would be required. However, as current driven by *X* is 200 times smaller than the current driven by the linear regulator, a simpler CCI (although less precise) is more appropriate than a CCII to reduce circuit complexity and power consumption.

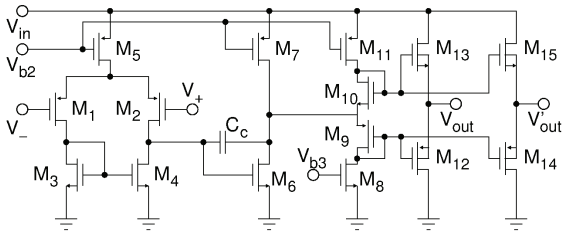

Fig. 2. Schematics of the voltage linear regulator. Bulk connections are not shown except when they are not connected to ground or to the power source (V_{in}). V_{out} is de primary output and V'_{out} is the secondary output with transistors 200 times narrower. Note that V_{in} is the power supply connected to most PMOS sources and bodies.

D. Hysteresis Current Comparator

To compare the current supplied by the linear regulator with a reference current and control the power switch, the hysteresis current comparator in Fig. 3 is used [10]. The comparator consists of a decision circuit (transistors M_{16}~M_{19}), an output buffer consisting of a differential gain stage (M_{20}~M_{24}), and an inverter (transistors M_{25} and M_{26}) to shape the output to logical values and drive the power switch.

The decision circuit operation is as follows. Transistors M_{16}~M_{19} dimensions are such that $\beta_{16}=\beta_{19}=\beta_A$, and $\beta_{17}=\beta_{18}=\beta_B$. Also, let's assume that current i_p is much larger than current i_n. Under this circumstance, M_{16} and M_{18} are on. Then, as M_{18} decreases v_{SD18}, it sets v_{on} closer to V_{in} and cuts off M_{17} and M_{19}. As a consequence, M_{16} drives all i_p and:

$$v_{op} = V_{in} - v_{THP} - \sqrt{\frac{2i_p}{\beta_A}} \quad . \tag{1}$$

Then, as current i_p decreases and/or current i_n increases, switching starts to take place when the source-gate voltage of M_{19} is equal to v_{THP}. As v_{SG19} is increased beyond v_{THP}, by further increasing i_n/decreasing i_p, M_{17} starts to take current away from M_{16}. This decreases $v_{SD16,17}$ and, thus, it turns M_{18} off.

When M_{19} is just about to turn on, this is to say, when v_{SG19} is approaching v_{THP} but the drain currents of M_{19} and M_{17} are still zero), M_{18} and M_{16} drain currents are:

$$\begin{aligned} i_n &= \frac{\beta_B}{2}\left(V_{in} - v_p - v_{THP}\right)^2 \\ i_p &= \frac{\beta_A}{2}\left(V_{in} - v_p - v_{THP}\right)^2 . \end{aligned} \tag{2}$$

As M_{18} has the same drain current as M_{16}, we can write the first switching point of the hysteresis comparator:

$$i_n = \frac{\beta_B}{\beta_A} i_p \quad . \tag{3}$$

The same reasoning can be made for $i_n > i_p$ and we get the other switching point:

$$i_n = \frac{\beta_A}{\beta_B} i_p \quad . \tag{4}$$

Thus, notice that unequal βs fix comparator hysteresis. In our design, we have set $\beta_A = 2\beta_B$, and $I_{ref}=5\ \mu A$. As a consequence, the comparator switches at $i_n=2.5\ \mu A$ and $i_n=10\ \mu A$, which corresponds to linear regulator currents 200 times larger $i_1=0.5\ mA$ and $i_2=2\ mA$, respectively.

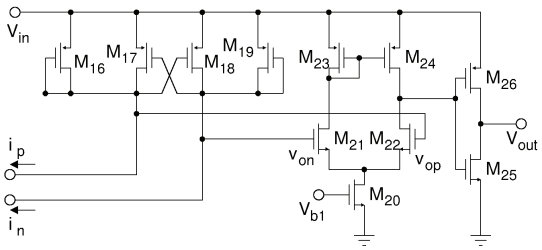

Fig. 3. Hysteresis current comparator

III. Simulation Results

The design has been validated by simulations where all devices are modeled using 180 nm technology from UMC with double well and normal and low threshold voltage transistors. The design must guarantee a constant output voltage of 1.1 *V* with an input from 1.5 to 1.8 *V* and a variable load current from 0 to 15 *mA*. Plot in Fig. 4 shows the transient behavior of the output voltage (V_{out}), load current (I_{load}), inductor current (I_{Ind}) and linear regulator current (I_{lin}) when load current suddenly switches from 0 to 15 *mA*, and vice versa. Note that the linear regulator supplies current to the load when the switching converter cannot supply it due to the sudden change at load impedance at 20 μs or sinks the excess current when load current is reduced abruptly. In addition, the linear regulator supplies the current required to compensate the switching behavior of current at the inductor and maintain the output stable. The voltage output is kept stable at 1.1 *V* except a small ripple of few *mV* when load current has a sudden change.

In Fig. 5 the output voltage (V_{out}) and the ripple output voltage (V_r) are plotted for different input voltages (V_{in}). The DC-DC converter can drive a proper output for input voltages above V_{in}=1.45 *V* with a constant output close to the nominal value, and a small ripple voltage (2 *mV*).

Finally, in Fig. 6 the power efficiency of the whole system is plotted for different load currents. As expected, the power efficiency increases for higher load currents up to 70% as the ratio of current supplied by the switching converter and current supplied by the linear regulator increases.

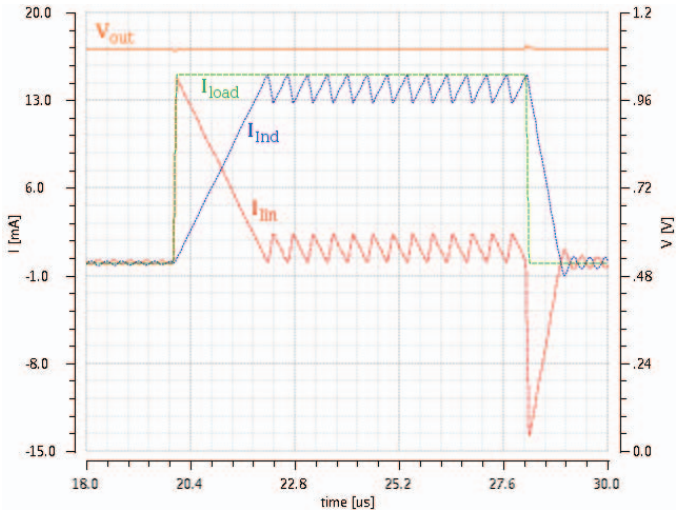

Fig. 4. Transient behavior of the proposed DC-DC hybrid converter to a current step from 0 to 15 *mA*, and vice versa showing its line regulation. Output voltage (V_{out}): straight line; load current (I_{load}): slashed line; Inductor current (I_{ind}): dotted line; linear regulator current (I_{lin}): slash-dotted line.

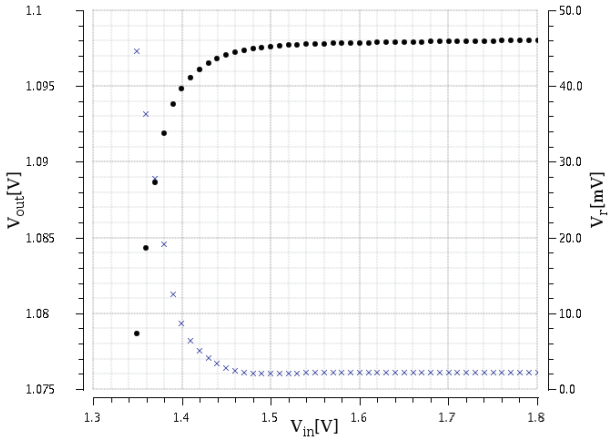

Fig. 5. Line regulation of the proposed hybrid DC-DC converter. Output voltage (V_{out}): black dots; ripple voltage (V_r): blue crosses.

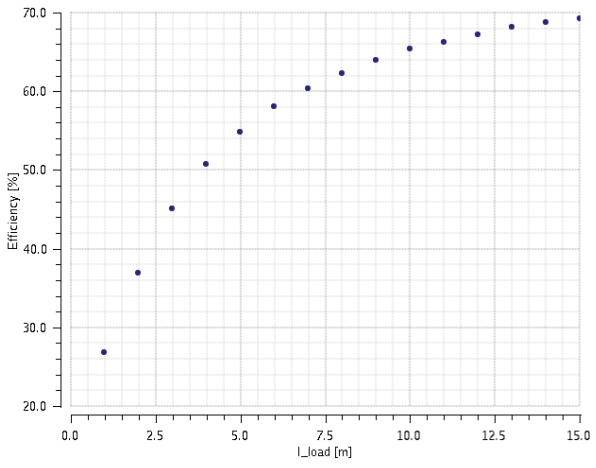

Fig. 6. Power efficiency of the proposed hybrid DC-DC converter for different load currents from 1 to 15 *mA*.

IV. Conclusions

Taking advantage of CMOS technology to implement on-chip DC-DC converters, this paper has shown the implementation of a CMOS hybrid or linear-assisted DC-DC regulator. Firstly, the paper shows that the proposed structure is well suited for voltage regulation for small to medium power consumptions of integrated circuits and achieves good static and dynamic characteristics. Secondly, it shows that the linear regulator, on one hand, eliminates the need for a filtering output capacitor and, on the other, it is able to supply sudden load current steps until the switching converter can supply the required current while keeping the output voltage stable with low ripple. While the switching converter supplies most of the steady-state current achieving good power efficiency, the linear regulator in parallel notably improves load regulation compensating fast load current variations. In this way, the design combines the best of linear and switching regulators compensating the drawbacks of both of them. Simulation results demonstrate the feasibility of the proposed structure and its appropriate load and line regulations.

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