$\mathcal{H}_\infty$ current controller for input admittance shaping of VSC-based grid applications

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***Abstract*—This paper presents a current controller that shapes, in the frequency domain, the input admittance of VSC converters connected to the grid. The controller is obtained by means of a $\mathcal{H}_\infty$ synthesis procedure, which minimizes the difference between the application closed-loop input admittance and a model-reference defined by the designer. This formulation achieves good accuracy in both modulus and phase. The proposed methodology allows the fulfilment of other current control objectives, such as current tracking, by defining frequency regions where each objective is desired. Experimental results show the good response of the proposed controller, both in frequency and time domain.**

***Index Terms*—Pulse width modulated power converters, current control, admittance, $\mathcal{H}_\infty$ control**

I. Introduction

THE INCREASING presence of power electronics-based devices in the power system, such as machine drives, power supplies, FACTS or renewable-energy interfaces is populating the grid of complex dynamics including non-linear behaviour, constant-power loading (CPL), control-loop induced resonances, etc. The results of recent investigations seem to mark those kind of dynamics as contributors-triggers-of power quality problems or even power system instabilities [1]–[4].

Although the problem, in its whole non-linear generality, is still under scientific discussion [4], [5], power electronic-based devices input admittance (see $\mathbf{Y}(s)$, Fig. 1), when linearised around the system operating point, is known to play a distinguished role on system stability and also on several power quality problems.

Its interest in power systems stability arises from [6], where a sufficient small-signal stability condition was derived based on the relation between impedances/admittances of the systems that are to be connected. More concretely, the stability relies on the Hurwitz condition of polynomial $D(s) = 1 + Z_s(s)Y_l(s)$, were Z_s and Y_l are the series equivalent impedance and admittance of the *main* power system and of the new connected *load*, respectively. The criterion has been further studied on [7]–[10].

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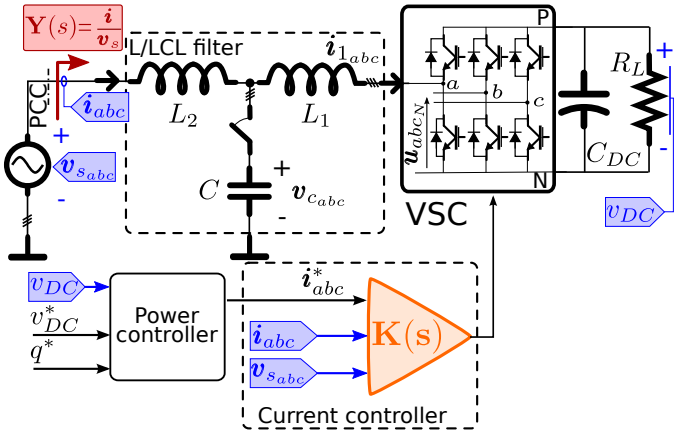

Fig. 1. Proposal block diagram: Active rectifier connected to the grid via L or LCL filter. In orange colour the proposed controller. In blue colour the measured signals.

This theoretical framework has motivated the publication of several works dealing with the shaping of converter closed-loop input admittance. A popular approach is to impose conditions over admittance module to ensure stability. Works [11]–[18] share the strategy of modifying the converter admittance on a particular -problematic- frequency, or in a small set of discrete frequencies, using classical control design procedures. In general terms they offer satisfactory results on the target frequencies, but the design problem complexity induces limitations when facing wide-band designs, and also in the management of the trade-offs between the admittance at different frequencies and other control objectives such as reference tracking or relative stability. [6] has also served to enunciate stability conditions based on the phase of the admittance transfer function of the connected converter. The most important approach on this direction is based on the known result from system theory stating that the connection of a passive [19] loads improves the relative stability of the complex system. [20]–[23] propose the use of feedforward and feedback modifications to ensure admittance passivity, modifying its phase, sometimes at the cost of uncontrolled modulus modifications. Finally, an open approach to the improvement of stability of interconnected systems has emerged from the recent work [5] where it is derived that negative imaginary systems may be beneficial from this point of view, although there have not been proposals developing this line.

Admittance shaping is an interesting topic also in the field of power quality were there have been proposals on different directions. On the field of FACTS it has been identified as a good alternative to damp resonances that facilitate the propagation of voltage and current harmonic through distribution or transport networks. The works developing this idea [24]–[30] present limitations similar to those expressed before. Finally, and although they are usually approached in a different way, active damping techniques or droop control techniques could be considered admittance shaping approaches [12], [14], [17], [31]–[33].

The present work proposes a systematic design procedure that allows to shape the converter input admittance, in modulus and phase, for wide frequency bands and handling other control objectives, such as reference tracking or stability, from a holistic point of view. The obtained flexibility may allow the use of the procedure to obtain controllers valid for all the scenarios described above.

To achieve that objective, the control problem is formulated as a model-reference based $\mathcal{H}_\infty$ synthesis procedure. More concretely, the designer provides the procedure with two model-reference transfer functions: one that specifies the desired input admittance and another that specifies the desired reference-tracking dynamic model (relationship between current reference, and grid injected current). As both objectives are not achievable at the same frequency, the designer also provides the algorithm with a frequency distribution of both control objectives. The process result is a discrete-time controller suitable for being programmed and executed in a DSP. The proposal is illustrated using a PWM rectifier application but is flexible enough to be applied to different control schemes and converter topologies.

This approach has been already explored by authors in [34], [35] obtaining promising preliminary results for simplified ideal scenarios. This manuscript extends the procedure to deal also with LCL filter structures, simplifies three-phase approach and integrates the controller in a realistic application with several hierarchical controllers in operation. The manuscript also gives a wide exploration of the possibilities and inherent limitations of the control design procedure, suggesting important design guidelines for the practical application of the method. In addition a complex experimental set-up has been prepared to obtain an actual experimental testing of the proposal.

The solution of the problem in the $\mathcal{H}_\infty$ framework transfers part of the design complexity to a computational algorithm, allowing the designer to deal with different complex control objectives in an tractable way. Following a model-reference design allows an accurate shaping in both modulus and phase. The convex nature of the underlying optimisation algorithm guarantees that an (sub)optimal controller is found. Although its presence on the control of DC/AC converters is still incipient, some approaches have been published in the field of current and voltage control reference tracking control, robust control, etc. [36]–[44].

The next section is dedicated to describe the theoretical basis of the design procedure. Section III gives practical insight into the design procedure, the underlying existing limitations and the implementation details. Section IV gives a summary of the different experimental tests followed to verify the proposals. The paper ends with a discussion of the conclusions extracted from the presented work.

II. Theoretical Background

A. System description and control objectives

The proposed current control design scheme has been applied to a PWM VSC-based active rectifier (see Fig. 1). This application represents a good benchmark plant, allowing a simultaneous testing of the current reference tracking (which comes from the power controller, Fig. 1) capabilities and of the admittance ($\boldsymbol{i}/\boldsymbol{v}_s$) emulation accuracy. Additionally, it is general enough to suggest that obtained results could be extrapolated to other common grid topologies or applications such as machine-drive front-end, FACTS, etc.

The control structure is divided in a classical two-hierarchical-levels control scheme: in the highest level, the load voltage is regulated to a given reference v^*_{DC} by the power controller (Fig. 1). This voltage reference, together with a possible reactive power reference q^*, will serve as inputs for the power controller block that will generate an AC current reference, namely $\boldsymbol{i}^*_{abc}$ that satisfies the desired power balance for a given -measured -Point of Common Connection (PCC) voltage, $\boldsymbol{v}_{s_{abc}}$.

To achieve both objectives the design follows a model-reference approach: the designer gives two reference models $\mathbf{Y}_{ref}$ and $\mathbf{T}_{ref}$. The former describes the desired relationship between the grid PCC voltage $\boldsymbol{v}_s$ and the grid current $\boldsymbol{i}$; in other words, the system input admittance. The latter describes the desired relationship between the grid current reference, $\boldsymbol{i}^*_{abc}$, and the actual grid current, $\boldsymbol{i}_{abc}$. It will later become evident that both objectives cannot be fulfilled at the same frequency so, additionally, the designer has to make a frequency distribution of the control objectives.

B. Dynamic Modelling

The active rectifier, shown in Fig. 1, is controlled in the $\alpha\beta$ stationary reference frame [45]. Expressing a three-wire converter control problem in $\alpha\beta$ reference frame allows to operate under unbalanced conditions in a natural way, removing component coupling and, thus, reducing the original MIMO problem to the control of two identical SISO uncoupled systems. The theory and procedures exposed on this proposal are expressed for only one control channel (α or β) and, similarly, the obtained controller will have to be executed twice, once for each component. As a consequence, the obtained closed-loop admittance will be equal for both components, being it a balanced three-phase admittance. It is also worth to remark that the design procedure could be translated into other typical reference frames, for instance, in synchronous dq axes.

Focusing on the inner control level process, the grid current in Fig. 1 follows the next linear dynamic expression, expressed in Laplace domain:

$$I(s) = G(s) \cdot U(s) + G_d(s) \cdot V_s(s), \tag{1}$$

where I, and V_s are the grid injected current and and the Point of Common Conection (PCC) voltage, respectively. $U(s)$ represents the averaged value, over a PWM half-period (T_s), of the voltage $\boldsymbol{u}_{abc_N}$ (VSC block on Fig. 1) that is generated by the PWM signals applied to the power devices gates. Transfer functions $G(s)$ and $G_d(s)$ are the open-loop command-to-output and input open loop admittance, respectively.

These last transfer functions are extracted from the differential equations that describe the system dynamics and are dependent on the grid filter that is used. For the L filter the transfer function are

$$G(s) = -\frac{1}{sL_f + R_f} \qquad G_d(s) = \frac{1}{sL_f + R_f}, \tag{2}$$

where $L_f = L_1 + L_2$ and $R_f = R_1 + R_2$ are the filter inductance and its parasitic equivalent resistance, respectively.

In the case of using an LCL filter, the following transfer functions are obtained

$$G(s) = -\frac{1}{sC(R_1 + sL_1)(R_2 + sL_2) + R_f + sL_f}, \tag{3}$$

$$G_d(s) = \frac{sC(R_1 + sL_1) + 1}{sC(R_1 + sL_1)(R_2 + sL_2) + R_f + sL_f}, \tag{4}$$

where L_1, R_1, L_2 and R_2 are the converter-side and grid-side inductance and resistance, respectively.

The outer DC-bus voltage controller is designed using a classical active power balance approach similar to the one described in [46]. Its design is out of the scope of this work that will only consider its main characteristics.

C. Controller structure and synthesis

Fig. 1 shows the structure where the proposed controller is integrated. The current controller, in orange colour, $\mathbf{K}(s)$, has three inputs: the PCC grid voltage measurement, namely $\boldsymbol{v}_s$, the grid reference current $\boldsymbol{i}^*$, and the sensed grid current $\boldsymbol{i}$. From the information provided by these three inputs the controller computes the average voltage at VSC AC terminal outputs, $\boldsymbol{u}$, needed to achieve control objectives. The controller transfer matrix is computed as a whole by the control design algorithm, however it is interesting to observe that, dividing the transfer matrix in rows: $\mathbf{K}(s) = [K_s(s) \quad K_{ref}(s) \quad K_i(s)]^T$, the actuation signal can be calculated as:

$$U(s) = K_s(s)V_s(s) + K_{ref}(s)I^*(s) + K_i(s)I(s). \tag{5}$$

Controller $\mathbf{K}$[1] can be considered, thus, to be formed by the addition of a grid voltage feedforward action (K_s), a current reference precompensation action (K_{ref}) and a grid current feedback action (K_i).

Expressing the closed-loop grid current, I, using the aforementioned structured transfer function, the following expression is obtained:

$$I = \underbrace{(1 - GK_i)^{-1}GK_{ref}}_{T(s)} I^* + \underbrace{(1 - GK_i)^{-1}(G_d + GK_s)}_{Y(s)} V_s, \tag{6}$$

[1]For notation compactness, the Laplace variable 's' is omitted when its presence results obvious attending to the context.

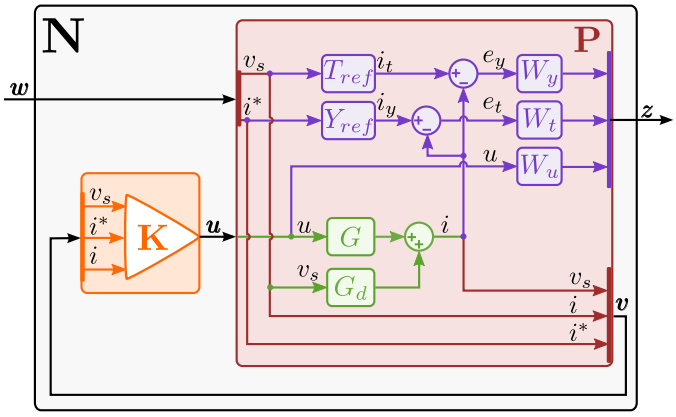

Fig. 2. General Control Problem (for any of the $\alpha\beta$ components) used for the $\mathcal{H}_\infty$ synthesis. The open-loop transfer functions are coloured in green, purple elements are added in the design process for controller synthesis. $\mathbf{P}$, in red colour, wraps around both. The desired controller $\mathbf{K}$ is shown in orange. Closed-loop system, $\mathbf{N}$, in black, results from connection of $\mathbf{P}$ and $\mathbf{K}$.

where T and Y are the closed-loop tracking and admittance transfer functions. It is important to note that system stability depends only on the system open-loop transfer function $L = -GK_i$.

Controller $\mathbf{K}$ is obtained through an $\mathcal{H}_\infty$ synthesis process that uses, as its entry point, the general control problem formulation, or generalised plant $\mathbf{P}(s)$ [47]. This virtual plant is a mathematical instrument that incorporates the open-loop plant and admittance transfer functions, G and G_d, respectively, a set of extra transfer functions that are used by the designer to specify the main control objectives and restrictions and, also, the control loop architecture. Structurally, $\mathbf{P}$ is a plant with two (vector) inputs and two (vector) outputs:

$$\begin{bmatrix} \boldsymbol{z} \\ \boldsymbol{v} \end{bmatrix} = \mathbf{P} \begin{bmatrix} \boldsymbol{w} \\ \boldsymbol{u} \end{bmatrix}, \tag{7}$$

where $\boldsymbol{w}$ is called exogenous inputs vector to the system, usually composed of references and disturbances. $\boldsymbol{z}$ is the vector of the so-called output *error* signals, that are to be minimised in some sense to meet control objectives, $\boldsymbol{u}$ is the actuation vector that will be computed by the controller and $\boldsymbol{v}$ is the measurements output vector that will enter the controller.

With the implicit information provided by $\mathbf{P}$, the $\mathcal{H}_\infty$ synthesis process computes a (sub)optimal controller $\mathbf{K}$, which minimises the infinity norm[2] of the closed-loop system $\mathbf{N}$ that results from the feedback interconnection of $\mathbf{P}$ and $\mathbf{K}$, and relates exogenous input vector $\boldsymbol{w}$ and *error vector* $\boldsymbol{z} = \mathbf{N}\boldsymbol{w}$, as shown on Fig. 2.

Minimising the closed-loop function infinity norm is equivalent to minimising the ratio between the energies (norm-2) of the *error vector* $\boldsymbol{z}$ and the exogenous vector $\boldsymbol{w}$:

$$\min_{\mathbf{K}} ||\mathbf{N}(\mathbf{K})||_\infty = \min_{\mathbf{K}} \frac{||\boldsymbol{z}||_2}{||\boldsymbol{w}||_2} \leq \gamma. \tag{8}$$

[2]The infinity norm of a MIMO system $\mathbf{H}(s)$ in the frequency domain is defined as $||\mathbf{H}(s)||_\infty \triangleq \sup_\omega \bar{\sigma}(\mathbf{H}(j\omega))$, where $\bar{\sigma}(\mathbf{H}(j\omega))$ is the maximum singular value of $\mathbf{H}(j\omega)$.

In other words, the synthesis process computes the controller that minimises the energy of the error signals for the considered set of disturbances, references and other exogenous signals. The designer task is, then, to choose the appropriate error signals and shape them to accomplish the control objective. In fact, choosing an inner structure for $\mathbf{P}$ that is effective in practice is the design keystone in this control paradigm.

The principle behind this control proposal is the minimisation of the difference between the output current of a designer provided Y_{ref} and that of the actual converter; if, given the grid PCC voltage, this difference is *small*, the converter would be following the admittance model, accomplishing the main objective of this work. Current tracking is approached in a similar manner.

Fig. 2 shows the proposed structure for $\mathbf{P}$. Over the diagram, green elements represent the actual plant under control. The plant output, i, is the result of adding the outputs of G and G_d transfer functions. These components model the contributions of the control actuation, u, and grid voltage, v_s, over i, respectively. Purple elements are added in the design process for controller synthesis. e_t is the difference between plant output i and the tracking reference model T_{ref} output, i_t. In a similar way, e_y is the difference between i and i_y, the output of the admittance reference model Y_{ref}. Controller actuation u has also to be added as a minimisation signal in order to avoid unnecessary -or impossible -control efforts. All these three variable are then multiplied by frequency weights (W_t, W_y, W_u, respectively), that emphasise the range of frequencies where each variable has to be minimised. Their outputs compose the $\boldsymbol{z}$ output vector. Finally, the controller that is produced from the synthesis process is displayed on green colour. Note that the inputs to the controller are all the exogenous signals ($\boldsymbol{w}$ vector) together with the plant measurements, i signal, namely $\boldsymbol{v}$ in the standard notation of (7). The controller output is the plant actuation signal, u.

Summing up, output and input signal vectors of generalised plant $\mathbf{P}$ defined in Fig. 2 are then:

$$\boldsymbol{z} = \begin{bmatrix} W_t \cdot e_t \\ W_y \cdot e_y \\ W_u \cdot u \end{bmatrix} \quad \boldsymbol{v} = \begin{bmatrix} v_s \\ i^* \\ i \end{bmatrix} \quad \boldsymbol{w} = \begin{bmatrix} v_s \\ i^* \end{bmatrix} \quad \boldsymbol{u} = u \tag{9}$$

It is important to stress on the way i_y and i are compared: e_y is calculated as the subtraction of both signals. As a consequence good admittance control can be achieved not only in modulus, but also in phase. Admittance transfer function phase is a key parameter because important dynamical properties, as for example dissipativity [19], depend on it.

Design of frequency weights has also a strong influence on the obtained controller $\mathbf{K}$: the signals involved in the $\boldsymbol{z}$ vector are actually incompatible from a minimisation point of view as it is not possible to mimic a certain admittance in the frequency bands where good tracking is required, and, also, it is not possible to minimise control effort at the same frequencies. The correct design of the functions inside $\mathbf{P}$ is, to a large extent, application dependent and is dealt in more detail in the next section.

III. Practical considerations

A. Design of current controller: reference model and weighting function selection

The generalised plant presented on § II-C is general enough to handle a wide variety of VSC control problems. The objective of this section is to settle some design heuristic rules that have been found to be useful by the authors.

As stated on previous sections, a designer following the described control architecture and methodology is requested to define five transfer functions, grouped in two classes. The first group is composed of the transfer functions that serve as reference models for current tracking or admittance shaping purposes. The second group is integrated by those transfer functions that emphasise -weight- the importance of the different reference models, or the control effort, for the different frequency bands.

1) Reference model selection: The reference models are used to specify, by the designer, how the grid injected current (i in Fig. 2) tracks the exogenous current reference (i^*, in Fig. 2) and the converter input admittance.

In typical applications the grid current is required to accurately track the provided reference, at least in a band around the fundamental frequency and, possibly, also in some of its lower order harmonics. Facing the design from a reference-model point of view, the easiest approach is to choose a $T_{ref} = 1$. Such a broadband tracking objective is clearly unachievable (and incompatible with any non-null admittance objective). The tracking reference weighting function (W_t) will serve as an effective tracking band-limiter.

The range of possibilities for admittance reference model (Y_{ref}) is wider and more application dependent. Although usually low-valued power-dissipative (resistive) responses are preferred, other behaviours could be considered. § III-B, below, shows some different example designs that can give an idea of the design method flexibility.

2) Weighting functions selection: The control strategy presented in this proposal is a trade-off problem generated by several inherent incompatibilities and constraints:

- Tracking and admittance control objectives are incompatible as they try to make the grid injected current follow the tracking and the admittance reference model output current, which are, in general, different. The designer has to choose which model is important for the different frequency bands.
- Control effort magnitude has to be reasonable inside the control band. For this reason it has to be included in the output error vector $\boldsymbol{z}$: if it were not, the optimization of $\|\|\mathbf{N}\|\|_\infty$ would possibly arrive to an optimum solution with not realistic actuation signals that would saturate the plant input (maximum duty cycle on PWM).
- Control band limitation. Given the sampled-time nature of the proposed control algorithm, actuation should be attenuated to a great extent before Nyquist frequency, f_{Ny}. This limitation represents a maximum limit on the band where control objectives can be achieved. Other band limitations are to be added in the case that the plant exhibits non-minimum phase behaviour or a delay in the

control input. These important topics will be more deeply dealt in § III-C.

The designer deals with these trade-offs by means of the frequency weighting functions. To properly understand its utility it helps to remember that the $\mathcal{H}_\infty$ controller synthesis algorithm tries to obtain a controller that keeps the error output vector $\boldsymbol{z}$ small. This way, a frequency weight that (relatively) amplifies a signal in a band, would yield a controller that keeps the unweighted actual signal smaller inside that band. In a similar fashion a weight (relatively) attenuating a signal in a band will induce a bigger actual unweighted signal in the closed-loop system. This article proposes the use of three different weighting functions:

- $W_t(s)$ transfer function weights the error with respect to the tracking reference model. If $T_{ref} = 1$ has been chosen, it weights the tracking error. High values are used for bands were good reference tracking is desired. In the case the controller is used in a PWM rectifier application, the designer has to take into account that the tracking band should be about ten times wider than the band of the DC-bus/power controller that generates the current reference, to ensure the current accurately tracks it.
- $W_y(s)$ weights the error with respect to the admittance reference model. High values are used for bands were good admittance shaping is desired. It has to be remembered that admittance and reference tracking are not compatible, so their respective weighting functions should be complementary.
- $W_u(s)$ weights the actuation in two senses: it is used to limit the maximum control bandwidth but also to limit the maximum control effort within the control band. Thus, typically, W_u is a high-pass function. The transition between the low and high gain bands marks the frequency where control actuation is desired to be small, i.e. the stop-band beginning. The maximum control effort in the control band is adjusted by modifying the gain of W_u in that band: lower values allow a bigger control effort and vice versa. This value is usually adjusted to get a control effort near the saturation limit under nominal transients and disturbances as, for instance, voltage dips.

Fig. 3 presents a possible selection of the aforementioned weighting functions. The plot divides the spectrum in four different frequency zones. In first zone, placed at subsynchronous frequency range, W_y gets the bigger value, indicating that the objective is to follow the admittance reference model. The same applies to the third-band, on supersynchronous frequencies. Arround the grid fundamental frequency, W_t gets a very high value. This is used to achieve null error in tracking sinusoidal references and, in practice, will yield a controller with (almost) a resonant-part on that frequency. Finally, in the fourth interval W_u gain gets higher signalling the end of the control band.

B. Design examples

This section presents three study cases. The objective is to give more insight into the design process, emphasise the designer typical work flow and strategy and demonstrate the flexibility of the procedure respect to the plant model and control objectives.

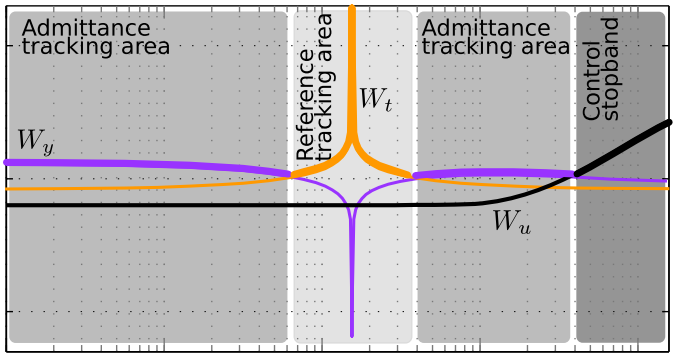

Fig. 3. Typical weighting function selection scenario

1) Broad-band admittance control (L filter): The first case proposes the design of an active rectifier whose admittance, outside the fundamental frequency range, presents purely resistive behaviour. The energy absorbed by the converter due to this dissipative behaviour is evacuated, by the DC-bus voltage controller, through the grid fundamental frequency. It is necessary, then, to provide the controlled system with fundamental frequency tracking capabilities. This objective may be achieved selecting, for instance, $Y_{ref} = 0.1\mho$ and $T_{ref} = 1$.

To distribute the different objectives along the spectrum this design uses the weights displayed on Fig. 4: W_t is chosen as a resonance in the grid fundamental frequency. A high gain ensures an accurate tracking. W_t bandwidth controls tracking transient response. Concretely it follows the structure:

$$W_t(s) = K_t \frac{s^2 + 2\zeta_n \omega_1 s + \omega_1^2}{s^2 + 2\zeta_d \omega_1 s + \omega_1^2}, \tag{10}$$

where $w_1 = 2\pi 60$ rad/s is the grid fundamental frequency, ζ_n varies the resonance bandwidth and ζ_n/ζ_d can be used to adjust the resonance peak maximum value.

Similarly, a complementary admittance weight W_y is defined using a notch characteristic in the fundamental frequency.

$$W_y(s) = K_y \frac{s^2 + 2\zeta_d \omega_1 s + \omega_1^2}{s^2 + 2\zeta_n \omega_1 s + \omega_1^2} \cdot \frac{1}{(1/\omega_y)s + 1}, \tag{11}$$

where w_y marks the maximum frequency where impedance emulation is desired. The notch part of the transfer function is designed following W_t criteria.

Finally, control effort is limited by the next weight:

$$W_u(s) = K_u \frac{(1/\omega_{u1})s + 1}{(1/\omega_{u2})s + 1}, \tag{12}$$

where the zero in ω_{u1} defines the frequency where control effort starts to be limited, in the beginning of the crossover band. The pole in w_{u2} marks the control stop band and the end of the crossover band. This pole is also needed to make W_u (and $\mathbf{P}$, Fig. 2) strictly causal, as required by $\mathcal{H}_\infty$ synthesis algorithm.

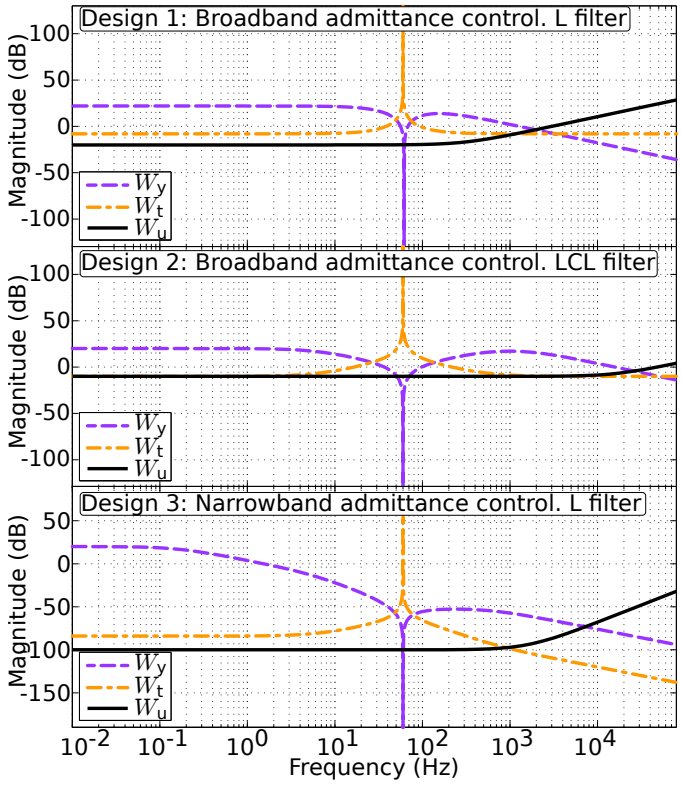

Fig. 4. Frequency weights for the different design examples.

2) Broad-band admittance control (LCL filter): This second example describes how the plant model affects the design flow. The control objective is the same as in the first example but the plant order has been increased by considering an LCL filter connection. Admittance reference is, again, a pure resistance $Y_{ref}(s) = 0.1\mho$. In this case the LCL resonance is also desired to be shaped, so control objectives spread over a wider band, using W_y equal to (11), but with a bigger ω_y.

Tracking reference is also kept as $T_{ref}(s) = 1$. This example has been designed to present a faster tracking behaviour. W_t follows, thus, (10) but selecting a wider bandwidth.

Control effort is shaped with W_u equal to (11). Again, the active control band is wider and ω_{u1} and ω_{u2} are selected to obtain actuation limitation at higher frequencies.

3) Narrow band admittance control (L filter): The objective of the third example is to illustrate the validity of the design proposal when considering higher-order reference models: process model is again an L-filter grid connected VSC but the desired admittance (outside the fundamental frequency) shows a resonant-like behaviour. From a hypothetical application point of view, this could be used, for instance, as a loss-less damper for a resonance placed at a known frequency. By using this resonance behaviour, admittance achieved on the desired frequency is larger than in previous examples, also minimising the influence over the rest of the spectrum and leaving more room for reference tracking, if needed.

The new admittance reference is:

$$Y_{ref}(s) = 0.01\frac{s^2 + 2\zeta_n\omega_{res}s + \omega_{res}^2}{s^2 + 2\zeta_d\omega_{res}s + \omega_{res}^2}\cdot\frac{1}{(1/\omega_{yref})s+1}, \quad (13)$$

where ω_{res} is the frequency where the maximum admittance is reached. The high frequency pole at ω_{yref} is used to make the admittance reference-model (Y_{ref}) more similar to the open-loop one (G_d), avoiding excesive control efforts on that frequencies.

Frequency range of admittance control is defined through a W_y equal in structure to (11) but with the real pole placed at lower frequencies to enhance its importance in subsynchronous frequencies.

Tracking reference is, again, $T_{ref}(s) = 1$; W_t changes slightly:

$$W_t(s) = K_t\frac{s^2 + 2\zeta_n\omega_1 s + \omega_1^2}{s^2 + 2\zeta_d\omega_1 s + \omega_1^2}\cdot\frac{1}{(1/\omega_t)s+1}, \quad (14)$$

The new pole at ω_t makes admittance control more dominant at frequencies above the fundamental (super-synchronous frequencies, where admittance resonance peak is placed) and below the control band upper limit (where W_u is dominant).

Control effort is again limited at high frequencies, with a weight W_u with similar dynamics to (12). This time it has double order to reduce crossover range, and be able to control admittance at higher frequencies.

$$W_u(s) = K_u\left(\frac{(1/\omega_{u1})s+1}{(1/\omega_{u2})s+1}\right)^2. \quad (15)$$

C. Controller limitations

The presented controller design and synthesis is subjected to the following known limitations:

1) Sampled-time implementation limitations: An inherent limitation in the practical implementation of discrete-time controllers is the impossibility of applying to the plant, in time k, an actuation computed with measurements also acquired in time k. In most power converter control scenarios signal acquisition time and controller actuation computation last for a non-negligible part of the controller sample time. The typical workaround is to postpone the actuation application until the arrival of the next sampling period. This is usually modelled placing a one-sample pure delay in the control input, z^{-1} in z-domain, of the plant discrete-time model. The existence of this delay introduces a high bound on the controller bandwidth, limitting the achievable bandwidth to [47]:

$$f_c < \frac{1}{2\pi T_s}, \quad (16)$$

which is, approximately, one third of f_{Ny}.

It is important to remark that this bound affects to both the feedforward and feedback components of the controller actuation, because both are affected by the input delay.

2) Waterbed limitations: The transfer function of the plant under control presents, as can be seen in (3), a relative degree: $rd(G(s)) = 3$. This fact makes applicable the Bode sensitivity integral theorem (first waterbed formula) [47] establishing a trade-off design decision between closed-loop performance and system robustness: increasing closed-loop performance at some frequencies comes at the cost of increasing the achieved sensitivity function infinity norm $||S(j\omega)||_\infty$, which

is a good inverse indicator of the design robustness. A commonly accepted design criterion is to synthesise loops with $||S(j\omega)||_\infty < 2$ (in natural units). This condition implies that the polar plot of $L(j\omega)$ lies outside of a circumference of radius > 0.5 centred at $(-1 + 0j)$, and, consequently, a gain margin bigger than 6 dB and a phase margin bigger than 30º.

3) Weight design limitations: In addition to the previous limitations, which actually have a clear indirect impact on the the design of the weighting functions, the latter are also subject to two additional limitations that have to be considered in the design process: i) Weights must be strictly stable and proper. Pure resonators and integrators are, thus, not allowed to be present in weight functions as they present poles over the $j\omega$ axis. There is no theoretical limitation, however, in placing them arbitrary close to the $j\omega$ axis. From a practical point of view, this limitation has no implication as the behaviour is practically equivalent. ii) Weight transfer function order. The order of the synthesised controller is that of the augmented $\mathbf{P}(s)$ plant transfer function. The three design weights are contained inside $\mathbf{P}$ so, an increase in their order implies an increase in the final controller, $\mathbf{K}$, order. The designer has to evaluate whether the performance improvement obtained by an extra state in a weight is worth the corresponding controller complexity increase.

D. Controller synthesis & implementation

The $\mathcal{H}_\infty$ synthesis tools are designed to work with continuous-time plants. The presented controller, however, is executed in a DSP, and thus, a discrete-time controller transfer function is needed. Using a direct discrete-time approximation of a continuous-time controller neglects important dynamics such as the pressence of a PWM modulator, that may be modelled as a zero-order hold, and the presence of a one-sample delay at the plant control input. To include such important elements, the zero-order hold discrete-time equivalent of $G(s)$ is computed and a one-sample delay element z^{-1} is added to it in the z domain. Fig. 5 shows a comparison of the frequency responses of $G(s)$, $G(z)|_{ZOH}$ and $z^{-1} \cdot G(z)|_{ZOH}$. It can be observed that, while the modulus of the transfer functions are similar, there are important differences in their phases that increase with frequency. While these differences could be neglected in the case of a reference-tracking controller with a conservative tracking bandwidth (relative to the switching frequency), in the case of the admittance shaping it would yield phase errors in the obtained closed-loop admittance.

After introducing these dynamic elements in the process, a continuous approximation of this plant is obtained via Bilinear transformation, making a frequency pre-warping to accurately preserve LCL resonance frequency. The open-loop admittance G_d can be directly included in the augmented plant $\mathbf{P}(s)$ as the grid voltage is, in fact, a continuous disturbance of the process. Frequency weights may also be directly expressed in continuous time, being conscious of the bandwidth limitations that are present because of the final objective of obtaining a discrete-time controller. Once the plant $\mathbf{P}$ is specified, the continuous-time controller, $\mathbf{K}(s)$ is obtained through a regular $\mathcal{H}_\infty$ synthesis process. The final discrete-time controller, $\mathbf{K}(z)$ is then obtained by computing a Bilinear transformation.

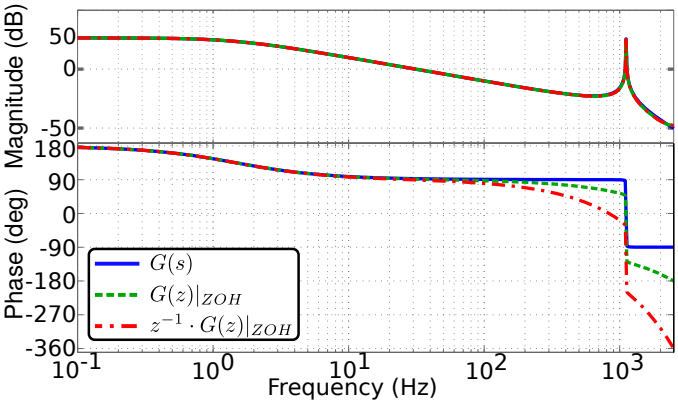

Fig. 5. Frequency responses of the continuous open-loop plant, $G(s)$, its Zero-Order Hold discrete-time equivalent, $G(z)|_{ZOH}$, and the delayed ZOH discrete-time equivalent, $z^{-1} \cdot G(z)|_{ZOH}$.

Algorithm 1 Controller synthesis procedure

```
1:  procedure CONTROLLER SYNTHESIS(G,GD,TS)
2:  Weight definition:
3:      Wu=tf(...); Wt=tf(...); Wy=tf(...);
4:  Process model:
5:      delay=tf([1],[1 0],ts);
6:      G_z=delay*c2d(G,ts,'zoh');
7:      G_eq_cont= d2c(Gz,'bilin',...);
8:  P assembly:
9:      systemnames='G Gd Yr Wy Tr Wt Wu';
10:     inputvar ='[e;i_ref;u]';
11:     outputvar = '[Wy;Wt;Wu;e;i_ref;G+Gd]';
12:     input_to_Wy='[Yref-G-Gd]';
13:     input_to_Wt='[Tref-G-Gd]';
14:     input_to_Wu='[u]';
15:     input_to_Yr='[e]';
16:     input_to_Tr='[i_ref]';
17:     input_to_G= '[u]';
18:     input_to_Gd= '[e]';
19:     P=sysic;
20: K synthesis:
21:     [K_cont,gamma]=hinfsyn(P,...);
22:     if (gamma>gmax) then goto Weight definition
23:     K=c2d(K_cont,'bilin',...);
24:     end
```

The algorithm synthesis is performed using MATLAB standard library and also its Robust Control Toolbox[3]. The transfer functions used in $\mathbf{P}$ are created using standard `tf`, `ss` commands. Continuous to discrete conversions, and vice-versa, are performed using `c2d` and `d2c`. Once they are created, process $\mathbf{P}$ is assembled using the scripting tool `sysic`. The controller is then synthesised using `hinfsyn` command. The snippet displayed on Alg. 1 describes the procedure used to obtain the final controller.

Once the controller is obtained, it is programmed in C code using a state-space description of the controller:

[3]The synthesis procedure here described represents only one alternative that has been found particularly intuitive by the authors but similar results could be obtained by different approaches.

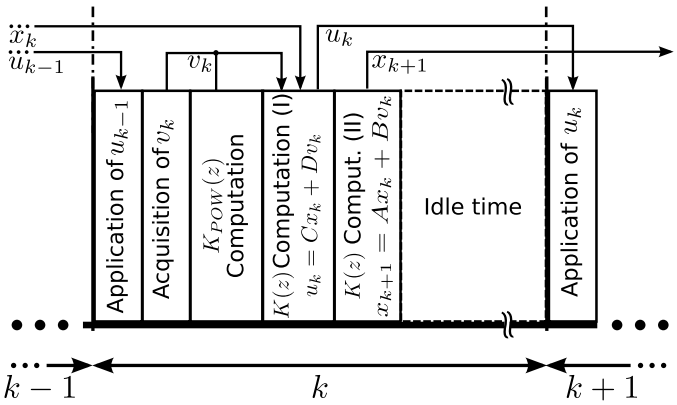

Fig. 6. Chronogram of the implemented control algorithm. The blocks show the different tasks executed in the processor unit. The arrows show the data flow between tasks and sample periods.

TABLE I
EXPERIMENTAL SETUP PARAMETERS

S	17.5 kVA	L_1	3.4 mH
V_g	120 V	R_1	28.8 mΩ
ω_1	$2\pi 60$ rad/s	L_2	1.7 mH
V^*_{DC}	700 V	R_2	18.6 mΩ
T_{sw}	400 μs	C	18 μF
T_s	200 μs	C_{DC}	4.7 mF
$K_{POW}(z)$	$K_p + \frac{K_I T_s}{(z-1)}$	K_I, K_P	0.2893, 0.0369

$$\begin{aligned} \boldsymbol{x}_{k+1} &= \mathbf{A}\boldsymbol{x}_k + \mathbf{B}\boldsymbol{v}_k \\ \boldsymbol{u}_k &= \mathbf{C}\boldsymbol{x}_k + \mathbf{D}\boldsymbol{v}_k \end{aligned} \tag{17}$$

where, $\boldsymbol{x}$, $\boldsymbol{v}$ and $\boldsymbol{u}$ vectors stand for the controller state, plant outputs measured by the controllers and controller actuation, respectively, and $[\mathbf{A}, \mathbf{B}, \mathbf{C}, \mathbf{D}]$ are the controller state matrices. Fig. 6 shows a diagram of the different tasks executed during a sample period in the DSP. The period starts updating PWM signals with the actuation computed during the previous sampling period, u_{k-1}. This time shift is reflected as the one-sample delay at the plant input. Next, signals from sensors are acquired. With those data, higher hierarchy loops, in this case the DC-bus voltage controller, are computed, obtaining the appropriate references for the current controller. The controller is executed in two steps. First the actuation to be applied in the next period, u_k, is computed. Finally, the controller internal states are updated, calculating x_{k+1}, before the DPS goes idle until the next period arrives.

IV. Results

The proposed control scheme has been verified by both simulation and experimental testing. The experimental set-up (see Fig. 7) consists of the connection between a AC programmable power supply Pacific SmartSource 345-AMX, emulating the grid, and a 17.5 kVA two-level VSC connected to it through an LCL or an L filter (Table I shows the main parameters of the set-up). A bank of passive loads is connected to the DC-bus to test the application under different operating points.

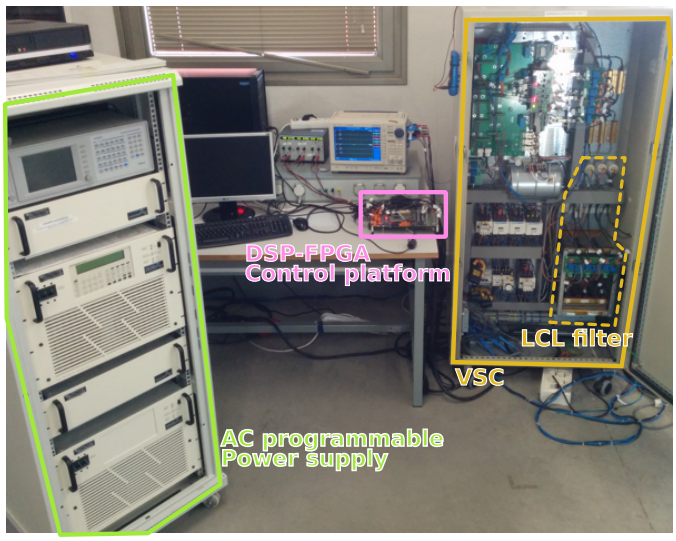

Fig. 7. Experimental Set-up

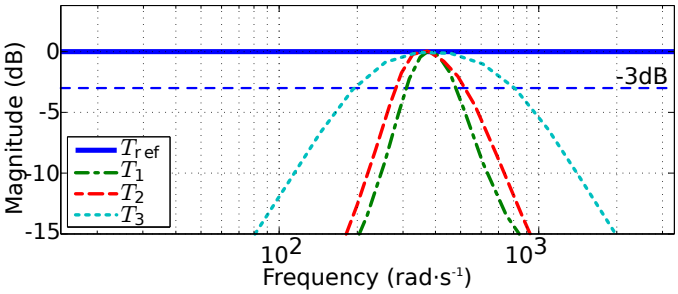

Fig. 8. Closed-loop analytic reference-tracking transfer function for the example designs $T_n(s)$, where n is the number of the design (refer to § III-B). Blue colour shows the reference model for all designs.

Control application is implemented on a Texas Instruments DSP TMS320DSK6713 based control platform described in detail in [48].

The experimental values of the closed-loop system admittance are obtained by adding a three phase controlled sinusoidal signal to the voltage generated by the AC power supply. The AC power supply has a connector (J5), with three analog inputs where the user can place reference voltage signals. These voltage signals are internally amplified and added to each one of the phases of the main power supply output. To obtain the experimental admittance value on a particular frequency, a three-phase balanced sinusoidal signal of a particular frequency was added to the main AC voltage. The generated voltage signal and the corresponding injected currents are then acquired at 5 kHz, ensuring that the possible transient effects have already finished and that the data registry contains several cycles of the injected signal. Voltage and current data are, then, converted to the $\alpha\beta$ reference frame, analysed with the MATLAB `fft` command, and divided to obtain the experimental value of the converter input impedance/admittance.

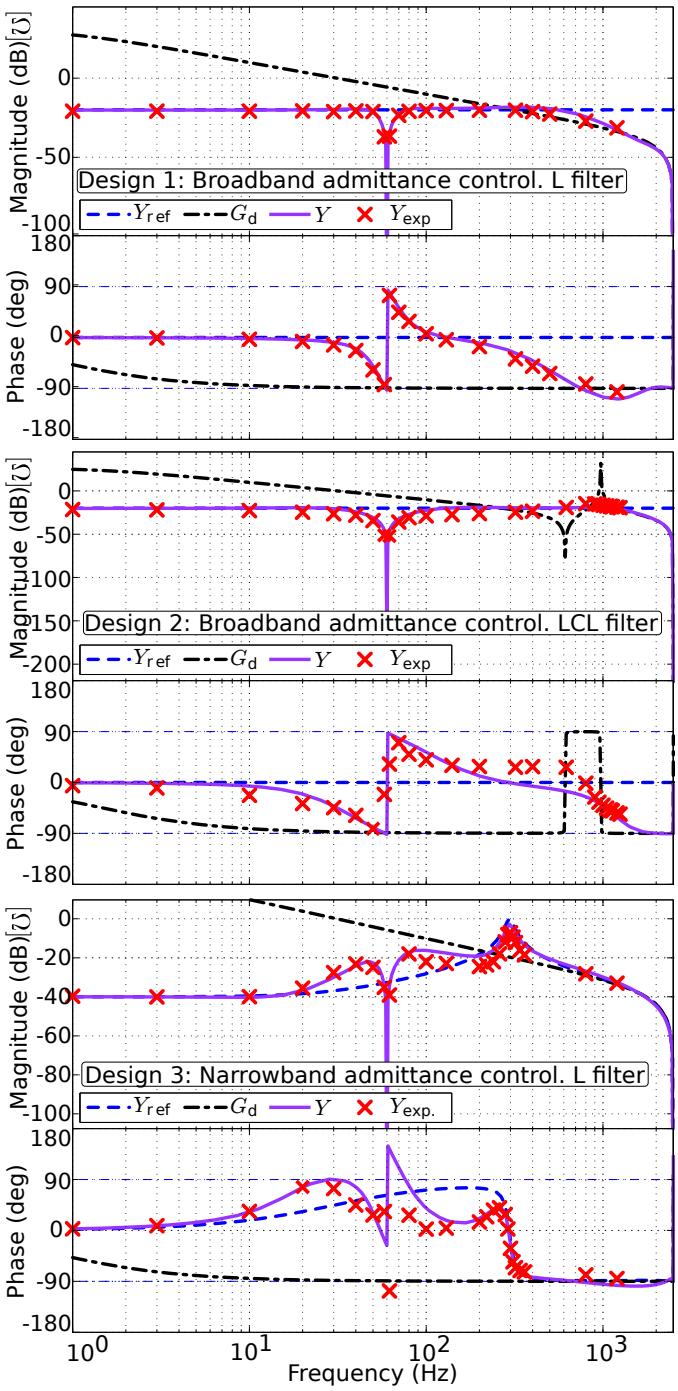

Fig. 9. Admittance frequency results. Open-loop admittance G_d is shown in black. Admittance reference model is shown in blue colour. The closed loop synthesised admittance (theoretical) is shown in purple. Red crosses show the experimentally measured admittance.

A. Frequency domain results

The three design cases described on § III-B have been implemented and tested to verify the validity of the described control proposal. Fig. 8 shows the closed loop analytic tracking function for the three designs. It can be observed that all designs achieve good tracking capabilities. The achieved bandwidth is different for the three designs, because it was specified that way during the design process.

Similarly, Fig. 9 evaluates the admittance shaping capabilities of the proposed control scheme. Over the figures, it can be seen the open-loop admittance G_d, the desired admittance reference model Y_{ref}, the theoretical closed-loop admittance (using the theoretical plant G and G_d and the synthesised controller, K) and the experimentally identified system admittance, for a discrete number of frequencies. It can be observed that the synthesised controller effectively shapes the system admittance in the three cases: as expected the admittance follows the reference below and above the fundamental frequency, up to the system control bandwidth. Around the fundamental frequency there is a transition zone, that may be shortened, if needed, by increasing resonators order in the corresponding weights.

The system admittance that has been experimentally identified accurately tracks the theoretical closed-loop admittance. Some minor errors on the phase values, probably due to inductance modelling errors, can be observed above the fundamental frequency.

B. Time domain results

The second design example (§ III-B) is used to validate the transient and tracking capabilites obtained with the proposed design procedure. Fig. 10 shows the initial converter connection and DC-bus charging to its nominal value (700 V). Fig. 11 shows the system behaviour when a 4.2 kW load is connected to the DC-bus. Fig. 14 shows the system behaviour under a soft reactive power change. Finally Fig. 13 shows system evolution when the grid suffers an unbalanced dip.

V. Conclusion

This paper presents a new current controller design methodology for simultaneous input admittance and current tracking control in power converter-based application. Presented controller is based on $\mathcal{H}_\infty$ synthesis, and allows admittance frequency shaping, in both magnitude and phase, by means of defining frequency-based admittance references for complete frequency bands. This feature allows, for example, defining system dissipativity, the active damping of system's resonance, define high/low impedance paths or fulfilment of impedance stability criterion (commonly used to predict stability in multi-converter networks). This feature extends the capabilities of previous appraches to the problem of closed-loop admittance shaping.

Proposed methodology is verified in a three phase active rectifier, which simultaneously fulfils a dual control objective: tracking of a current reference which comes from a DC-side voltage, whose design lies out of the scope of this proposal, and control of the application's input admittance. This is possible if the frequency ranges of both control objectives do not overlap, which can be achieved by defining frequency-weights in the $\mathcal{H}_\infty$ controller structure. Control operates in $\alpha\beta$ axes and was tested for both L and LCL filter topologies, measuring only the grid current and voltage, as well as the DC-bus voltage.

Designing criteria for the proposed controller is given. To demonstrate the proposed admittance control generality and

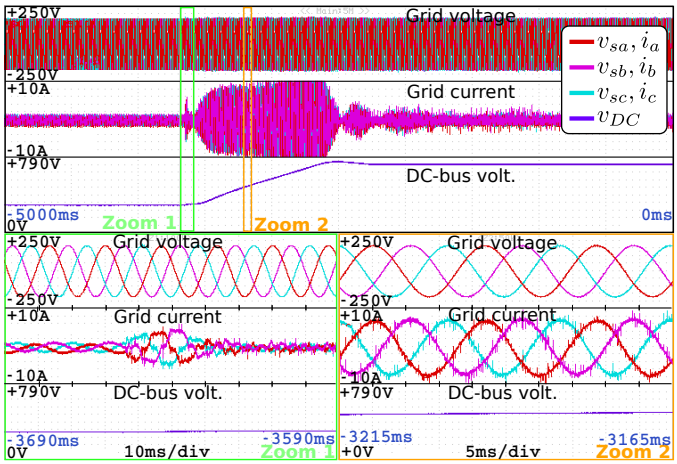

Fig. 10. Initial grid connection. General view shows DC-bus charging from the diode-rectified level to the nominal value (700 V). Zoom 1 shows the current transient when PWM starts. Zoom 2 details system signals during bus boosting. After elevation currents go null because bus is unloaded.

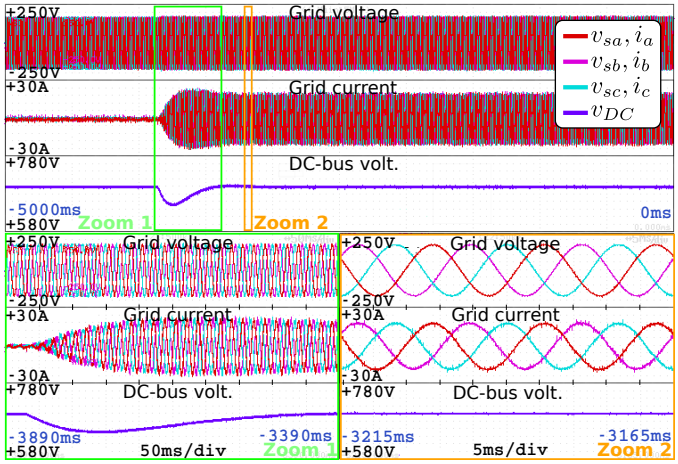

Fig. 11. Connection of a 4.2 kW DC-load with a null reactive reference. Top shows the complete transient. Zoom 1 focuses on the currents and DC-voltage evolution after the connection. Zoom 2 shows grid currents and voltages in steady-state.

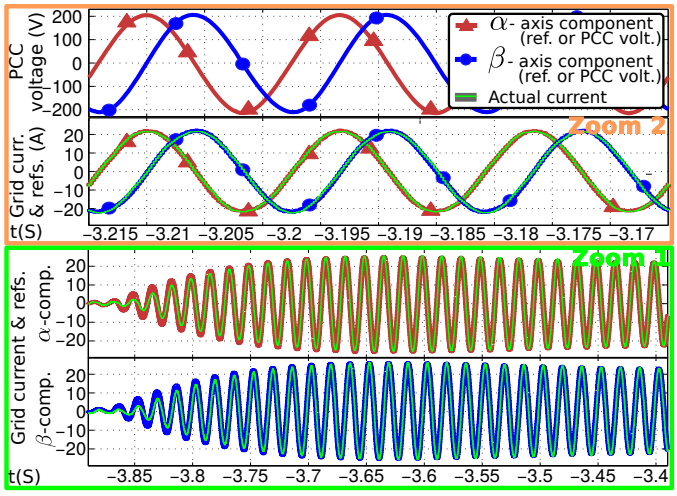

Fig. 12. $\alpha\beta$ components evolution for zoom ranges of transient in Fig. 11. (Zoom 2) Top: PCC $\alpha\beta$ voltages. Botton: $\alpha\beta$ grid consumed currents and references. (Zoom 1) Top and botton: Grid consumed current and the reference provided by the outer controller for the α and β components, respectively.

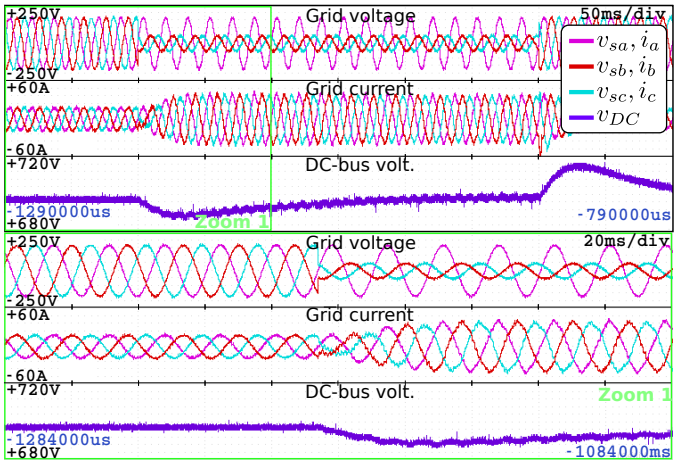

Fig. 13. Response under grid voltage dip (type E [49]) when DC-bus is loaded with 4.2 kW. Phases b and c fall to 30% of its value keeping their phase untouched. Top view shows the complete transient in grid voltages, currents and DC-bus voltage. Lower view focuses on the dip initial edge.

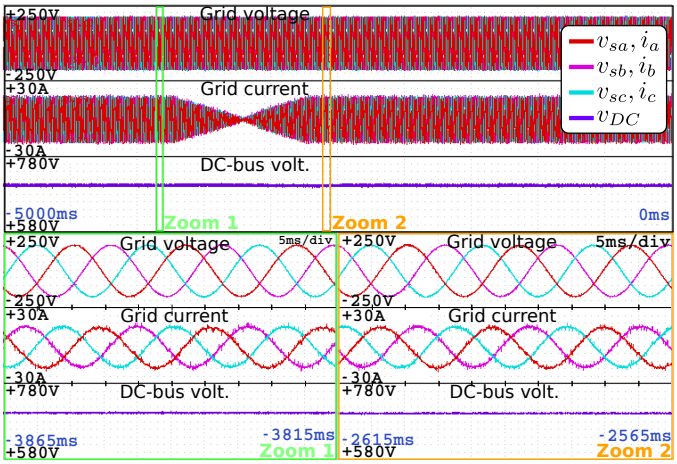

Fig. 14. Change in the reactive power reference. With the DC-bus unloaded, reactive power reference goes from 4 to -4 kVAr. Power controller forces the transient to follow a slope. Top view shows the complete transient. Zoom 1 and 2 focus on the phase between grid voltage and currents for both references.

feasibility, three different admittance references were considered: admittance control over a broad-band for both L and LCL filter topologies, making the active rectifier behave as a resistance and actively damping the LCL resonance, and a design that defines a low impedance path around a given frequency and a high impedance path for the rest.

All the proposed designs are experimentally implemented and tested, with both good frequency and time domain results. Future works would consider the effect and capabilities of the proposed algorithm in more complex grid connected scenarios, with several active components connected to the same AC grid and its effect over the proposed control algorithm.

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