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Charge trapping control in MOS capacitors

M. Dominguez-Pumar, C. Bheesayagari, S. Gorreta, G. Lopez, I. Martin, E. Blokhina, J. Pons-Nin

***Abstract*—This paper presents an active control of C-V characteristic for MOS capacitors based on Sliding Mode control and sigma-delta modulation. The capacitance of the device at a certain voltage is measured periodically and adequate voltage excitations are generated by a feedback loop to place the C-V curve at the desired target position. Experimental results are presented for a n-type c-Si MOS capacitor made with silicon dioxide. It is shown that with this approach it is possible to shift horizontally the C-V curve to the desired operation point. A physical analysis is also presented to explain how the C-V horizontal displacements can be linked to charge trapping in the bulk of the oxide and/or in the interface silicon-oxide. Finally, design criteria are provided for tuning the main parameters of the sliding mode controller.**

***Index Terms*—Sliding Mode Control, MOS capacitors, dielectric charge control**

I. Introduction

Dielectric charge trapping is widely known as an important reliability issue in MOS capacitors and related structures such as ultra-thin gate oxides used in MOSFETs [1], or in MEMS. This phenomenon alters device performance, affecting its circuital features and even reducing its effective lifetime. Shift of the capacitance-voltage (C-V) characteristic [2], [4], and therefore of the threshold voltage, or NBTI degradation observed in p-MOSFETs [5] are examples of serious reliability problems due to oxide charge trapping.

The physical mechanisms responsible for charge trapping are rather complex and dependent on the fabrication process, the temperature and the electrical stress applied to the device [8], [14]–[18]. Most works focus on the design and characterization of materials and structures to reduce the effects of charge trapping. Although these methods have substantially reduced the charge trapping in the dielectrics, shift of the C-V characteristic due to charge trapping still represents a reliability issue in MOS transistors and capacitors. The purpose of this paper is to show how a simple control technique, based on Sliding Control [19], can be used to deliberately shift the C-V characteristic to a desired operation point, either for compensating dielectric charging or for other circuital requirements.

The method is similar to that used in MEMS devices, [19], [20], consisting on the application of bipolar actuation voltage stresses and a sigma-delta modulation control loop. It has been successfully demonstrated in silicon dioxide MOS capacitors.

II. Fabrication process

The capacitors used in the experiments were fabricated on a n-type c-Si <100> wafer, 280 μm thick and resistivity of 2.5$\pm$0.5 Ωcm. The process starts with an RCA clean followed by a thermal oxidation for 30 minutes with a temperature ramp between 850-1080°C. A SiO_2 layer of $\sim$ 40 nm thick is grown on both sides of the wafer. The SiO_2 of the back side is removed with HF etching while the front side is protected with photoresist. To obtain a good ohmic contact at the back surface, a stack consisting of $\sim$4 nm a-SiCx(i) (x$\sim$0.1), 15 nm n-doped a-Si and 35 nm a-SiCx (x$\sim$1) is deposited on the back side of the wafer by PECVD. Then, a laser doping technique, [21], is applied trough this dielectric stack to create localized n^{++} regions with 400 μm pitch. After this laser processing step, the bottom of the sample is ready to be contacted with 480 nm of Ti/Al stack deposited by RF sputtering. A second deposition of Ti/Al is made at the front side to create the upper contact. The active device area is delimited by photolithography patterning and wet etching. A final annealing in N_2 atmosphere at 400ºC for 30 min improves the contacts and the adherence with the c-Si. Figure 1 shows a cross section of the device.

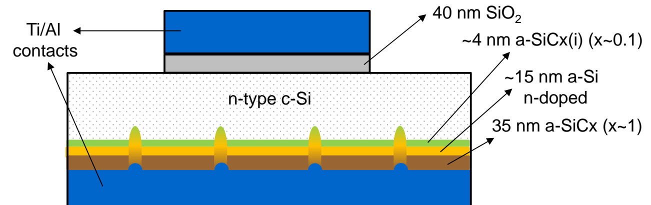

Figure 1. Cross section of the MOS capacitor used in the experiments.

III. Design of the C-V control circuit

The main contribution of this work is to change the paradigm from the observation of charge trapping degradation to a new one deliberately using the trapping phenomena either to mitigate the effect on the device performance or to tailor its operational properties. The mean to do that is to periodically sense the capacitance value at a certain voltage and applying positive or negative voltage pulses to keep constant this value around a target threshold.

The control scheme designed is based on sigma-delta modulation and uses a feedback loop to periodically monitor the displacement of the C-V curve, see Figure 2 (a). It is a sampled circuit and at each sampling period, T_S, it evaluates whether the current value of the magnitude to control is above or below its desired value, hence the sign function in the loop. In our case, the magnitude to control is the total charge in the dielectric, which is indirectly sensed by observing the horizontal displacement of the C-V curve. The detection of whether the C-V lies to the right or to the left of its final desired position can be achieved by observing the value of the capacitance at a constant voltage of interest, $C[V_1]$.

The objective of the control is to shift the C-V curve of the device so that the value of the capacitance at the

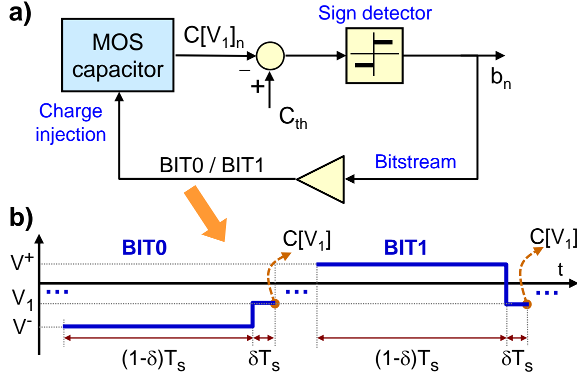

Figure 2. a) Sigma-delta feedback loop for C-V control. The device capacitance is measured periodically at voltage V_1 and compared with a threshold value, C_{th}. Depending on the result, either a BIT1 or BIT0 waveform is applied during the next period. b) BIT0 and BIT1 voltage waveforms. The capacitance measurement is taken at the end of each waveform.

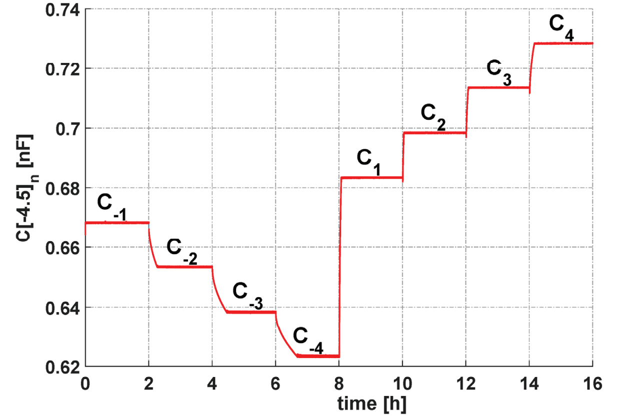

Figure 3. Time evolution of $C[V_1]_n$ during the experiment. For each C_i segment this value is almost constant and matches its corresponding target value, C_{th}. $V_1 = -4.5V$.

voltage reference V_1 is C_{th}, i.e., $C[V_1](t) \approx C_{\text{th}}$. To this effect the feedback loop applies an adequate sequence of voltage waveforms to the device. These waveforms must be designed to obtain two separate results: 1) to allow periodical monitoring of $C[V_1](t)$ at times $t = nT_S$; 2) to apply the correct excitation to shift the C-V in the adequate direction.

The voltage waveforms designed, named as BIT0 and BIT1, can be seen in Figure 2 (b). In both cases the waveform ends with a segment of time of duration δT_S, in which V_1 is applied to the device to be able to measure the relative position of the C-V curve, with regard to the desired position, i.e., make the comparison between $C[V_1]_n = C[V_1](nT_S)$ and C_{th}. On the other hand, the actuation voltages, $\{V^+, V^-\}$, are chosen so that they generate horizontal shifts of the C-V of different sign: if $C[V_1]_n < C_{th}$ a BIT1 is applied during the next clock cycle, and a BIT0 otherwise (see Figure 2).

It must be noted that the application of either a BIT0 or a BIT1 waveform implies the application of two voltages, either $\{V^-, V_1\}$ for BIT0, or $\{V^+, V_1\}$ for BIT1. To be able to control the C-V curve, the continuous application of BIT0 waveforms must generate shifts of different sign to the continuous application of BIT1 waveforms. This has been indeed the case in our experimental results.

Finally, the periodical comparison between $C[V_1]_n$ and C_{th} generates a bitstream at the output of the modulator, $b_n = sgn(C_{\text{th}} - C[V_1]_n)$. From this signal it is possible to obtain real time information of the charging dynamics within the device.

IV. Experimental Results

The control method has been applied to one of the MOS capacitors described in Section II, of 1mm^2 area. It has been observed that continuous application of $V^- = -3V$ generates a shift to the right of the C-V curve, whereas application of $V^+ = 6V$ produces a shift to the left. In order to have good sensitivity to the displacements of the C-V curve produced during the experiments, the value $V_1 = -4.5V$ has been chosen. The sampling period is $T_S = 350$ms and $\delta = 1/3$.

A Keysight E4980A LCR meter (with an AC measuring frequency of 1.99 MHz) controlled from a computer periodically measures the capacitance and sets the actuation voltages. The experiment has been carried out for 16 h with 8 different target capacitances, each one kept for 2 hours (see Table I). Figure 3 shows the evolution as a function of time of the capacitance measured at the end of each clock cycle, $C[V_1]_n$. As it can be observed, the capacitance is almost constant during most part of each interval. At the beginning of each interval a transient can be observed in which the measured capacitance increases or decreases till the next threshold value is reached. Once the

Table I
C_{TH} values used during the experiment. Voltage shifts of the obtained C-V curves measured at $0.4nF$.

Segment name C_i	Time [h]	$C_{\text{th}(i)}\,[nF]$	$V_{\text{sh}}(0.4nF)\ [mV]$
C_0	$t < 0$	–	0 (Initial Value)
C_{-1}	$t \in [0, 2]$	0.668	-36
C_{-2}	$t \in [2, 4]$	0.653	135
C_{-3}	$t \in [4, 6]$	0.638	275
C_{-4}	$t \in [6, 8]$	0.623	384
C_1	$t \in [8, 10]$	0.683	-288
C_2	$t \in [10, 12]$	0.698	-624
C_3	$t \in [12, 14]$	0.7135	-1034
C_4	$t \in [14, 16]$	0.732	—

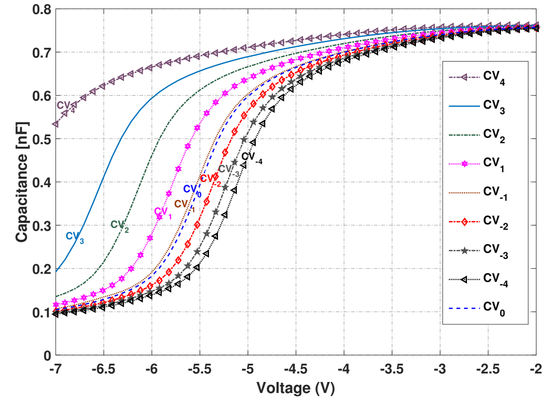

Figure 4. C-V curves obtained at the end of each C_i segment. For each CV_i curve shown, it is $C(-4.5V) \approx C_{\text{th}i}$, as defined in Table I. Within some limits, the control can place the C-V curve arbitrarily at any position.

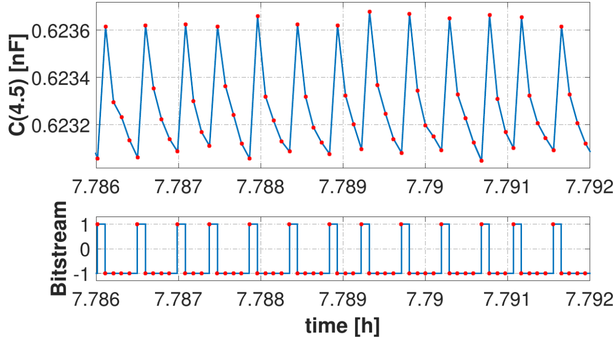

Figure 5. Top: Zoom of $C[V_1](nT_S)$ for a short time within segment C_{-4}. Bottom: sequence of bits applied during this time.

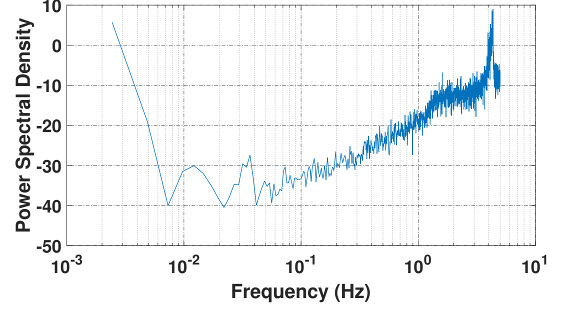

Figure 7. Power spectral density obtained from the C_1 step of the experiment (between t=8h and t=10h). Total number of bits of the sequence: 16312.

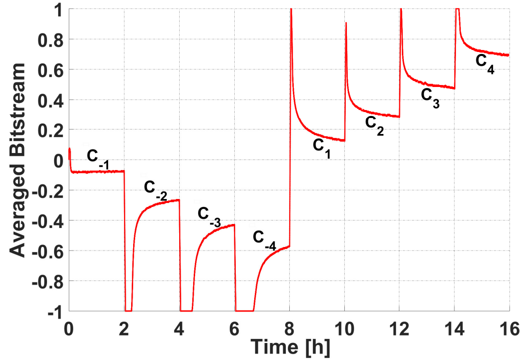

Figure 6. Average bitstream obtained during the experiment. Each time the target capacitance, C_{th}, is changed the bitstream saturates till such target value is reached. Increasing the average number of BIT1 waveforms allows to increase the value $C[V_1]$, hence displacing the C-V to the left.

desired value has been reached, the feedback loop applies the excitation required to keep it constant.

Figure 4 shows the C-V characteristic of the device at the end of each 2-hour controlling segment (C_i). By applying this control method it is possible to shift the C-V curve horizontally. The corresponding values of the voltage shift, measured at 0.4nF of device capacitance, are listed in Table I. A zoom of the time evolution of the capacitance measured at V_1 can be observed in Figure 5. As it can be seen, each time the capacitance is below the desired threshold value (C_{th}=0.6231nF for segment C_{-4}) the feedback loop applies a BIT1, and in this case it takes between 3 and 4 consecutive BIT0s to take it down again below the threshold. This is compatible with the standard behaviour of first-order sigma-delta modulators [20].

Figure 6 shows the average bitstream generated by the feedback loop during the experiment. As it can be observed, for achieving lower C_{th} values it is necessary to inject more BIT0 waveforms (the average bitstream decreases). On the other hand, increasing the average number of BIT1 waveforms generates higher values of $C[V_1]$. Each time a new target value is applied the control saturates (it applies only BIT0 or BIT1 waveforms) till the new C_{th} value is reached. Once in this range, the average bitstream follows a slow time evolution, which has also been observed in previous works [19].

Finally, a distinctive feature of sigma-delta modulators is the power spectrum density of the generated bitstream. For the first order case it is known that the quantization noise presents a zero at 0Hz and the slope is approximately 20dB/dec (see Figure 7).

V. Physical analysis

The objective of this section is to explain the physics underlying the control experiments introduced earlier in the paper. We analyze the dependence of the CV curves on the charge trapped in the dielectric, and on other related factors such as density of interface traps. Open loop measurements will also be shown, in which the displacement of the CV curves can be observed as a function of different open loop actuations using constant voltages.

A. Study of the CV characteristic as a function of charge trapping

In order to check whether the C-V shifts reported in fig. 4 can be related to charges accumulated in the oxide, the experimental results have been compared with simulations performed using a model of the device capacitance. This model includes effects such as charges in the oxide bulk, charge trapping in the SiO_2-Si interface and work function difference between the metal and the semiconductor.

1) Modelling device capacitance: The model has been obtained following the classical theory for Metal-SiO_2-Si structures [6], [8]. The capacitance per unit area of the structure C is a series combination of the oxide layer capacitance C_{ox} and the semiconductor capacitance C_s,

$$C = \frac{C_{ox} C_s}{C_{ox} + C_s} \tag{1}$$

An analytical expression of C_s for uniformly-doped silicon and high frequency (HF) conditions is obtained in Chapter 7 of [8] from the equivalent charge density in the semiconductor Q_s. For n-type silicon the latter is,

$$\begin{aligned} Q_s &= \pm \frac{\sqrt{2}\epsilon_s \epsilon_0}{\beta L_D} \sqrt{\frac{n_i^2}{N_D^2}(e^{-\beta\psi_s} + \beta\psi_s - 1) + e^{\beta\psi_s} - \beta\psi_s - 1} \\ &= \pm \frac{\sqrt{2}\epsilon_s \epsilon_0}{\beta L_D} F(\beta\psi_s, \frac{n_i}{N_D}) \end{aligned} \tag{2}$$

where n_i and ϵ_s is the intrinsic carrier concentration, N_D is the donor concentration, $L_D = \sqrt{\epsilon_s \epsilon_0 / q\beta N_D}$ is the Debye length, $\beta = q/k_B T$ and ψ_s is the potential, or energy band bending, at the silicon surface. The semiconductor capacitance can be obtained as,

$$C_s = \frac{dQ_s}{d\psi_s} = \frac{\epsilon_s \epsilon_0}{\sqrt{2} L_D} \left| \frac{\frac{n_i^2}{N_D^2}(1 - e^{-\beta\psi_s}) + e^{\beta\psi_s} - 1}{F(\beta\psi_s, \frac{n_i}{N_D})} \right| \quad (3)$$

This implies that ψ_s must be calculated first to obtain C_s.

Let us now consider that a voltage bias V is being applied to the device. The voltage drop across the entire structure must be zero,

$$V - \Delta\phi_{ms} - \psi_s - \psi_{ox} = 0 \quad (4)$$

where $\Delta\phi_{ms}$ is the work function difference between the metal and the semiconductor and ψ_s and ψ_{ox} are respectively the potential drops along the semiconductor and along the oxide. ψ_{ox} can be calculated as Q_m / C_{ox}, being Q_m the charge density in the metal layer. Additionally, by charge neutrality Q_m must be equal to the charge at the oxide-semiconductor interface and the charge in the semiconductor Q_s. As discussed later in this section, the charge at the oxide-semiconductor interface can be modelled as $Q_{ox} + Q_{it}$, where Q_{ox} is an equivalent-fixed charge and Q_{it} is the charge due to interface traps. According to all this, charge neutrality leads to,

$$\psi_{ox} = \frac{Q_m}{C_{ox}} = -\frac{Q_{ox}}{C_{ox}} - \frac{Q_{it}(\psi_s)}{C_{ox}} - \frac{Q_s(\psi_s)}{C_{ox}} \quad (5)$$

Note that both Q_{it} and Q_s are functions of the surface potential ψ_s. By substituting (5) into (4), one can obtain

$$V - \Delta\phi_{ms} - \psi_s - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{it}(\psi_s)}{C_{ox}} - \frac{Q_s(\psi_s)}{Cox} = 0 \quad (6)$$

The surface potential ψ_s and therefore the total capacitance of the device $C(V)$ can be calculated by numerically solving equation (6) and then using equations (3) and (1).

2) Modelling oxide charges: Up to four different types of charge can exist in the oxide layer [7]:

- Mobile ionic charge: positive charges in the oxide bulk due to ionic impurities such as Na^+ or K^+.
- Oxide-trapped charge: positive or negative charges due to holes or electrons trapped in the oxide bulk.
- Fixed oxide charge: positive charge due to structural defects closer to the oxide-semiconductor interface.
- Interface-trapped charge: positive or negative charges due to process induced defects, metal impurities and bond-breaking processes (i.e. induced by radiation), located in the oxide-semiconductor interface.

The first three types of charge lead to rigid shift of the C-V curve. In the model used in this work, Q_{ox} summarizes the effect of these charge types, seen as an equivalent charge density in the oxide-semiconductor interface, after integration of the Poisson equation along the oxide layer.

On the other hand, interface traps are electrically connected with the semiconductor and therefore can be charged or not depending on the surface potential ψ_s. Moreover, interface traps can be acceptor-like if they are between the valence band energy E_v and the intrinsic Fermi level E_i, or donor-like from E_i to the conduction band E_c. The simplified model of the interface-trapped charge Q_{it} used in this work assumes that: a) there is a constant trap density D_{it} along the semiconductor gap, b) all trap levels below the Fermi level E_f are full and all above E_f are empty, c) acceptor-like traps are negatively charged for energies between E_f and E_v while donor-like traps between E_f and E_c are positively charged. Under these assumptions, the following expression is obtained,

$$Q_{it}(\psi_s) = D_{it}\left(\beta ln(\frac{n_i}{N_D}) - \psi_s\right) \quad (7)$$

3) Simulations versus experimental data: Fittings of the experimental C-V curves reported in fig. 4 with the analytical model described above have been performed, taking Q_{ox} and D_{it} as parameters. The results are shown in fig. 8. In good agreement with theory, these results indicate that the horizontal-rigid C-V shifts correspond to variations of the charge trapped in the oxide Q_{ox}. Moreover, both the mobile ionic charge and the fixed oxide charge components of Q_{ox} depend on the fabrication process and they can hardly vary during the experiments. Then it can be concluded that such C-V shifts correspond to positive and negative variations of the charge trapped in the bulk of the oxide, being the total oxide charge positive in the cases reported.

Additionally, the charge trapped in the interface Q_{it} can be either positive or negative depending on the surface potential, thus on V. This produces opposite shift in the accumulation and depletion sections within the same C-V curve, a phenomenon known as C-V stretch-out [8]. This phenomenon may explain the CV stretching observed for the CV_4 in Figure 4. In fig. 4 a small discrepancy between simulation and experimental results is seen in the accumulation section. However, this discrepancy is due to the simplified model used, which assumes a constant D_{it}. This is a rough approach, since, in practice, D_{it} can exhibit noticeable variation along the band gap [24].

B. Open loop actuation with constant voltages: observation of C–V transient displacements

The objective now, is to present a first analysis of the dynamics of charge trapping as a function of constant voltage open loop actuations. Figure 9 shows the CV curves obtained at different instants during an experiment made on a pristine device (not previously stressed). In this experiment a sequence of different voltages is applied to the device, while the CV is measured at the time instants on which the actuation voltage is commuted. The sequence of applied voltages and voltage shifts of the CV curves for this experiment can be found in Figure 10. As it can be seen, the experiment begins by applying an increasing sequence of positive voltages, and the CV curve is displaced to the left, indicating an increase of net trapped charge. In a second part of the experiment, a decreasing sequence of negative voltages is applied and the CV curves move the right, indicating a decrease in the net trapped charge.

Figure 11 shows the result of a second experiment performed in another pristine device. In this second case initially

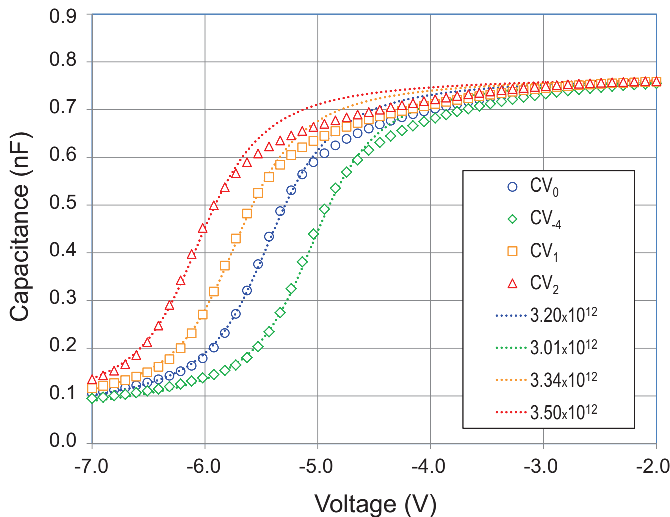

Figure 8. Comparison between experimental C-V curves (ticks) and simulation results of the reference device (dashed lines). The value of Q_{ox} used in each simulation is given in cm^{-2}. An interface trap density D_{it}=1.55×$10^{12}$$cm^{-2}eV^{-1}$ was used in all simulations.

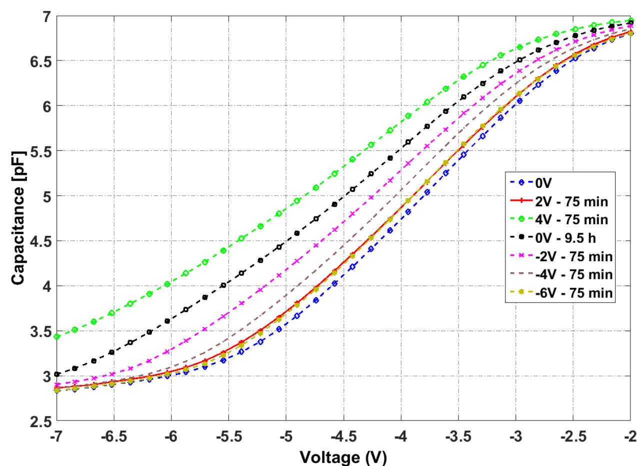

Figure 9. CV characteristics measured in a experiment on which a sequence of different constant voltages were applied during different intervals of time, to a pristine device. The succession of applied voltages is: 0V, 2V, 4V, -2V, -4V and -6V. The time intervals were in all cases 75 minutes. The second time that a 0V was applied the time interval was 9.5h. This is a pristine device (not previously stressed) with an area of 50x50 μm^2.

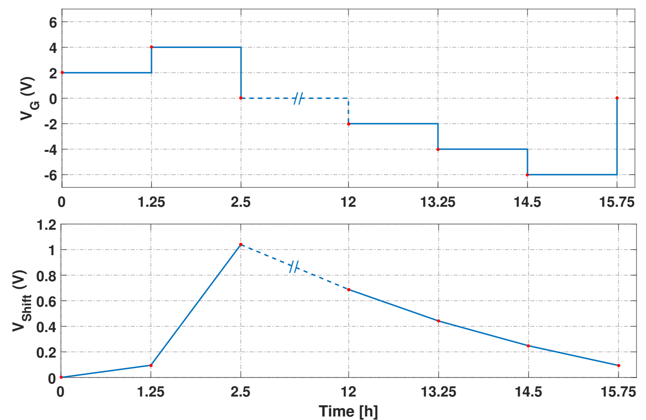

Figure 10. a) Sequence of applied voltages in the experiment of Figure 9, b) voltage shifts of the CV curves during the experiment (measured at 5pF). A positive value of voltage shift implies a shift to the right from the original position (first 0V, pristine condition), i.e., a decrease of net trapped charge.

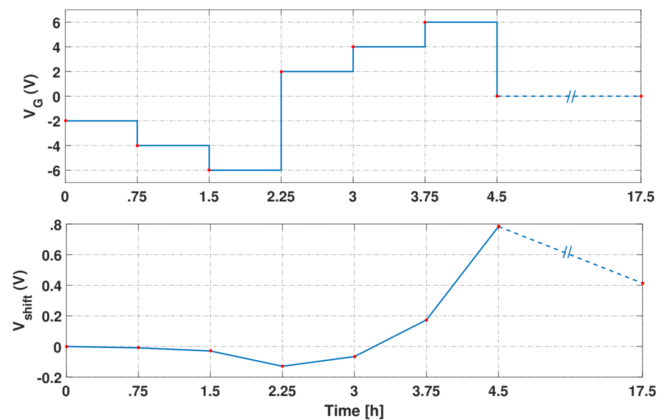

Figure 11. a) Sequence of applied voltages in a second experiment on a pristine device, b) voltage shifts of the CV curves during the experiment (measured at 5pF).

a decreasing sequence of negative voltages is applied, and then an increasing sequence of positive voltages. As it can be observed the application of negative voltage produces displacements to the right (decrease of net trapped charge) while the application of positive voltages generates an increase of the net trapped charge (voltage shift positive).

C. Discussion and design criteria

Charge trapping and de-trapping as well as the conduction processes taking place in the dielectrics are complex. It has been shown that horizontal shifts of the CV curves are attributed to the presence of charge trapping in the bulk of the oxide. The stretching of CV characteristics is associated with different density levels of interface traps in the oxide-silicon interface. This way, it has been possible to obtain a good match between the experimental curves with the curves fitted taking into account this model. The main conclusion is that monitoring of the CV displacement allows to follow the time evolution of the net charge trapped in the bulk of oxide and in the silicon-oxide interface. Finally, the application of voltages of different polarity, at least for those magnitudes that have been measured in this paper, generate either to increase or decrease the net charge in the dielectric.

The essential mechanisms allowing a sliding mode control, or any other type of control, are obviously how sensing and actuation can take place. The main advantage of the sliding mode topology presented in this work is that it is only necessary:

- for sensing: to detect whether the net trapped charge is above or below a certain desired level,
- for actuation: to be able either to increase or decrease the

net trapped charge.

The proposed control will generate the adequate sequence of BIT0/BIT1 symbols so as to make $C[V_1] = C_{th}$. This means that V_1 must be chosen to have enough sensitivity for the detection of CV horizontal shifts. The V^+ and V^- voltages are chosen in a first step by observing the resulting CV shifts in constant voltage open-loop actuations. The fine tuning is achieved by observing the open-loop actuation with BIT0 or BIT1 waveforms. Due to the switching of voltages within each symbol, the real actuation range provided by constant sequences of BIT0 or BIT1 symbols is smaller than the one obtained for constant voltage actuation with V^+ or V^-.

VI. Conclusions

A C-V control for MOS capacitors has been presented. It is based on sigma-delta modulation and allows to position horizontally the C-V characteristic of the device. The control capability relies on the complementary sign of the shift generated by voltages of different polarity, in what is a sliding mode control. Several analysis and measurements have been undertaken in order to know the main conduction mechanisms in the oxide, and how charge trapped can be sensed and actuated. To the knowledge of the authors this is the first time that trapped charge has been controlled in MOS capacitors. This may be seen as new way of improving the reliability of MOS structures.

References

[1] Dimitris P. Ioannou, "HKMG CMOS technology qualification: The PBTI reliability challenge," *Microelectronics Reliability*, Volume 54, Issue 8, August 2014, Pages 1489-1499

[2] Szu-Wei Huang and Jenn-Gwo Hwu, "Lateral nonuniformity of effective oxide charges in MOS capacitors with Al/sub 2/O/sub 3/ gate dielectrics," *IEEE Trans. Electron Devices*, vol. 53, no. 7, pp. 1608–1614, jul 2006. [Online]. Available: http://ieeexplore.ieee.org/document/1643494/

[3] S. Huang and H. J.G., "Lateral Non uniformity of Effective Oxide Charges in MOS Capacitors With Al2O3 Gate Dielectrics," *IEEE Trans. on Electron Devices*, vol. 53, no. 7, pp. 1608–1614, july 2006.

[4] A. Kahraman, E. Yilmaz, S. Kaya, and A. Aktag, "Effects of post deposition annealing, interface states and series resistance on electrical characteristics of HfO2 MOS capacitors," *J. Mater. Sci. Mater. Electron.*, vol. 26, no. 11, pp. 8277–8284, nov 2015.

[5] T. Grasser, B. Kaczer, W. Goes, T. Aichinger, P. Hehenberger, and M. Nelhiebel, "Understanding negative bias temperature instability in the context of hole trapping," *Microelectronic Engineering*, vol. 86, no. 7-9, pp. 1876–1882, july 2009.

[6] R.F. Pierret, *Field Effect Devices: Volume IV*, 2nd ed. MA, USA: Addison-Wesley, 1990.

[7] B.E. Deal, "Standardized Terminology for Oxide Charges Associated with Thermally Oxidized Silicon," *IEEE Trans. on Electron Devices*, vol. 27, no. 3, pp. 606–608, 1980.

[8] S. Sze and K. Ng, *Physics of Semiconductor Devices*, 3rd ed. NJ, USA: Wiley, 2006.

[9] R. Ramprasad, "Phenomenological theory to model leakage currents in metal-insulator-metal capacitor systems," *Phys. Stat. Sol.*, vol. 239, pp. 59–70, 2003.

[10] R. Rodriguez, M. Nafria, J. Sune and X. Aymerich, "Trapped charge distributions in thin (10nm) SiO2 films subjected to static and dynamic stresses," *IEEE. Trans. on Electron Devices*, vol. 45, p. 881, 1998.

[11] J.C. Tseng and J.G. Hwu, "Oxide-Trapped Charges Induced by Electrostatic Discharge Impulse Stress," *IEEE. Trans. on Electron Devices*, vol. 54, p. 1666, 2007.

[12] R. Khosla, P. Kumar and S. Sharma, "Charge trapping and decay mechanism in post deposition annealed Er2O3 capacitros by nanoscropic and macroscopic characterisation," *IEEE. Trans. on Device and Materials Reliability*, vol. 15, p. 610, 2015.

[13] M.S. Rahman and E.K. Evangelou , "Dielectric Relaxation and Charge Trapping Characteristics Study in Germanium Based MOS Devices with HfO2/Dy2O3 Gate Stacks," *IEEE. Trans. on Electron Devices*, vol. 58, p. 3549, 2011.

[14] M. Razeghi, *Fundamentals of Solid State Engineering. Second Edition*. Springer, 2006.

[15] A. Gehring and S. Selberherr, "Modelling of tunnelling current and gate dielectric reliability for non volatile memory devices," *IEEE Trans. on Device and Materials Reliability*, vol. 4, no. 3, pp. 306–319, 2004.

[16] L. Larcher, A. Padovani, V. della Marca, P. Pavan and A. Bertacchini, "Investigation of trapping/detrapping mechanisms in Al2O3 electron/hole traps and their influence on TANOS memory operations," in *VLSI Technology Systems and Applications (VLSI-TSA), Int. Symp. on*, April 2010, pp. 52–53.

[17] T. Grasser, B. Kaczer, W. Goes, H. Reisinger, T. Aichinger, P. Hehenberger, P. J. Wagner, F. Schanovsky, J. Franco, M. T. Luque and M. Nelhiebel, "The paradigm shift in understanding the bias temperature instability: From reaction-diffusion to switching oxide traps," *IEEE Trans. on Electron Devices*, vol. 58, no. 11, pp. 3652–3666, Nov 2011.

[18] A. A. Boo, Z. Y. Tung and D. S. Ang, "New Observations on the Correlation Between Hole-Trapping Transformation and SILC Generation Under NBTI Stressing," *IEEE Electron Device Letters*, vol. 37, no. 4, pp. 369–372, April 2016.

[19] M. Dominguez-Pumar, S. Gorreta and J. Pons-Nin, "Sliding Mode Analysis of the Dynamics of Sigma-Delta Controls of Dielectric Charging," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2320–2329, 2016.

[20] S. Gorreta, J. Pons-Nin, E. Blokhina, O. Feely and M. Dominguez-Pumar, "Delta-Sigma Control of Dielectric Charge for Contactless Capacitive MEMS," *Microelectromechanical Syst. J.*, vol. 23, no. 4, pp. 829–841, 2014.

[21] I. Martín, M. Colina, A. Coll, G. López, P. Ortega, A. Orpella and R. Alcubilla, "c-Si Solar Cells based on Laser-processed Dielectric Films," *Energy Procedia*, vol. 55, pp. 255–264, 2014.

[22] W. Harrell and J. Frey, "Observation of Poole–Frenkel effect saturation in SiO2 and other insulating films," *Thin Solid Films*, vol. 352, no. 1-2, pp. 195–204, 1999.

[23] Y. Seo, S. Lee, I. An, C. Song, and H. Jeong, "Conduction mechanism of leakage current due to the traps in ZrO 2 thin film," *Semicond. Sci. Technol.*, vol. 24, no. 11, p. 115016, 2009.

[24] Takashi Hori, *Gate Dielectrics and MOS ULSIs - Principles, Technologies and Applications*. Heidelberg, Germany: Springer-Verlag, 1997.