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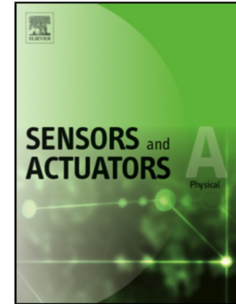

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MOSFET dynamic thermal sensor for IC testing applications

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HIGHLIGHTS:

-A single MOSFET can be employed as a thermal sensor to measure on-chip dynamic thermal signals caused by a power-dissipating CUT.

-The measurement depends on the thermal properties of the substrate, the CUT-sensor distance, and the electrical properties of MOSFET sensor.

-Thermal simulations in COMSOL and experimental results from a chip fabricated in 0.35 μm CMOS technology are provided.

-The proposed thermal sensor is applied to estimate the linearity of an RF amplifier.

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Abstract— This paper analyses how a single metal-oxide-semiconductor field-effect transistor (MOSFET) can be employed as a thermal sensor to measure on-chip dynamic thermal signals caused by a power-dissipating circuit under test (CUT). The measurement is subjected to two low-pass filters (LPF). The first LPF depends on the thermal properties of the heat-conduction medium (i.e. silicon) and the CUT-sensor distance, whereas the second depends on the electrical properties of the sensing circuit such as the bias current and the dimensions of the MOSFET sensor. This is evaluated along the paper through theoretical models, simulations, and experimental data resulting from a chip fabricated in 0.35 µm CMOS technology. Finally, the proposed thermal sensor and the knowledge extracted from this paper are applied to estimate the linearity of a radio-frequency (RF) amplifier.

Keywords: IC testing; MOSFET; RF testing; temperature sensor; thermal coupling; thermal testing.

1. INTRODUCTION

Among many other applications [1], integrated thermal sensors are employed as built-in testers (BIT) of other blocks (so-called CUT) embedded into the same integrated circuit (IC). The thermal sensor is placed near the CUT so that they are thermally coupled through the semiconductor substrate and then it measures on-chip thermal variations caused by the power dissipated by the CUT. These thermal measurements can be used to detect failure or hot-spots in digital ICs [2,3] and in operational amplifiers [4], and to extract figures of merit, such as the centre frequency or the 1-dB compression point (CP), of analogue RF-ICs [5,6]. The main advantage of employing thermal sensors, instead of electrical sensors [7,8], in RF-IC testing is that no node of the CUT is electrically loaded by the BIT. Thermal measurements can also be performed using off-chip optical instrumentation, such as an infrared-radiation (IR) camera,

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that access to the die through its upper, back or lateral sides [9,10]. These off-chip techniques are less attractive in terms of cost and integration, but they do not suffer from CUT-sensor electrical coupling.

The simplest on-chip thermal sensor that can be used in BIT applications is a diode-connected transistor, with either a bipolar junction transistor (BJT) [11,12] or a MOSFET [13]. The higher accuracy provided by BJT-based sensors is not a key element for the selection of the sensing transistor since the magnitude of interest here is the change of temperature caused by CUT and not the absolute value of temperature. The comparative analysis reported in [14,15], which was carried out through static on-chip thermal measurements, shows that MOSFET-based sensors offer the following advantages: (i) fully compatibility with the fabrication process, (ii) more sensitivity (especially, in strong inversion [14]) to on-chip thermal variations caused by the CUT, and (iii) less layout area required around the CUT, which is crucial for BIT applications because a small sensor can be easily fit in the empty areas with minimum impact on the IC design. Note that the layout of the CUT should not be re-designed as a consequence of placing the thermal sensor because this is a time-consuming task, especially when designing RF circuits that are so sensitive to layout parasitic components. In that sense, the sensor is expected to be placed in empty areas around the CUT and, hence, we can have a certain distance between the power-dissipating device of the CUT and the sensor.

Some BIT applications involve dynamic thermal measurements, i.e. the sensor has to measure an on-chip AC thermal signal whose amplitude (and/or phase) has information about the CUT performance. For instance, when RF-ICs are thermally tested using the heterodyne technique (which will be explained later in Section 5), the information about the performance at high frequency is embedded into a low-frequency (e.g. 1 kHz) on-chip thermal signal [5, 6]. In the literature, we can find other applications interested in measuring the amplitude and phase shift of AC thermal signals, for example: the determination of thermal properties of

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fluids [16] and the monitoring of biofilm dynamics [17]. In those examples, however, the heater and the sensor are not thermally coupled through the silicon substrate but through the fluid or biofilm under test. In any of these applications involving AC thermal measurements, both the frequency of the AC thermal signal and the distance between the CUT (or heater) and the sensor play a significant role in the thermal coupling [18]. This was also reported for BJT-based thermal sensors fabricated on a silicon-on-insulator substrate [19], which involves a lower heat spreading due to the lower thermal conductivity of glass.

With the final aim of using a single MOSFET to measure on-chip AC thermal signals resulting from the heterodyne test of RF circuits, this paper analyses the main parameters (i.e. operating frequency, CUT-sensor distance, dimensions and bias of the MOSFET sensor) affecting the measurement. Knowledge about the effects of distance and frequency on the dynamic thermal measurements is essential to decide the right placement of the MOSFET sensor around the CUT and the appropriate operating frequency. This is evaluated theoretically in Section 2, through thermal simulations in Section 3, and experimentally in Section 4. Finally, the concept is applied to characterise an RF power amplifier (PA) in Section 5 and the advantages of the proposed technique are discussed in Section 6.

2. THEORETICAL MODELS

2.1. On-chip thermal oscillation

The heat dissipated by the CUT, which is here a harmonic function of frequency f, is mainly transferred by conduction through the substrate towards the bottom, thus generating a gradient of temperatures in its neighbourhood. This thermal variation is then monitored by a thermal sensor that is located at a distance d from the CUT. This scenario can be treated, in a first approximation and whenever the thermal penetration depth (δ_p) is smaller than the substrate thickness, as a semi-spherical heat source in a semi-infinite homogeneous medium with concentric semi-spherical isothermal surfaces, as shown in Fig. 1. Two remarks about

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Fig. 1: (a) the thermal sensor is assumed to be small and made of silicon and, therefore, the medium can be considered homogeneous in spite of the presence of the sensor, and (b) the adiabatic boundary condition considered on top takes into account that the additional layers of the backend part (such as silicon dioxide and polyamide) have a low thermal conductivity. In that scenario, the amplitude and phase shift of the thermal oscillation (T) can be expressed, using phasor notation, as [20]

$$T(d,f)=\frac{C}{d}e^{-d/\delta_{\mathrm{p}}}e^{-jd/\delta_{\mathrm{p}}}, \tag{1}$$

where C is a constant and δ_{p} depends on f as

$$\delta_{\mathrm{p}}=\sqrt{\frac{D}{\pi f}}, \tag{2}$$

D being the thermal diffusivity of the medium (i.e. $90\cdot10^{-6}$ m^2/s for silicon).

Equation (1) shows that the amplitude (A) of the on-chip thermal oscillation generated by the CUT depends on both d and f. Using as a reference the value of amplitude (A_0) obtained at a distance d_0 and at a frequency f_0 (and, hence, at a penetration depth $\delta_{\mathrm{p},0}$), the amplitude can be normalised and simplified (assuming as $\delta_{\mathrm{p},0} >> d_0$) as

$$A_{\mathrm{norm}}(d,f)=\frac{A}{A_0}=\frac{d_0}{d}e^{d_0/\delta_{\mathrm{p},0}-d/\delta_{\mathrm{p}}}\approx\frac{d_0}{d}e^{-d/\delta_{\mathrm{p}}}. \tag{3}$$

At low frequencies (i.e. when $\delta_{\mathrm{p}} >> d$), A_{norm} can be approximated as $A_{\mathrm{norm,LF}} \approx d_0/d$ and, hence, it can be considered independent of f. However, at high frequencies (i.e. when δ_{p} and d are comparable), A_{norm} decreases with increasing f due to the attenuation caused by the exponential term in (3). Therefore, the measurement is subjected to a "thermal" LPF with the following 3-dB cut-off frequency:

$$f_{\mathrm{c,t}}=\frac{0.12D}{\pi d^2}. \tag{4}$$

Note that if an increase of d decreases $A_{\mathrm{norm,LF}}$ by a factor K, then $f_{\mathrm{c,t}}$ also decreases but by a factor K^2. In the next sections, we assume $d \geq 20$ µm, which fixes $f_{\mathrm{c,t}} \leq 9$ kHz.

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For BIT applications, the thermal sensor should be placed as close as possible to the CUT in order to enhance the thermal coupling, but with minimum impact on its layout (for instance, using empty areas around the CUT). In that sense, we can have a certain distance between the power-dissipating device of the CUT and the sensor. Once d is known, the operating frequency (i.e. Δf in the heterodyne technique explained in Section 5) should be selected to be lower than $f_{c,t}$ at that d. However, if the value of d is very small (say, a few microns), it is advisable to operate at $f \ll f_{c,t}$ so as to reduce the CUT-sensor capacitive electrical coupling, which behaves as a high-pass filter.

2.2. Dynamic thermal sensor

As a thermal sensor, we propose to use a diode-connected n-type MOSFET operating in strong inversion and biased with a DC current source (I_B), as shown in Fig. 2a. Assuming the temperature dependence of both the carriers mobility and the threshold voltage of the MOSFET, the output voltage (v_{out}) of the circuit in Fig. 2a linearly depends on temperature with the following sensitivity [14]:

$$S_T = \beta - \frac{\alpha}{2}\frac{1}{T_0}\sqrt{\frac{2I_B}{\mu_0 C_{ox}\frac{W}{L}}}, \qquad (5)$$

where β is the temperature coefficient of the threshold voltage, α is the exponent of the temperature dependence of the mobility, T_0 is a reference temperature, μ_0 is the carriers mobility at T_0, C_{ox} is the gate oxide capacitance per unit area, and W and L are the width and length of the MOSFET channel, respectively. Since $\alpha < 0$ and $\beta < 0$ [21], we can achieve a high (positive) sensitivity using a high value of I_B and/or a low value of W/L; note, however, that the sensor area (and, hence, W and L) can be determined by the available layout area around the CUT. Values of S_T up to +6.6 mV/K, which is three times higher than in BJT-based sensors, were reported in [14] for static on-chip thermal measurements. For the previous discussion, we have assumed that I_B is far from the CUT and, therefore, it is not

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affected by the dissipated power. Changes of ambient temperature affecting I_B are not expected to be critical whenever these are slower than the IC test.

When the circuit in Fig. 2a is subjected to on-chip thermal oscillations at f, the MOSFET carries out a small-signal temperature-to-voltage conversion at f. This conversion is done around a DC operating point that can be quite susceptible to process variations, but this is not a major concern here since the information is embedded into the small signal at f. The circuit in Fig. 2a can be modelled by the small-signal equivalent circuit shown in Fig. 2b that includes an AC voltage source, an output resistance (r_{out}) and an output capacitance (c_{out}). The amplitude of voltage source depends on S_T and, hence, on I_B and W/L. The output resistance can be approximated to g_m^{-1} [22], where g_m ($=\sqrt{2\mu_0 C_{ox} I_B W/L}$) is the transconductance of the MOSFET, whereas the output capacitance includes the contributions of the MOSFET itself, the current source, the input/output pad, and the off-chip readout electronics. According to Fig. 2b, the measurement is subjected to an electrical LPF with the following 3-dB cut-off frequency:

$$f_{c,e} = \frac{1}{2\pi r_{out} c_{out}}. \quad (6)$$

Simulations in Cadence-Spectre showed that $r_{out} < 100$ kΩ for the MOSFETs under test. Therefore, considering $c_{out} = 10$ pF, we have $f_{c,e} > 160$ kHz, which is much higher than the value of $f_{c,t}$ estimated in Section 2.1. Consequently, the thermal LPF behaviour is expected to dominate over the electrical one.

In comparison with the dynamic thermal sensor suggested in [5], which relies on a differential configuration of two sensing devices implemented with parasitic BJTs, the MOSFET sensor proposed in Fig. 2a occupies less layout area (say, ten times less), which facilitates its integration around the CUT. Moreover, the sensing circuit shown in Fig. 2a does not need any preliminary calibration, as it happens in [5] to adjust the mismatch between the two sensing devices that brings the amplifier output to saturation [6]. On the other hand, in

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comparison with the sensor suggested in [17] that relies on a thin-film germanium thermistor, the required area of the MOSFET sensor in Fig. 2a is also much smaller (more than a hundred times). Furthermore, the thermistor proposed in [17] is not located at the CUT level (i.e. top of the substrate) but at the backend part and, therefore, the scenario shown in Fig. 1 would not be valid.

3. THERMAL SIMULATIONS

The effects of both frequency and distance on the CUT-sensor thermal coupling have been simulated in a 3D structure using the heat-transfer module in COMSOL Multiphysics. The geometry considered in the simulations, which agrees with that of the chip fabricated and tested in Section 4, is represented in Fig. 3. The CUT is emulated by a heater dissipating a sine-wave power signal of frequency f and amplitude P_p, whereas the sensor is replaced by a testing point placed at a distance d from the centre of the heater. The boundary conditions assumed are: (a) isothermal (20ºC) at the bottom surface, which takes into account that this surface will be in contact with a high-conductivity large-area metal; and (b) adiabatic at the lateral and top surfaces, which considers that the heat will be mainly transferred by conduction through the silicon substrate towards the bottom [23]. The frequencies simulated are from 100 Hz to 200 kHz and, hence, the values of δ_p calculated by (2) are from 12 μm to 535 μm. Because the maximum value of δ_p is smaller than the thickness of the silicon substrate, the results of the simulations can be considered quite independent of the boundary condition assumed at the bottom surface [24].

The frequency response of the thermal amplitude at different values of d (from 20 μm to 100 μm) and for P_p = 5.5 mW (which is the value applied later in the experiments) is shown in Fig. 4a. We can observe an LPF behaviour with a low-frequency amplitude (A_{LF}) that is inversely proportional to d, as predicted by (3). Furthermore, the higher d, the lower $f_{c,t}$, as suggested by (4). For example, we have A_{LF} = 222 mK and $f_{c,t} \approx$ 10 kHz at d = 20 μm, but

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A_{LF} = 35 mK and $f_{c,t}$ ≈ 600 Hz at d = 100 µm. For comparison purposes, the simulation results in Fig. 4a are normalised to the value obtained at d_0 = 20 µm and f_0 = 100 Hz and represented in Fig. 4b together with the theoretical results calculated from (3). The agreement between simulation and theoretical data is remarkable.

Simulation results also show that the on-chip thermal map clearly depends on the frequency of the dissipated power. As an example, Fig. 5 represents the plan view (at the heater depth) of the isothermal lines when the frequency is (a) 100 Hz, (b) 1 kHz and (c) 10 kHz. Note that an increase of frequency causes a higher confinement of the thermal energy around the heater and, therefore, a lower thermal amplitude at a certain distance from the heater.

4. EXPERIMENTAL RESULTS

A chip including heaters (that emulate the CUT) and thermal sensors was implemented in 0.35 µm CMOS technology of AMS (AustriaMicroSystems), and then tested using the experimental setup shown in Fig. 6. A signal generator providing a sinusoidal voltage with a frequency f (from 100 Hz to 200 kHz, as in Section 3), an amplitude (A_h) of 0.2 V and a DC level (V_{dc}) of 1.2 V was used to excite the heater. With this excitation, the heater (which was a diode-connected MOSFET with W_h= 450 µm and L_h= 1 µm) dissipated 5.5 mW at f according to simulations in Cadence-Spectre of the extracted view. This power generated an on-chip thermal signal at f that was converted into a voltage signal through the MOSFET thermal sensor shown in Fig. 2a. The sensor was placed at different d (20 µm and 35 µm), was biased at different I_B (10 µA, 20 µA and 40 µA) and had different W/L ratios (1/1, 1/4, 1/16 that correspond to transistors named M1, M2 and M3, respectively). The amplitude (A_s) of the sensor output voltage at f was then measured by a lock-in amplifier (Signal Recovery 7265). The setup also had an IR-camera (FLIR SC5500) with a lock-in processing module [10] that was used to validate the on-chip sensor measurements in the frequency range from 100 Hz to 2 kHz.

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The experimental frequency response (for M2 with I_B = 40 µA and S_T = 4.2 mV/K [14]) of the thermal amplitude at different values of d is shown in Fig. 7 (in dashed line). We can observe again that the higher d, the lower both the amplitude at low frequency and the bandwidth. For comparison purposes, Fig. 7 also includes the simulation results (in continuous line) represented before in Fig. 4a, which are qualitatively similar to the experimental data. Moreover, in Fig. 7 we also have the measurements carried out with the IR camera (in black dashed line), which fairly agree with the MOSFET measurements in the operating frequency range of the camera

The effects of I_B on the frequency response of the output voltage of M2 (at 35 µm) are represented in Fig. 8, which clearly shows, besides the LPF behaviour, that the amplitude increases as I_B increases, as predicted by (5). On the other hand, Fig. 9 shows the effects of W/L on the frequency response when d = 35 µm and I_B = 10 µA. Now, the amplitude increases as W/L decreases, as also predicted by (5). The flat frequency response of M1 in Fig. 9 is due to a thermal insensitivity caused by a mutual compensation of mobility and threshold voltage thermal effects [25]. Therefore, according to Figs. 8 and 9, the rules for increasing the thermal sensitivity of MOSFETs in dynamic measurements are the same as in static measurements, i.e. high bias current and low W/L ratio. The experimental tests in Figs. 8 and 9 were carried out in the frequency range from 100 Hz to 10 kHz since the signal amplitude was really low after 10 kHz (see Fig. 7).

5. APPLICATION TO IC TESTING

The CUT selected to prove the feasibility of the proposed thermal sensor is a class-A RF-PA with a cascode stage, as shown in Fig. 10a, and with a central frequency of 440 MHz. A microphotograph of the layout of the RF-PA, which was embedded into the same chip indicated in Section 4, is shown in Fig. 10b. The cascode transistor (M_2 in Fig. 10a), which was implemented by three transistors ($M_{2,a}$, $M_{2,b}$ and $M_{2,c}$) connected in parallel, was

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considered as the power-dissipating device of the CUT. The MOSFET thermal sensor (with $W/L = 1.5/24$ and $I_B = 20$ µA) was placed between $M_{2,a}$ and $M_{2,b}$, as shown in Fig. 10b; the distance between the centre of $M_{2,a}$ (or $M_{2,b}$) and the centre of the thermal sensor was around 20 µm. The layout area of the MOSFET sensor was a thousand times smaller than that of the RF-PA, excluding the PAD area.

The figure of merit extracted from the RF-PA shown in Fig. 10a was the 1-dB CP, which is defined as the input power that provides an output power that is 1 dBm smaller than that expected in an ideal linear amplifier [26]. The estimation of the 1-dB CP using thermal measurements relies on the fact that the relation between the power dissipated (and, hence, the thermal variation) and the input power is linear while the RF-PA operates in its linear range, but it follows a non-linear behaviour when the RF-PA reaches saturation [5]. In other words, when a saturation phenomenon occurs in the electrical behaviour of a CUT, the same is observed in its dissipated power and then this is reflected in the thermal field.

The linearity of the RF-PA was first tested using RF instrumentation. The output power (P_{out}) was measured at different input power levels (P_{in}) while keeping the frequency constant (i.e. 440 MHz). The results are represented in Fig. 11a, where we can observe that the relation between P_{out} and P_{in} is linear (i.e. slope of one on a log-log scale) at low levels of P_{in}, but it becomes nonlinear at high levels. The 1-dB CP was found at −2.5 dBm.

The same RF-PA was then thermally tested using the MOSFET dynamic thermal sensor proposed in Fig. 2a and the heterodyne technique. This technique relies on applying two tones (f_1 and f_2) of high frequency to the input, with Δf ($= f_2 - f_1$) being much smaller than f_1 and f_2. Then, as a consequence of the frequency mixing generated by Joule effect, the RF-PA dissipates power (and, hence, generates an on-chip thermal signal) at the beating frequency (i.e. at Δf) with information about the performance at high frequency [5]; other spectral components of the dissipated power (such as those at f_1, f_2, $f_1 + f_2$,…) are filtered out by the thermal LPF behaviour shown in Fig. 4. This on-chip thermal signal at Δf was monitored by

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the MOSFET sensor in Fig. 2a. The amplitude (A_s) of v_{out} at Δf was measured at different P_{in} levels while keeping f_1 (= 440 MHz – $\Delta f/2$) and f_2 (= 440 MHz + $\Delta f/2$) constant. The results are shown in Fig. 11b for two values of Δf (1013 Hz and 10013 Hz), with a higher amplitude at Δf = 1013 Hz due to the thermal LPF. Similarly to Fig. 11a, the relation between A_s and P_{in} was linear (i.e. again a slope of one) at low levels of P_{in}, but it was not at high levels. The 1-dB CP can be here estimated as the input power that provides an output voltage that is 1 dBmV smaller than that obtained in an ideal linear amplifier. Thus, the 1-dB CP was −2.4 dBm for Δf = 1013 Hz, and −2.8 dBm for Δf = 10013 Hz, which are very similar to the value obtained before using RF instrumentation.

6. DISCUSSION

According to the experimental results explained in Section 5, the use of a single MOSFET as a dynamic thermal sensor to extract electrical information about a CUT seems feasible. If that thermal sensor is employed together with the heterodyne technique to test RF-CUTs, we have the following main advantages:

- Since thermal measurements are non-invasive and do not electrically load any node of the CUT, the presence of the thermal sensor do no alter the electrical performance of the CUT. Moreover, we do not need a simultaneous co-design of the CUT and the sensor, as it happens in conventional BIT strategies based on electrical sensors.
- Thanks to the application of the heterodyne technique, the sensing circuit operates at low frequency regardless of the operating frequency of the CUT. Actually, an amplifier operating at higher frequencies (e.g. in the millimetre wave band) could be characterised using the same sensing circuit and without any change in the measurement method.
- The MOSFET thermal sensor is fully compatible with the fabrication process and requires a small layout area. Therefore, it can be placed in empty areas around the CUT with minimum impact on the IC design.

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- Because there is no loading effect and the area overhead is minimum, different thermal sensors can be employed to individually characterise each of the blocks of a RF system-on-chip (e.g. low-noise amplifier, mixer, local oscillator, power amplifier, etc.). Furthermore, thanks to the thermal LPF behaviour explained in Section 2.1, those tests can de done simultaneously without affecting each other whenever these blocks are separated enough and the operating frequency is high enough.
- Unlike off-chip measurement methods (either electrical or thermal), the proposed on-chip technique not only can be used for pass/fail screening in a low-cost high-volume manufacturing test environment, but also for on-line monitoring of parameter drifts during normal operation of the IC.

7. CONCLUSIONS

This paper has shown that a single MOSFET can be employed to measure on-chip thermals oscillations at f generated by a power-dissipating CUT, with the final aim of extracting electrical information about the CUT. The theoretical models, simulations and experimental results reported along the paper have provided guidelines to improve (a) the CUT-sensor thermal coupling by an appropriate selection of the CUT-sensor distance and the operating frequency, and (b) the temperature-to-voltage conversion at f by a correct selection of the bias current and the dimensions of the MOSFET sensor. These concepts have been then proved by testing the linearity of a RF-PA. The 1-dB CP estimated using the MOSFET dynamic thermal sensor had an error of 0.1 dBm when Δf = 1013 Hz. We believe this is a promising IC testing technique since it is non-invasive and low cost, and its impact on the IC layout design is minimum.

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Figure 11. Experimental results of the linearity test of the RF-PA using (a) RF instrumentation and (b) the MOSFET thermal sensor shown in Fig. 2a.

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Figure 1

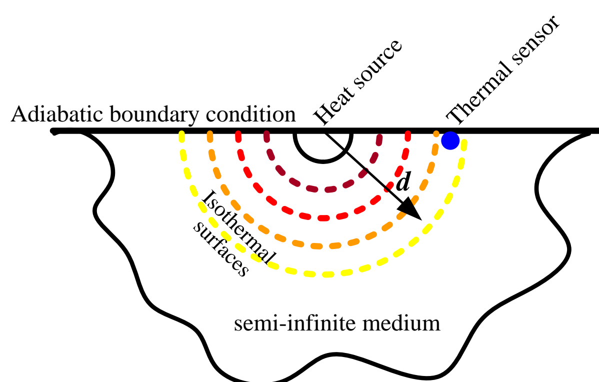

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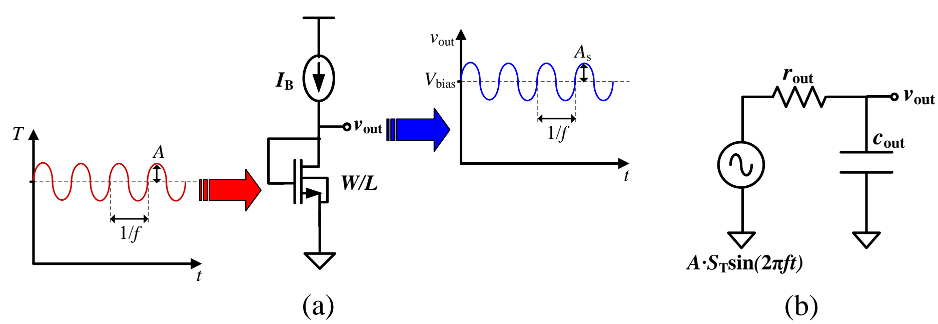
Figure 2



(a) (b)

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Figure 3

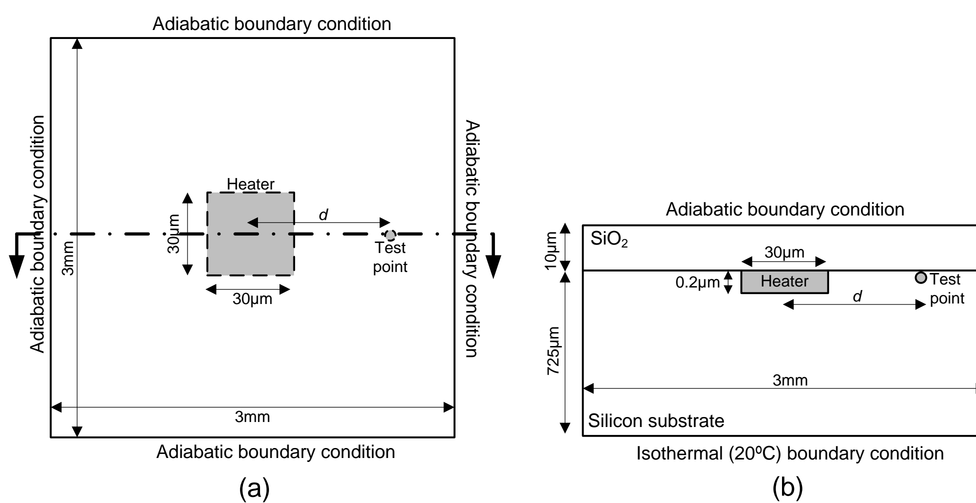

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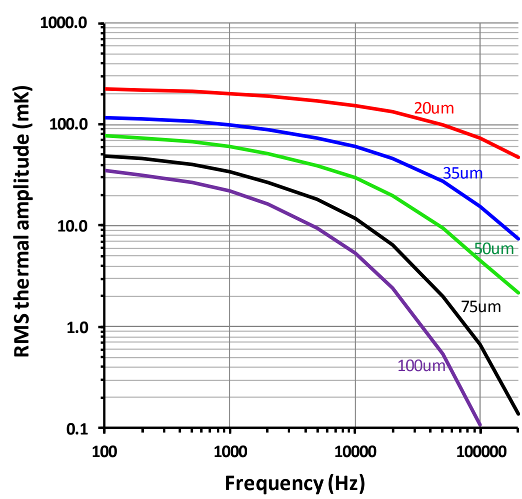
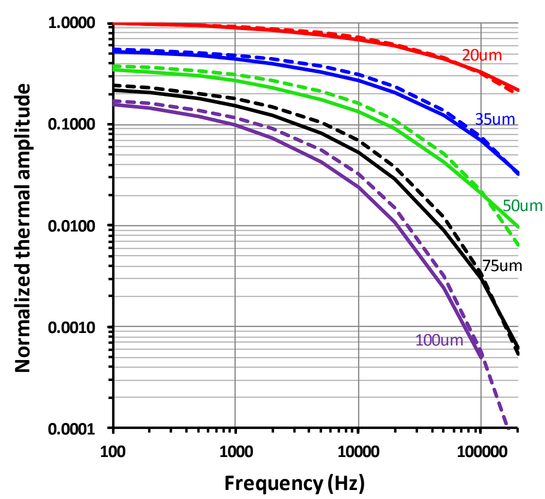
Figure 4



(a)



(b)

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Figure 5

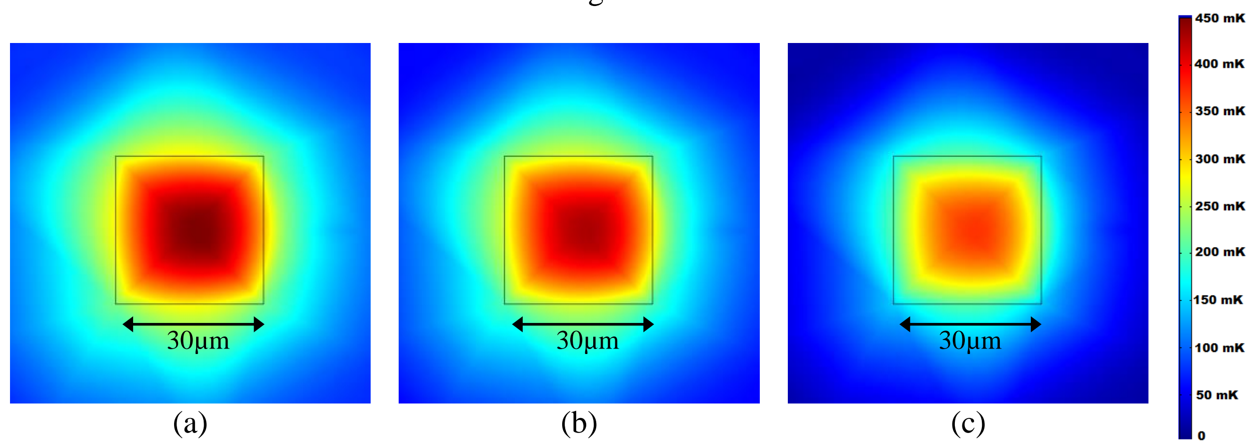

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Figure 6

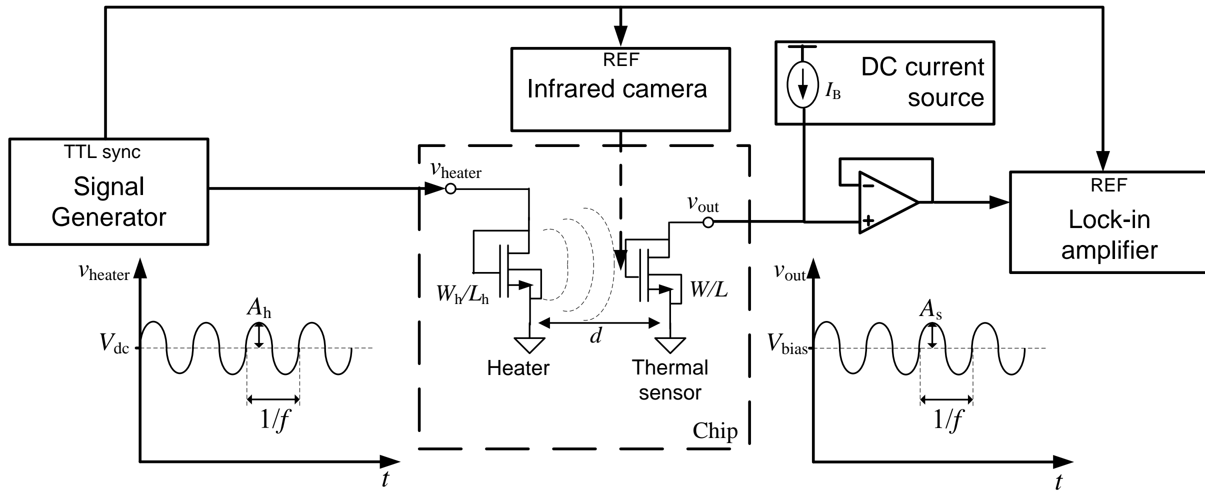

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Figure 7

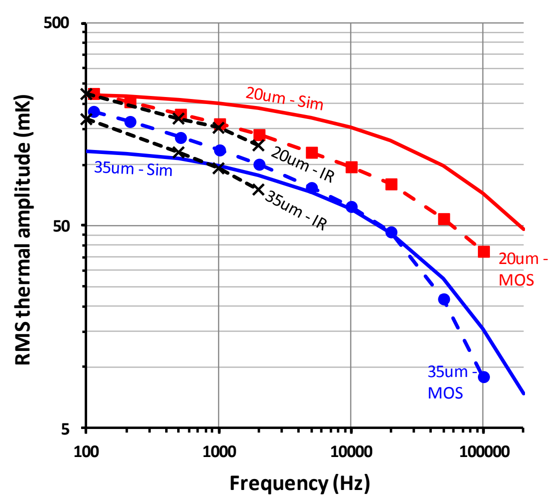

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Figure 8

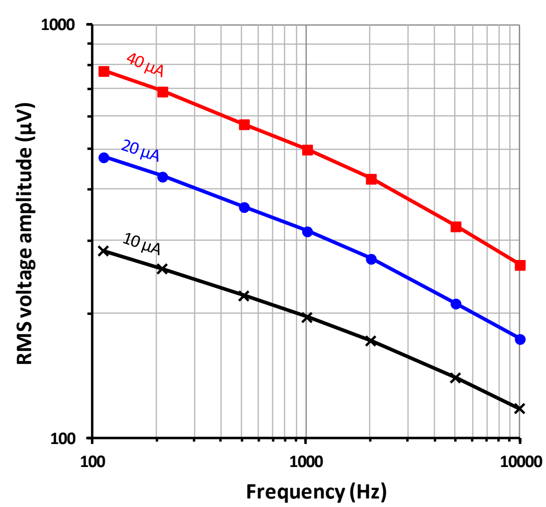

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Figure 9

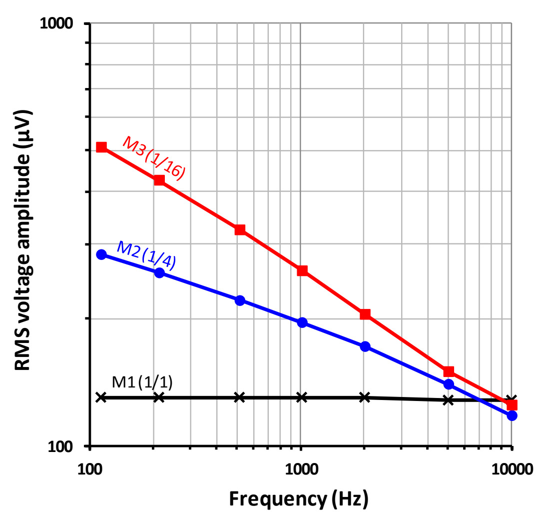

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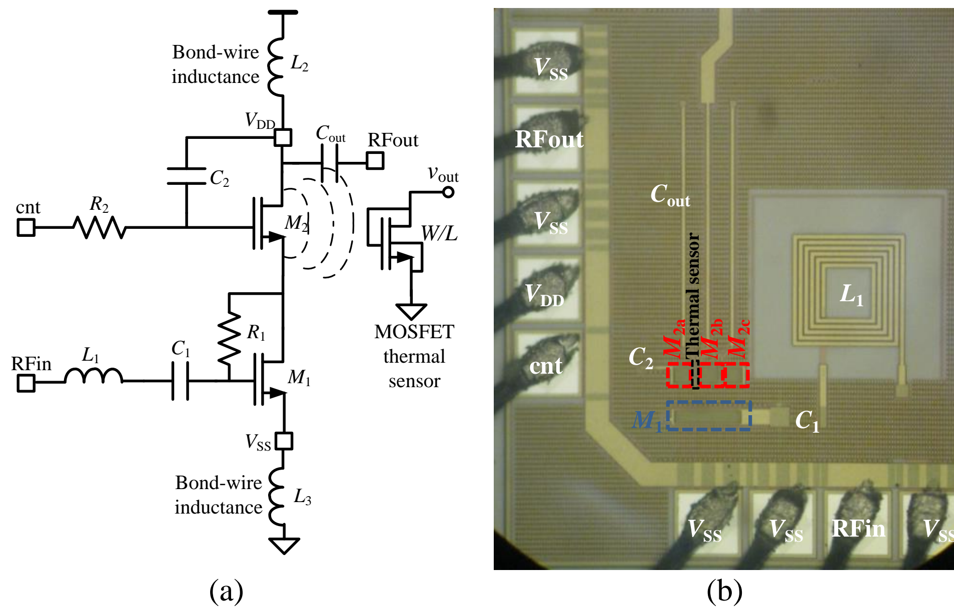
Figure 10



(a) (b)

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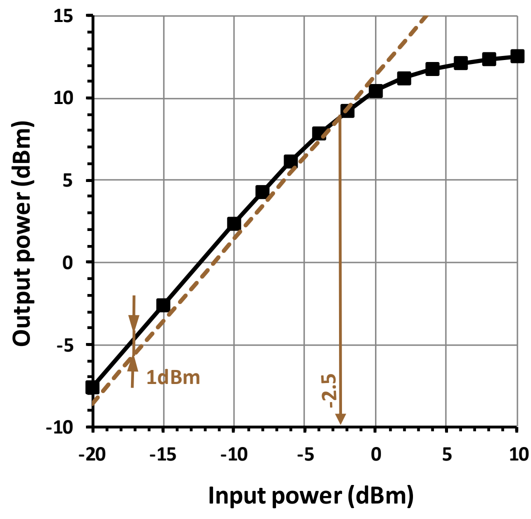
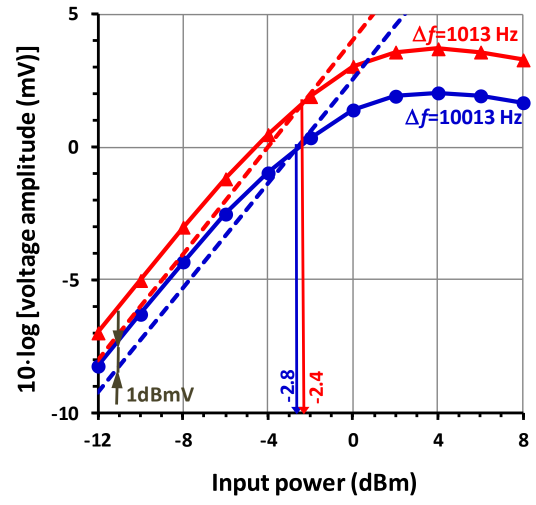
Figure 11



(a)



(b)