Supply Modulator for Linear Wideband RF Power Amplifiers

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Resumen
Este artículo trata de las técnicas de diseño de reguladores de potencia conmutados de alta eficiencia destinados a alimentar amplificadores de potencia (PAs) lineales, empleando técnicas de seguimiento para estándares inalámbricos de banda ancha. Los cuellos de botella presentados implican un compromiso entre tensión, *slew rate* y ancho de banda. De hecho, la limitación de *slew rate* es identificada como el principal desafío. Por tanto, se propone una técnica de mejora del *slew rate* denominada "bang-bang". Este enfoque permite el uso de moduladores de alimentación eficientes para la alimentación de los mencionado amplificadores de potencia de banda ancha. El esquema propuesto no degrada significativamente la eficiencia del PA y preserva, e incluso mejora, la estabilidad del regulador conmutado. El prototipo ha sido implementada utilizando la tecnología de TSMC 0,18 µ*m*. Resultados de simulación post-layout en Cadence® son presentados para demostrar la viabilidad del diseño llevado a cabo.

Palabras Clave: Reguladores DC/DC conmutados de alta eficiencia, moduladores de alimentación, amplificadores de potencia lineales de banda ancha, técnicas de seguimiento de envolvente, estándares inalámbricos para banda ancha, controlador '*bang-bang*', técnicas de mejora del *slew rate*.

Abstract
This paper deals with the design techniques of power efficient switching regulators intended for linear power amplifiers (PAs) employing envelope tracking techniques in wideband wireless standards. The bottlenecks involve a tradeoff between ripple voltage, slew rate and bandwidth. The slew rate limitation is identified as the main challenge; thus a 'bang-bang' slew-enhancement technique is proposed. This approach enables the use of efficient supply modulators in wideband power amplifiers. The proposed scheme does not significantly degrade PA efficiency and preserves, and even improves, the stability of the switching regulator. The prototype has been implemented using the TSMC 0.18 µm technology; schematic simulation results in Cadence® are presented to prove the concept.

Keywords: Power efficient switching DC/DC regulators, supply modulators, wideband linear power amplifiers (PAs), envelope tracking techniques, wideband wireless standards, 'bang-bang' controller, slew rate-enhancement techniques.

1. Introduction

Radio frequency (RF) power amplifiers (PAs) play a key role in transmitting information between places for communication purposes. These forms of communication could be between mobile phone handsets, base stations, computers or Bluetooth devices. The RF PA's main goal is to transmit the information with enough power and spectral purity to drive the antennae. However, the PA is usually responsible for most of the power consumption in the entire transceiver. Additionally, the PA suffers from poor power efficiency, especially when transmitting low power.

The stringent linearity requirements in broadband systems makes the linear PAs, particularly class A, the preferred choice in the transceiver. This linearity requirement, coupled with the fact that the PA operates at low transmit power during most of its operation, makes the power efficiency of the entire transceiver poor [1]. The limited power efficiency of the transceiver leads to a reduction in the battery life of portable devices like mobile phones, laptops and MP3 players. This issue of poor power efficiency is also critical in base stations where a high efficiency and low power consumption is important in determining the size of heat sinks for cooling purposes.

In this paper, power management techniques are employed for improving the power efficiency of a class-A PA. An efficient technique to offset the slew limitations of the switching regulator architecture used in envelope tracking techniques is proposed. This approach alleviates the problem of low slew rate by adding a *bang-bang* controlled current source. The proposed supply modulator promises an average efficiency of 81.6%. A key advantage is that the proposed scheme enables the use of limited clock frequency switching regulators for signal bandwidths up to 20 *MHz*.

2. Supply Modulator for Power Amplifiers

Wireless transmitters employing envelope tracking techniques are becoming popular nowadays since they provide significant power savings [2]. In envelope tracking techniques, the DSP generates the baseband signal (information to be transmitted) as well as the envelope tracking signal. A supply modulator generates the PA's supply voltage whose output is correlated with the envelope signal. To achieve optimal tracking, the regulator's bandwidth must be higher than the in-band signal bandwidth. The issue is that it is highly desirable to reduce modulator's bandwidth well below the switching frequency to provide enough attenuation to the switching harmonics. Reducing the modulator's bandwidth and clock frequency reduces the switching losses.
The trend of increasing bandwidths and increasing peak to average power ratio of current signal codification schemes such as OFDM makes the design of the supply regulator particularly challenging since it requires wide and fast variations in the supply voltage. The aforementioned conventional switching regulators are very efficient provided that the switching losses and quiescent current consumption are minimized. Thus, clock frequencies cannot be drastically increased. Most existing solutions that deal with these issues combine a linear regulator (or class AB amplifier) in parallel with a switching regulator (architecture referred to as hybrid converters or master-slave modulators) to increase the speed of the supply modulator while maintaining other performances such as small ripple and small switching losses [3]-[6]. However, hybrid converters have the following issues: *a*) relatively high quiescent current consumption; *b*) potential stability issues; and *c*) increased losses due to extra amplifiers.

3. Main Concept Behind the Proposed Solution

The conventional switching regulator is the most efficient way of modulating a supply voltage so far as the switching losses and quiescent current are minimized. As a result, the proposed solution is based on the conventional –step-down or buck– switching regulator architecture. For small ripple applications, the capacitance is usually increased thus limiting the architecture's slew-rate. However, if an auxiliary block is added to the switching regulator such that it supplies current to the output node of the switching regulator when it is slew limited, then the speed of the switching regulator is further enhanced. Figure 1 shows a block diagram of the envelope tracking architecture with the proposed bang-bang controller used to improve the regulator's slew rate. The '*bang-bang*' controller has negligible quiescent current consumption and does not degrade the stability of the switching regulator since it operates on demand only. Furthermore, only positive slew rate needs to be enhanced since enhancing negative slew rate does not help at all to improve PA power efficiency. Additionally, this auxiliary block should only be activated when the digital predictor finds that the baseband signal variations are faster than regulator's slew-rate. All these features are desired to make the system very efficient.

ISBN: 978-84-695-9922-8

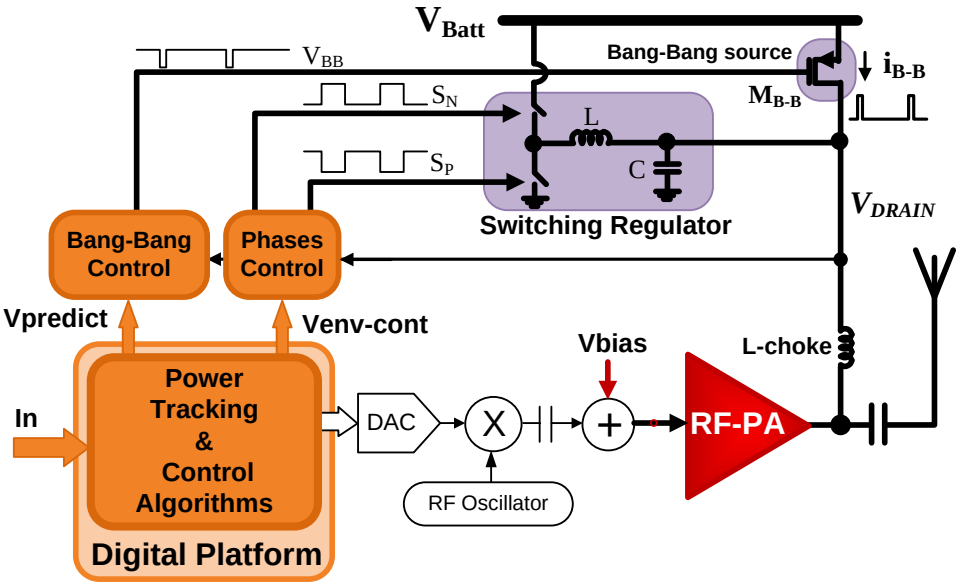

Figure 1. *Block diagram of the transmitter front-end with the proposed supply modulator employing a 'bang-bang' slew enhancer.*

The main highlights of the proposed bang-bang solution are: (*a*) High current efficiency (negligible quiescent current consumption); (*b*) easy to stabilize since the bang-bang action will be sporadic; (*c*) area efficient (only positive slew rate enhancement); (*d*) Optimal performance since the regulator can be designed for small ripple and stability while the slew-rate limitations are offset by the action of the bang-bang current source.

4. Description of the Building Blocks

4.1. Phase Controller and Compensation Network

The phase controller generates the clock phases for controlling the switches S_P and S_N (according to Figures 1 and 2, I change "P" and "N" in capital letters in all the text). It implements a PWM function just as the conventional architecture of a classical switching regulator. A dead time control circuit (DTC) is added to generate non-overlapping clocks to prevent the occurrence of short-circuit currents due to power switches S_P and S_N, being on at the same time. Figure 2 shows the phase controller's schematic. The loop is stabilized employing the error amplifier (EA) which processes the error signal generated; baseband input signal and envelope tracking signal are compared at the input of this block. The EA output is then compared with a triangular waveform to complete the pulse-width modulation process.

If k is the conversion gain of the PWM, defined as duty-cycle of the phases controlling the output waveform S_P and S_N times V_{Batt}, then the transfer function of the phase controller, see Figure 2, can be obtained as:

$$\phi(s) = \frac{-k}{sR_2(C_1+C_3)} \frac{(1+sR_1C_1)(1+sR_2C_2)}{1+sR_1\dfrac{C_1C_2}{C_1+C_3}} \qquad (1)$$

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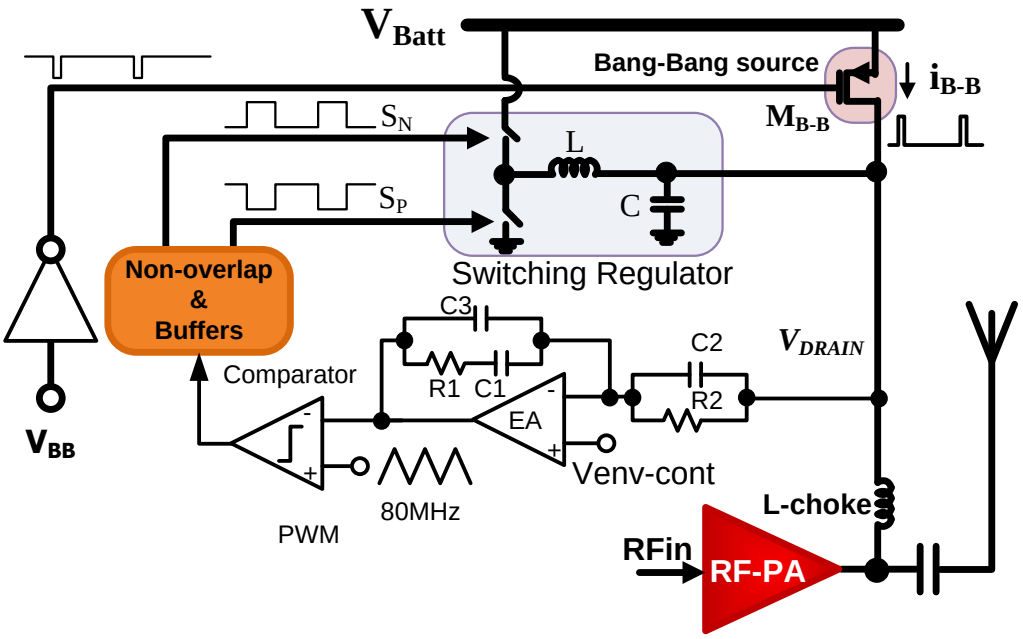

Figure 2. *Circuit level implementation of the proposed architecture.*

Combining this transfer function with the filter transfer function, and considering the fundamental component only, the loop gain becomes:

$$L(s) = \frac{-k}{sR_2(C_1+C_3)} \frac{(1+sR_1C_1)(1+sR_2C_2)}{1+sR_1\frac{C_1C_2}{C_1+C_3}} \frac{1}{s^2LC+s\frac{L}{R}+1}, \qquad (2)$$

where R is the equivalent baseband impedance seen from the drain terminal including R_2; it is assumed that the PA capacitance and C_2 are accounted when computing C in (2). Proper placement of the poles and zeros in the transfer function is needed to stabilize the system under all operating conditions; e.g. PA output resistance varies with signal power and high frequency attenuation is needed to further reduce the power of high frequency switching harmonics. Employing the compensating zeros scheme makes the loop stable and ensures large loop gain over a wide frequency range that minimizes tracking errors between the envelope signal and the output voltage. Table 1 shows the values of the components used to design the compensation network.

Table 1. *Component values of the compensation network.*

R_1	R_2	R_3	C_1	C_2	C_3
18 kΩ	**18 kΩ**	**95 kΩ**	**4 pF**	**1pF**	**100 fF**

The main design considerations for the error amplifier (EA) are: (1) A high gain over a wide frequency range; (2) a wide input common mode range. The envelope signal is required to vary from 0.35 *V* to 1.6 *V* with a 2 *V* supply if modern CMOS technologies are used; thus, the amplifier's input common mode range has to be almost rail-to-rail to accommodate envelope variations within this voltage range; and (3) the amplifier must have a high 3 *dB* corner frequency.

4.2. '*Bang-Bang*' (BB) Controller

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The bang-bang system is required to provide the slew rate needed by the regulator to follow the envelope signal in the event of fast and large power variations. It consists of a control scheme and a switchable current source which is activated if, and only if, the signal variations exceed the regulator's slew-rate. The concept is illustrated in Figure 3. While the input signal speed is within the limits of the regulator's capability, the BB system is in standby. However, when a fast input signal arrives, the controller, equipped with a digital predictor, enables the BB system increasing drastically system slew-rate thus providing enough current and voltage that maintains the PA operating in linear region.

The bang-bang controller signal V_{BB} turns on the current source, M_p, when the output is not able to follow the envelope signal (when the output is slew-limited). The current provided charges up the output node quickly for the output node to follow the envelope signal. The slew rate provided by the BB current-source is given by:

$$I_{BB} > SR_{out}C = V_{\max-envelope}\omega_{\max-signal}C \tag{3}$$

With C=3.6 nF, signal bandwidth of 20 MHz and PA output signal variation of 1 V, the current provide by the bang-bang controller must be over 430 mA. Larger signal variations may require BB currents above 1 A. The bang-bang controller is implemented with a digital predictor and a comparator. In this paper, the predictor is not discussed, only the analog section is addressed.

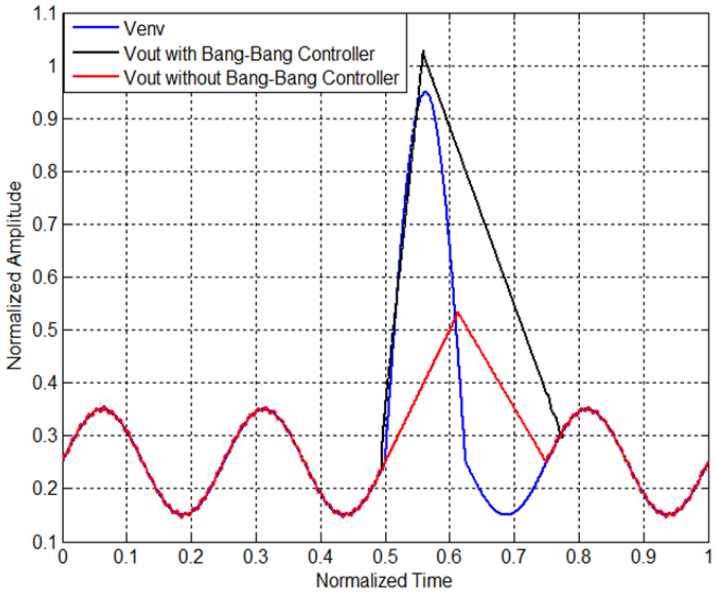

Figure 3. *Envelope signal and switching regulator's output voltage with and without the ideal bang-bang controller.*

The critical parameters of the comparator are speed and common mode range. The comparator's propagation delay is designed to be less than 2 ns for a 100 mV overdrive. The input common mode range is required to be from 0.3 V to 1.6 V since the envelope signal varies within this range. Therefore, the comparator is designed to have a rail-rail input stage, as shown in Figure 4 [7].

4.3. Modulator's envelope control signal $V_{env\text{-}cont}$.

The linear RF-PA is used to test the functionality of the supply modulator. A scaled down version of the envelope signal added to an estimated overhead voltage is used as the reference voltage for the control of the supply modulator according to Figure 5.

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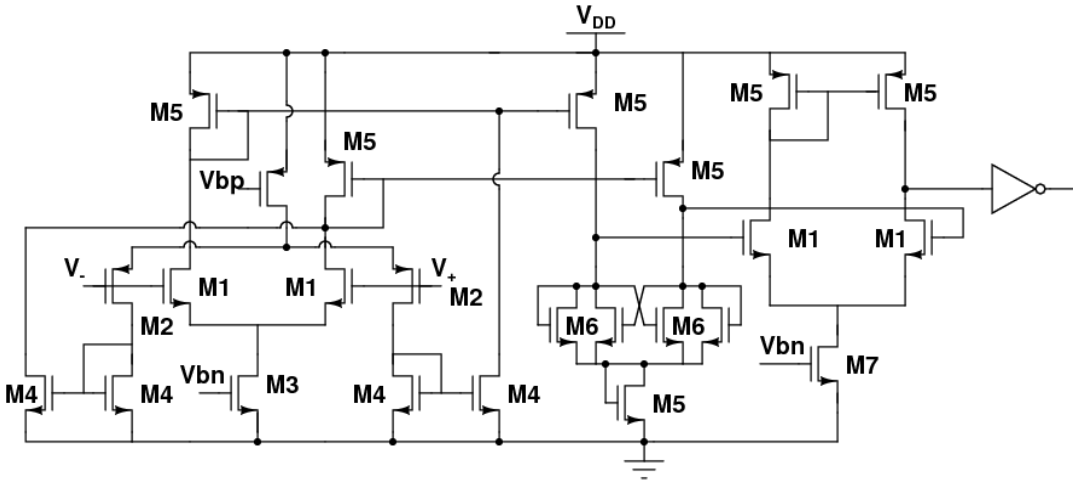

Figure 4. *Simplified schematic of the comparator.*

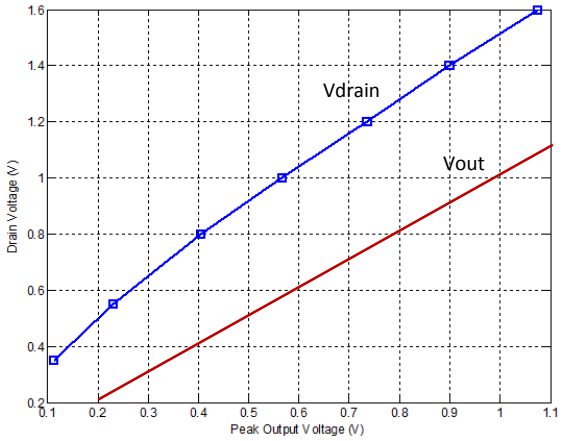

Figure 5. *Plot of PA drain voltage against peak output voltage.*

4.4. Switching Regulator and Selection of *L* and *C*.

The power switches S_P and S_N are implemented with PMOS and NMOS transistors respectively. The proposed switching regulator is designed for equal switching and conduction losses when the static power consumption is equal to the average power consumption of 71.5 *mW*. The dimensions of the switches are shown in Table 2.

Table 2. *Switch dimensions and critical parameters.*

Switch	W (μm)	L (μm)	R_{ON} (mΩ)	C_p (pF)
S_P	3072	0.18	713	8.15
S_N	768	0.18	695	2.56

The switching regulator is designed to handle envelope variations with bandwidths up to 4 *MHz* without any help from the bang-bang controller. As a result, the inherent slew rate of the switching regulator should be enough to handle such envelope variations. To achieve this, the slew rate required will be 16 *mV/ns*. Therefore, a relatively large *L* and small *C* will be the best option because it relaxes the amount of current required by the bang-bang controller to meet the slew requirements. However, for a fixed *LC* product, a large *L* and small *C* cause larger overshoots and undershoot in the presence of load transients; thus, the size of the components have to be carefully evaluated. For this case, with *L*=330 *nH*, and *C*=3.6 *nF*, the switching regulator is able to support

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envelope variations up to 4 *MHz* without any help from the bang-bang controller. A switching frequency of 80 *MHz* is used for this design.

5. Simulation Results

Figure 6 shows a plot of the output voltage and the envelope signal for the proposed supply modulator. These plots show that the stand alone switching regulator and the proposed supply modulator have the same performance for envelope signals up to 4 *MHz*. Figure 7 shows that the stand alone switching regulator is not able to handle 20 *MHz* variations in the envelope signal (dark dotted line) while the proposed supply modulator is able to closely follow 20 *MHz* envelope variations.

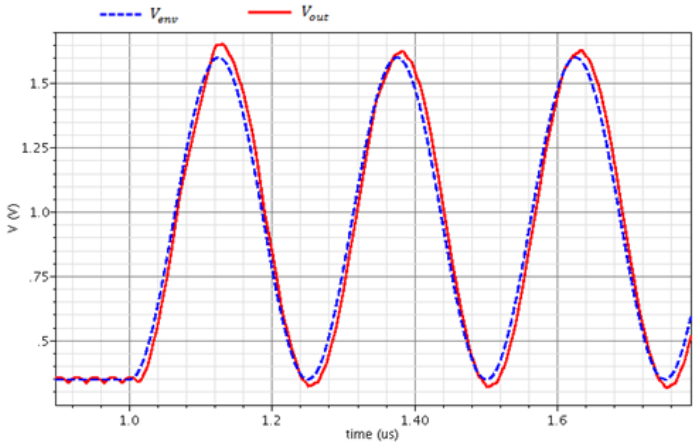

Figure 6. *Modulator's output for a 4 MHz signal.*

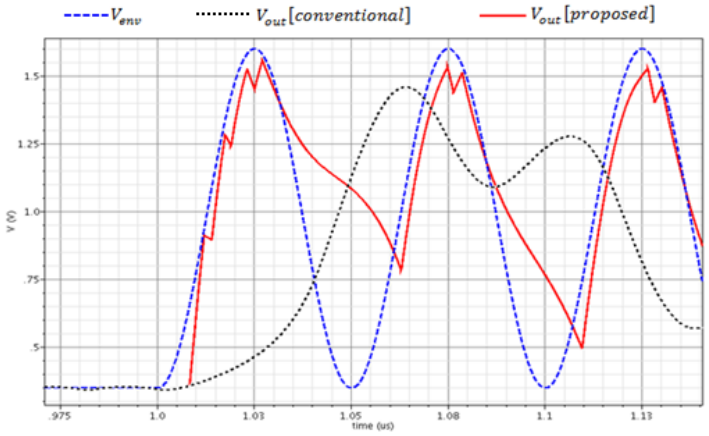

Figure 7. *Modulator's output voltage for a 20 MHz signal.*

The efficiency of the supply modulator is obtained from Cadence®. This efficiency is obtained for different output power transmitted and plotted in Figure 8. The average efficiency of the supply modulator is 81.6%. A summary of performance of the supply modulator with the PA as a load is shown in Table 3. In addition, Table 4 shows how the proposed supply modulator compares with state of the art. It is noticed that the proposed supply modulator simultaneously achieves a high bandwidth and high average power efficiency.

6. Conclusions

The design of an efficient supply modulator for linear wideband RF power amplifiers has been presented. The performance of the supply modulator has been shown for bandwidths up to 20 *MHz*. The proposed supply modulator has negligible quiescent current consumption, is easy to stabilize,

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has high efficiency and is simple to design. It achieves an average efficiency of 81.6% when used in a CDMA handset.

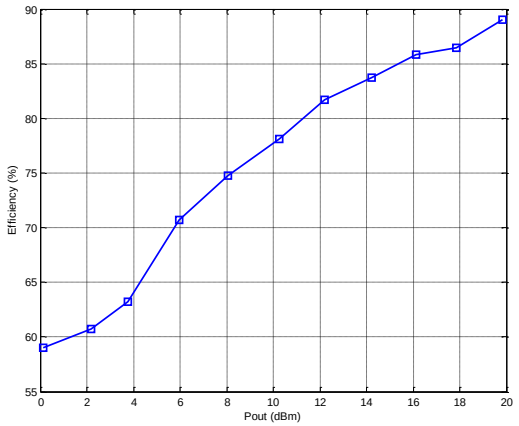

Figure 8. *Plot of the efficiency of supply modulator vs. output power.*

Table 3. *Summary of performance of supply modulator with PA load.*

Supply Voltage	2.0 *V*
Output Voltage Range	0.35 *V* – 1.6 *V*
Maximum Output Power (RMS)	19.5 *dBm*
Quiescent Current (I_{bias})	0.92 *mA*
Maximum Envelope Bandwidth	20 *MHz*
Switching Frequency	80 *MHz*
Output Inductance, *L*	330 *nH*
Load Capacitance, *C*	3.6 *nF*
Average Efficiency: Supply Modulator	81.6%

Table 4. *Comparison of results with state-of-the-art.*

	[2]	**[5]**	**[3]**	**Proposed Architecture**
Techn.	180 *nm* SiGe	65 *nm* CMOS	350 *nm* CMOS	180 *nm* CMOS
Max. BW	20 *MHz*	20 *MHz*	2.5 *MHz*	20 *MHz*
Average Eff.	65%	*59%	*30%	81.6%

* Efficiency at 16 *dBm*.

7. References

1. S. Egolf, “Intelligent Power Management: A Method to Improve 2G/3G Handset Talk Time,” Microwave Journal, pp. 94-100, July 2007.
2. W. Feipeng, et.al., "A monolithic high-efficiency 2.4-GHz 20-dBm SiGe BiCMOS envelope-tracking OFDM power amplifier," IEEE J. of Solid-State Circuits, pp. 1271-1281, June 2007.
3. W.-Y. Chu, et.al., “A 10 MHz Bandwidth, 2 mV Ripple PA Regulator for CDMA Transmitters,” IEEE Journal of Solid-State Circuits, pp. 2809-2819, December 2008.
4. N. Schlumpf, et.al., “A Fast Modulator for Dynamic Supply Linear RF Power Amplifier,” IEEE J. of Solid State Circuits, 1015-1025, Jun 2004.

5. R. Shreshta, et.al., “A Wideband Supply Modulator for 20MHz RF Bandwidth Polar PAs in 65nm CMOS,” IEEE J. Solid-State Circuits, pp. 1272-1280, Apr. 2009.
6. T. W. Kwak, et.al., “A 2W CMOS Hybrid Switching Amplitude Modulator for EDGE Polar Transmitters,” IEEE International Solid-State Circuits Conference, pp. 518-619, 2007.
7. R. J. Baker, CMOS Circuit Design, Layout and Simulation, 2nd ed. Piscataway, NJ: Wiley-IEEE, 2005.

8. Acknowledgments

This work has been partially supported by the Spanish Ministry of Science and Innovation by projects TEC2010-15765/MIC, and TEC2011-27047.