DESIGN OF A MULTI-MODULE AND FULLY INTEGRATED SWITCHED-CAPACITOR DC-DC POWER CONVERTER

A Degree's Thesis
Submitted to the Faculty of the
Escola Tècnica d'Enginyeria de Telecomunicació de Barcelona
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by
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of the requirements for the degree in
Electronic Systems Engineering

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Advisor from NXP Semiconductors: Gerard Villar Piqué

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Abstract

DC-DC converters are one of the main components of a power management unit and, concretely, the Switched-Capacitor DC-DC Power Converters (SCPC) are recently used due to their high efficiency and the possibility of being fully integrated. In this thesis, it is designed a SCPC converter in a 140 nm technology with the objective of replace a low frequency continuous-time regulator. With an input voltage of 20 V, the SCPC converter designed achieve an output voltage of 3.3 V and an output current of 5 mA with a 69% of efficiency. Different mathematical optimization and minimization methods have been developed in order to reduce the losses of the converter and accomplish the specifications. A multi-module structure is implemented with the objective of reducing the total area. Also, it is designed a control loop to provide robustness and load regulation in front of process and temperature variations.
Resum

Els convertidors DC-DC són una de les parts més importants d’una unitat d’administració d’energia i, concretament, els convertidors de potència DC-DC amb condensadors commutats (Switched-Capacitors DC-DC Power Converter, SCPC), són utilitzats recentment degut a la seva alta eficiència i per la possibilitat de ser completament integrats. En aquesta tesi s’ha dissenyat un convertidor SCPC amb una tecnologia de 140 nm i amb l’objectiu de substituir un regulador lineal de baixa eficiència. Amb una tensió d’entrada de 20 V, el convertidor SCPC dissenyat genera una tensió de sortida de 3.3 V, un corrent de sortida de 5 mA i te eficiència del 69 %. Diferents mètodes matemàtics d’optimització i minimització s’han desenvolupat per reduir les pèrdues del convertidor i complir les especificacions. S’ha implementat una estructura multi-mòdul amb l’objectiu de reduir l’àrea total. També s’ha dissenyat un làc de control per proporcionar robustesa al convertidor i regular la càrrega enfront possibles variacions de procés i temperatura.
Resumen

Los convertidores DC-DC son una de las partes más importantes de una unidad de administración de energía y, concretamente, los convertidores de potencia DC-DC con condensadores conmutados (Switched-Capacitors DC-DC Power Converter, SCPC), son utilizados recientemente por su alta eficiencia y por la posibilidad de ser completamente integrados. En esta tesis se ha diseñado un convertidor SCPC con una tecnología de 140 nm y con el objetivo de sustituir un regulador lineal de baja eficiencia. Con una tensión de entrada de 20 V, el convertidor SCPC diseñado genera una tensión de 3.3 V y una corriente de salida de 5 mA con una eficiencia del 69 %. Diferentes métodos matemáticos de optimización y minimización de han desarrollado para reducir las pérdidas del convertidor y cumplir las especificaciones. Se ha implementado una estructura multi-modulo con el objetivo de reducir el área total. También se ha diseñado un lazo de control para proporcionar robustez al convertidor y regular la carga ante posibles variaciones de proceso y temperatura.
Acknowledgements

First of all, I would like to express my gratitude to my supervisor in NXP Semiconductors, Mr. Gerard Villar, who provides me the opportunity to work in this project. He is a talented and professional engineer, and his suggestions deepen my understanding of analog circuit design. Special thanks are given to Mr. Ravi Karadi and Mr. Henk Jan Bergveld, who have helped me in different occasions.

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Last but certainly not the least, a special thanks to my family. Words cannot express how grateful I am to my mother and father for all the sacrifices that you have made on my behalf.
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1. Introduction

The project presented and developed in this thesis is carried out in the R&D department of NXP Semiconductors. The R&D department receive requests from other departments of the company to design and implement a wide range of microelectronic circuits that require innovation. In this thesis, it is presented the design and the implementation of one of the subsystems of a requested chip.

1.1. Application and Objectives

The circuit requested and designed in this project is a DC-DC power converter with an input voltage of 20 V, an output voltage of 3.3 V and an output current of 5 mA. The power converter is one of the parts of a chip that will be used in the voltage supply of an LED lamp. The converter will be implemented in the second version of the chip because, in the first one, the logic parts of the chip were designed with a technology of 250 nm and it was decided to re-build them with 140 nm, which requires a lower voltage supply of 3.3 V.

In the first version of the chip it was used an LDO as a voltage regulator. The problem of LDO regulators is their low efficiency when the input-to-output voltage ratio is high. As it can be seen in (1.1), with an input voltage of 20 V, an output voltage of 3.3 V and knowing that the input and output current of a LDO is the same, the power efficiency is 16.5 %, which is really low. Therefore, as different parts of the chip were re-built, it was decided to request a new and more efficient converter.

\[
\eta = \frac{P_O}{P_{in}} = \frac{V_O \cdot I_O}{V_{in} \cdot I_{in}} = \frac{V_O}{V_{in}} = \frac{3.3 \text{ V}}{20 \text{ V}} = 16.5 \%
\]  
(1.1)

The converter designed in this project will replace the LDO. That means that there are some requirements for the new converter. The circuit designed has to be fully integrated on silicon, so it cannot have any external components. The area is also another important requirement: it can be obtained a higher power efficiency with a larger area, which is the objective of this new converter, but the area is expensive. Therefore, the area occupied by the converter has been limited to 0.75 mm². With this area and knowing that the main objective of the new converter is to achieve an efficiency higher than 16.5 %, the minimum efficiency specification had been limited to 65 %. Table 1.1 summarizes the specifications of the converter that is going to be designed in this project.

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<tr>
<td>Efficiency</td>
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<tr>
<td>Output Voltage</td>
<td>3.3 V</td>
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<tr>
<td>Output Current</td>
<td>5 mA</td>
</tr>
<tr>
<td>Output Ripple</td>
<td>&lt;330 mV</td>
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<tr>
<td>Area</td>
<td>0.75 mm²</td>
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Table 1.1. Requirements of the DC-DC converter
1.2. Classification of DC-DC Power Converters

There are different types of DC-DC power converter architectures that can be designed for this project. They can be divided into two main groups based on their operation: Continuous-Time and Switching DC-DC converters. Each one of the groups have a very different design process, so it is necessary to know which one fits better the converter specifications before setting a Project Plan. The following text explains briefly these two types of converters, presenting their advantages and disadvantages.

Continuous-Time Regulators

Continuous-Time regulators, also known as linear regulators or LDO's, are one of the most widely used voltage regulators due to their relatively small size and operation free of switching noise. Their output voltage is regulated by changing the on-resistance of a pass transistor according to the action of a feedback loop [1]. All the output current is taken directly from the input source through a controlled transistor resistance, so the maximum efficiency of a linear regulator is directly proportional to the ratio between the output and input voltage, can be seen in (1.1). This efficiency limitation is less relevant when the difference between the output and input voltage, also called the dropout voltage, is low; but it becomes critical when the dropout voltage is large.

Switching Power Regulators

The switched mode DC-DC converters operate by storing temporarily their input energy in a reactive device and then releasing it to the output at a different voltage. The transistors used in these converters works in two modes: linear or cutoff. Due to this operation, switching regulators can provide a much higher power efficiency (theoretically 100 %) than linear regulators. However, switching converters are more complex to design than the linear, and they also generate Electromagnetic Interference (EMI) due to their switching action. On the basis of their main energy transfer components, switching regulators are further divided into Inductive and Capacitive switching mode converters.

Inductive switching regulators store energy in the magnetic field and then they release it to the output voltage. As consequence of the switched operation, the output voltage presents a certain amount of ripple. Their biggest advantage is the high efficiency that they can achieve (theoretically are able to provide 100 %), but these regulators have a big size due to the inductor, which makes them unsuitable for integrated applications. Some works like [2] and [3] have been able to design this type of converters completely integrated using monolithic inductors, but the area is still quite large and the efficiency drops due to the parasitic losses of the integrated circuits.

The other type of switching power regulator are the Switched-Capacitor (SC) DC-DC converters. This type of converters use capacitors instead of inductors as the energy transfer main component. They have two principal components: transistors and capacitors. Depending on the number of transistors and capacitors in the SC converter, a wide range of topologies can be configured with different conversion ratios between input and output voltages. As opposite to inductive converters, the SC converters are easier to be integrated due to the planar implementation of the capacitors. These converters have a higher efficiency than the linear regulators with large dropout voltage, but, theoretically, lower than inductive converters.
1.3. State of the Art Switched-Capacitor converters

From the previous classification and with the requirements shown in Table 1.1, it is decided that the converter that is going to be designed in this project will be a Switched-Capacitor DC-DC Power Converter. One of the earlier integrated capacitive converters used in a power-management context was the Dickson topology [4]. Numerous references [5], [6] and [7] follow the approaches presented by Dickson but without any general analysis method, till Makowski and Maksimovik developed a fundamental model in [8] and it was optimized by Seeman in [9].

Switched-Capacitor converters have the advantage of light weight, small size, and high power density [10], and they are also comparable and even superior to inductive switching converters in terms of efficiency at low power levels, although inductive converters generally enable higher output powers [11]. In addition, SC technology can have less EMI when they operate with a single switching frequency clock [12]. These evident benefits have led to increased research in the field of SC DC-DC converters.

However, like all other design approaches, SC converters have some design limitations. A high input voltage might be a problem in advanced silicon processes, as these voltages are much higher than the typical breakdown voltage of the process. Even so, some SC converters with high efficiency are designed at [13] and [14] with a wide range input voltage.

Another limitation of the SC converters is that their integrated capacitors possess high bottom plate parasitic between the bottom plate of the capacitor and the substrate. These can result in an important amount of power loss during the circuit operation due to charging and discharging the bottom plate capacitances, but it is possible to reduce bottom losses depending on the SC converter structure [15].

Some recent works have overcome these aforementioned design limitations. Works [16] and [17] are examples of small size and fully integrated DC-DC converters in 45 nm technology, while references [18] and [19], provide a wide range of voltage conversion as well.
1.4. Work Plan

A working plan schedule is designed once the DC-DC converter type is decided and studied. The Work Plan includes the different steps that must be followed during the nine months project, and the periods and milestones of each part. In the next sections the Work Plan is presented.

1.4.1. Work Packages, Tasks and Milestones

| Project: Theoretical study of DC-DC converters | WP ref: 1 |
| Major constituent: Theoretical study | Sheet 1 of 4 |
| Short description: | Planned start date: 3/03/2014 |
| | Planned end date: 21/04/2014 |
| | Start event: 3/03/2014 |
| | End event: 14/04/2014 |

**Internal task T1.1**: Analysis of possible DC-DC converters

**Internal task T1.2**: Topology study of Switched-Capacitor power converters

**Internal task T1.3**: Study of the chosen technology process

| Project: Switched-Capacitor converter design | WP ref: 2 |
| Major constituent: Hardware design | Sheet 2 of 4 |
| Short description: | Planned start date: 21/04/2014 |
| | Planned end date: 1/09/2014 |
| | Start event: 14/04/2014 |
| | End event: 1/09/2014 |

**Internal task T2.1**: Single DC-DC converter block

**Internal task T2.2**: Drivers and level-shifters

**Internal task T2.3**: Auxiliary Supply Rails and Start-up

**Internal task T2.4**: Non-overlapping and timing block

**Internal task T2.5**: Multi-module structure
**Project:** Optimization and improvement  
**WP ref:** 3  
**Major constituent:** Simulation  
**Sheet 3 of 4**

**Short description:**
Once the power stage is finished is needed to check if it is possible to make some improvements on the design performance and simulate different possible environments.

**Planned start date:** 1/09/2014  
**Planned end date:** 29/09/2014

**Start event:** 27/04/2014  
**End event:** 26/09/2014

**Internal task T3.1:** Losses study

**Internal task T3.2:** Non-linear optimization of switches sizes

**Internal task T3.3:** Process and temperature effect study

---

**Project:** Control Design  
**WP ref:** 4  
**Major constituent:** Hardware design  
**Sheet 4 of 4**

**Short description:**
Design the feedback loop for the Switched-Capacitor to provide load regulation and analyze different control strategies to reduce the output ripple.

**Planned start date:** 29/09/2014  
**Planned end date:** 28/11/2014

**Start event:** 26/09/2014  
**End event:** 28/11/2014

**Internal task T4.1:** Analysis of possible controls

**Internal task T4.2:** Chosen feedback loop design

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**Milestones**

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1.4.2. Time Plan

The Time Plan summarizes the duration of each work package and task, presented in the previous section. The Time Plan is shown in Figure 1.1 and it is presented as a Gantt Diagram showing graphically the beginning and the end of each task.

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</table>

Figure 1.1. Gantt Diagram of the Project Plan

1.4.3. Work Plan modifications

From the beginning there were not any big issues along the development of the project in the design part: all the tasks have been accomplished according the time plan presented at the beginning of the project. However, there were some incidences in the simulation part.

At the task T2.2: Drivers and level-shifters design, some simulations were supposed to be run to check the correct performance of these blocks, but the simulator found some convergence issue. This problem was solved, but it took more than expected, delaying the time plan. However, when the time plan was done, possible incidences were taken into account, giving more time to some of the difficult tasks like this one. Thus, the impact of the overall timing has been minimal.

1.4.4. Incidences

During the design of the single DC-DC converter block (task T2.1), it was decided to do in parallel the losses study (T3.1) and the optimization of the switches (T3.1). At the first version of the Work Plan, the plan was to build and simulate the whole converter in open loop first (WP2) and at the end optimize it and improve it (WP3). However, if the optimization or the losses study had forced to make some critic modification at the first blocks, it would have been necessary to redesign all the following blocks again, being time inefficient. Thus, it was is decided to make the optimization and the losses study along the design of each simple block of the converter, being more time efficient in case of critical changes.
2. Switched-Capacitor DC-DC Power Converters (SCPC)

A SC DC-DC converter is composed by two blocks, shown in Figure 2.1: the conversion block and the control block. The conversion block, also called power stage, is the main part of the converter because it performs the power conversion from the DC input voltage to the DC output voltage. The control block is used to manage the behavior of the converter block in order to achieve the desired converter specifications.

![Figure 2.1. Graphic representation of a SC converter](image)

This chapter describes the fundamental characteristics to design and implement the conversion block with of a Switched-Capacitor DC-DC converter architecture.

2.1. Basic Theory of Switched-Capacitor DC-DC Converters

Switched-Capacitor DC-DC converters are mainly composed by capacitors and switches. The connections of these components can be configured in different ways in order to obtain a wide range of architectures. Firstly, to understand how the SC converter works, an example of voltage doubler, shown in Figure 2.2 (a), is explained. The SC converter has two phases, $\varphi_1$ and $\varphi_2$, and each phase, depending on which switches are on or off, will have different configuration. In the first phase, the floating capacitor is connected between the input voltage and ground, as is shown in Figure 2.2 (b), so it is charged with $V_{IN}$. In the second phase, shown in Figure 2.2 (c), the capacitor is connected between the input and the output voltage. Hence, the output voltage will be the sum of the input voltage and the voltage of the capacitor: twice $V_{IN}$. Due to the buffer capacitance at the output and a frequently repeated switching operation as described, the output voltage will eventually increase and maintain $2V_{IN}$.

![Figure 2.2. Working operation of a voltage doubler: (a) doubler topology (b) phase 1 operation (c) phase 2 operation](image)
To analyze and design the SC converter, the converter can be modeled as an ideal continuous-time circuit composed by an ideal DC transformer and a series resistance connected to the output, as is shown in Figure 2.3. The conversion ratio $M$ of the transformer depends on the topology of the SC converter and it will determine the maximum efficiency (2.1). The series resistance is the average equivalent output resistance, $R_{OUT}$. It is the consequence of charging and discharging the floating capacitors across the internal impedances of the switches-transistors.

$$\eta_{max} = \frac{V_o}{M \cdot V_{in}}$$  \hspace{1cm} (2.1)

The range of possible output voltages depends on the conversion ratio and the $R_{OUT}$ resistance of the converter. All the possible conversion ratios of SC converter were established by the theorem presented in [8]. In it, is obtained that depending on the number of floating capacitors, the conversion ratio $M$ can be modeled as a fraction of the Fibonacci series elements. In Table 2.1 is shown the possible conversion ratios for different conversion ratios.

<table>
<thead>
<tr>
<th>Number of floating capacitors</th>
<th>Conversion Ratio, M</th>
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<tbody>
<tr>
<td>1</td>
<td>$\frac{1}{2}, 1, 2$</td>
</tr>
<tr>
<td>2</td>
<td>$\frac{1}{3}, \frac{2}{3}, \frac{1}{2}, 2, 3$</td>
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<tr>
<td>3</td>
<td>$\frac{1}{5}, \frac{4}{5}, \frac{3}{5}, \frac{2}{5}, \frac{5}{5}, \frac{4}{5}, \frac{3}{5}, \frac{2}{5}, \frac{5}{5}, \frac{4}{5}, \frac{3}{5}, \frac{2}{5}, \frac{3}{5}, \frac{4}{5}, \frac{2}{5}$</td>
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Table 2.1. Conversion ratio values versus number of floating capacitors

The value of the average equivalent output resistance $R_{OUT}$ depends, apart from the converter architecture, on the switching frequency $f_S$, the capacitance of the floating capacitors $C_F$, the on-resistance of the switches $R_{ON}$, and the duty cycle of the clock signal. From Figure 2.3 is obtained the expression (2.2), which sets the relationship between $R_{OUT}$ and the electrical specifications of the converter. According with this figure, that for a maximum efficiency, the output resistance have to be minimum.
In [8] it was determined that the output resistance has two different asymptotic behaviors depending on the switching frequency, as is shown in Figure 2.4 (a): Slow-Switching Limit (SSL) and the Fast-Switching Limit (FSL). Then, in [9] it is developed and obtained an expression to calculate the equivalent output impedance based on the switching limits:

\[ R_{out} = \frac{M \cdot V_{in} - V_o}{I_o} \]  \hspace{2cm} (2.2)

The \( R_{FSL} \) and \( R_{SSL} \) impedances represent the asymptotic values of the FSL and SSL limits, respectively. The value of these two limit resistances can be obtained with (2.4) and (2.5), just when the clock signal has a 50% duty-cycle:

\[ R_{FSL} = p R_{on} \]  \hspace{2cm} (2.4)

\[ R_{SSL} = \frac{m}{f_s \cdot C_T} \]  \hspace{2cm} (2.5)

Where \( R_{on} \) is the on-resistance of the switches, \( f_s \) is the switching frequency, \( C_T \) is the sum of all the floating capacitances and \( p \) and \( m \) are constants that depend on the topology of the converter. Hence, the \( R_{OUT} \) will depend on the previous parameters. If some of them are modified, the asymptotic curve of the output resistance will be modified.

In Figure 2.4 (b), the effects of the variation of the \( R_{FSL} \) and \( R_{SSL} \) parameters over the \( R_{OUT} \) curve are shown.

![Figure 2.4](image-url)

**Figure 2.4.** (a) Output impedance as a function of the switching frequency (b) \( R_{OUT} \) curve subject to different parameter variations [20]
2.2. Switched-Capacitor Converter Power Losses

The Switched-Capacitors converters have different loss mechanisms due to their own converter nature and to the parasitics of their implementations. There are three important loss mechanisms: conduction, bottom plate and gate drive losses.

Conduction Losses

The efficiency loss due to the topology structure is known as conduction loss. This losses are caused by charging and discharging the floating capacitors of the converter via power switches with a finite $R_{\text{ON}}$. They are modeled as the power dissipated in the average equivalent output resistance $R_{\text{OUT}}$, as is shown in (2.6).

$$P_{\text{OUT}} = I_0^2 \cdot R_{\text{OUT}}$$  \hspace{1cm} (2.6)

The $R_{\text{OUT}}$ have to be small to minimize the conduction losses. This losses are the responsible of the upper limit of the power efficiency set by (2.1), so, in principle, a low value of $R_{\text{OUT}}$, as well as small $M \cdot V_{\text{IN}} - V_{\text{OUT}}$ difference, is preferred to reduce conduction losses. However, that would require bigger devices and higher switching frequency, which would increase the switching losses and the size of the converter.

Bottom Plate Capacitance Loss

SC converters have the advantage that all their components can be integrated, but it is also a drawback because due to the integrated implementation of the capacitors, parasitic capacitances exist from the bottom plate of the charge transfer capacitors to ground. The power loss due to the bottom plate capacitance is modeled as [21]:

$$P_{\text{BP}} = f_s \cdot \sum_i C_{\text{BP},i} \cdot V_{\text{BP}}^2 \hspace{1cm} (2.7)$$

Where $f_s$ is the switching frequency, $C_{\text{BP}}$ are the bottom plate capacitances and $V_{\text{BP}}$ are the voltage swing across each of the bottom plate capacitances. The bottom plate capacitances are charged and discharged along the two phases of the converter and the energy stored on them is wasted. Therefore, the larger the bottom plate capacitance is, the higher the energy loss will be, and the efficiency will drop.

Switching Loss

As the floating capacitors, the transistors used as switches in SC converters also have parasitic capacitances. When the transistors are switched on and off, their parasitic capacitances are charged and discharged, so part of the energy is wasted in them and the efficiency is reduced. The power consumed in this process is given by [22]:

$$P_{\text{SW}} = f_{\text{SW}} \cdot \sum_i C_{\text{MOS},i} \cdot V_i^2 \hspace{1cm} (2.8)$$
Where $C_{\text{MOS}}$ represents the parasitic capacitances between the four terminals of a MOS transistor, shown in Figure 2.5, and $V_i$ represents the maximum voltage swing across these parasitic capacitors. The switching losses will be increased with bigger transistors, associated with bigger channel widths. On the other side, smaller transistors width results in higher $R_{\text{ON}}$, which will increase the conduction loss. Hence, there must be found an optimum design in order to obtain the maximum efficiency.

![Figure 2.5. MOS transistor parasitic capacitances](image)

With the three types of losses explained above, the overall efficiency equation of the SC converter can be expressed like (2.9):

$$\eta = \frac{P_O}{P_O + P_{R_{\text{OUT}}} + P_{PB} + P_{SW}}$$

(2.9)

Where $P_O$ is the total output power, $P_{R_{\text{OUT}}}$ is the conduction loss, $P_{PB}$ is bottom plate capacitance loss and $P_{SW}$ is the switching loss. To minimize the power loss, the sizing of the switches and the capacitors, as well as the choice of the switching frequency, need to be focused in the value of $R_{\text{OUT}}$ that provides the required $V_O$ and $I_O$ for a given conversion ratio.

### 2.3. Multi-Module Interleaved SCPC

The conversion block, shown in Figure 2.1, used to be composed by a single power stage, formed by one SC converter circuit. A different and more recent way to design this block is by implementing a multi-module structure. This structure is based on the distribution of a number of equal power stage modules in parallel, with all their outputs connected together. All the blocks are identical and they are connected in parallel, so the output voltage of the structure will be the same as the individual modules output voltage. On the other side, the total output current will be the sum of all the output currents of the power stage modules. Thus, the output current of each module can be expressed as (2.10).

$$I_{\text{out one module}} = \frac{I_{\text{out SC converter}}}{\text{number of modules}}$$

(2.10)
All the SC converters modules of the multi-module structure must have the same switching frequency to generate all of them the same output voltage and output current, but the clock signals of each module must have different phases. This way, each module will generate power in different moments in time, the output will receive a close to constant charge injection and the ripple will be lower.

The main objective of the multi-module structure is to reduce or even eliminate the output buffer capacitance. The capacitors are the biggest component of the SC converters, so with this technique the total area can be reduced. All the power stage modules will be connected to the output and, at the same time, some of the floating capacitors of each SC converters will be connected to the output and added to the output buffer capacitor. Hence, the integrated output buffer capacitor can be reduced or eliminated and the total area can be also reduced by using the floating capacitors.
3. Switched-Capacitor Power Stage design

A Switched-Capacitor DC-DC Power Converter is composed by different blocks. In this chapter are described the different steps followed to choose the optimum circuit architecture and components, to design a single SC converter module and, finally, to implement a multi-module structure.

3.1. Topology selection

The first step on the design of a SC converter is to choose a circuit architecture, also called topology. The chosen circuit architecture will depend on the input to output conversion ratio (M) and the number of floating capacitors of the converter. As can be seen in equations (2.1) and (2.2), the maximum efficiency ($\eta_{\text{max}}$) and the average equivalent output resistance ($R_{\text{OUT}}$) depend on M. These two parameters are the most important: if the $R_{\text{OUT}}$ value was too small, the switching losses would increase and the power efficiency, would be reduced. The $\eta_{\text{max}}$ and the $R_{\text{OUT}}$ of different conversion ratios are calculated and compared in Appendix 1 section 1. It is obtained that the best M for the given specifications is M=1/5. With this ratio, it is possible to achieve a maximum efficiency of 82.5% and $R_{\text{OUT}}=140$ Ω.

Each conversion ratio can be implemented by different topologies that depend on the number and the configuration of the different components. The main components of a SC converter are the switches and the floating capacitors. As is shown in Table 2.1, the conversion ratio of 1/5 would have at least 3 or more floating capacitors. Appendix 1 section 2 presents the mathematical analysis done to three different topologies that provide M=1/5. From this analysis, it is obtained that the optimum circuit architecture is the one shown in Figure 3.1 (a).

![Figure 3.1. Operation of the proposed M=1/5 topology: (a) schematic (b) phase 1 configuration (c) phase 2 configuration](image-url)
In Figure 3.1 (a), it is shown the main SC converter block with the distribution of the floating capacitors and switches. All the switches have a tag that indicates in which phase they must be closed to obtain the two circuit configurations presented in Figure 3.1 (b) and (c), corresponding to the 2 phases of the clock signals.

### 3.2. Single Module Power Stage design

A multi-module structure is going to be implemented with the objective of reducing the output buffer capacitor, as is explained in section 2.3. Hence, for this project, it is decided to implement a five-module structure with the same SC converter each one. From equation (2.10) and knowing that a five-module structure is going to be implemented, each SC converter must be designed with an output current of 1 mA.

As is explained in section 2.3, the five converters must have the same clock switching frequency $f_S$, but each clock signal must have different phases. The distance between two consecutive signals must be the same, so the out of phase must be $T_d = T_s/5$. Figure 3.2 shows the five out of phase square signals module that must be obtained to implement the multi-module structure.

**Figure 3.2. Five square out of phase signals**

In this section, the 1mA converter module with the topology shown in Figure 3.1(a) and other blocks required for the implementation of a multi-module structure are designed.

### 3.2.1. Capacitors and Switches design

Two steps are followed for the design of the main components of a single SC converter module. First, the values of the channel widths ($W$) of the power switches and the capacitances ($C$) of the floating capacitors are designed for a module of an output current of 5mA. Then, to obtain the 1 mA module it is deducted from (2.2) and (2.3) that the capacitances and the widths values must be divided by the number of modules, in this case 5. In the text below, the design of the floating capacitors and the switches of the converter is presented.
Floating Capacitors selection and sizing

The capacitors are the biggest components of the SC converters and the area is one of the most critic specification, so it must be found an optimum distribution of the floating capacitors (C_F) and the switching frequency (f_S) for the proposed topology. As shown in Figure 3.1 (a), the topology chosen has four floating capacitors and each one has to withstand different voltages, so different technological implementations of the floating capacitors are needed. As explained in section 2.2, the bottom plate losses depend on the switching frequency (f_S) and the topology, but also on the technology of the capacitors. Therefore, a mathematic study was done, presented in Appendix 2, to optimize the f_S and the area in order to reduce the switching losses. At the end of the study it is obtained that the optimum switching frequency is 10.77 MHz and the optimum technology to implement all the floating capacitors is Fringe Capacitor, with C_1=C_2=C_3=C_4=150pF.

The values in the study are calculated for an output current of 5 mA. Following the procedure explained at the beginning of this section, the capacitances must be divided by five to obtain the 1 mA module values. Therefore, the four capacitances will be 30 pF.

Switches selection and sizing

One of the difficulties of the SC converter requested is its high input voltage. The native transistors of the technology used as switches have low break down voltage: 1.8 V or 3.3 V; but for the present design there are required switches with a break down voltage up to 8 V. For this reason, a special technology option is used with a higher break down voltage in some of the switches.

The choice of using NMOS or PMOS depends on the position of the switch in the converter. NMOS transistors are used more often than PMOS because they have smaller size for the same on-resistance. However, this choice also depends on the availability on generation of the corresponding gate driving voltages. In some switches, a PMOS transistor is preferred over an NMOS because the driving voltages are easier to generate or another transistor has the same driving voltage needed.

The type and the widths of the transistors are designed based on the previous considerations. The complete design procedure is explained in Appendix 3 section 1. Figure 3.3 shows the final SC converter proposed with the chosen MOS switches. It also shows, in green, the node voltages of the converter along the 2 phases of operation, calculated with assumption of no-load condition and ideal switches.

With obtained values, the efficiency is η=74.5 %, which is lower than the maximum efficiency expected from this topology: η_max=82.5 %. As explained in section 2.2, the SC converters are sensitive to the bottom plate and the switching losses. The bottom plate losses are already minimized at the capacitors design, so a mathematical study is done to minimize the switching losses by optimizing the widths of the power switches. The developed study is presented in Appendix 3 section 2, and with the obtained optimized values, the efficiency is η=76 %. It may seems that it is not a big change between before and after the optimization, but in more advanced stages of the design, a 1.5 % of efficiency will be very significant.
The switches design is finished by obtaining the widths values of the 1 mA module, which are shown in Table 3.1.

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<thead>
<tr>
<th></th>
<th>SW1</th>
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<th>SW3</th>
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<td>GO2</td>
<td>GO2</td>
<td>GO2</td>
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<td>GO2</td>
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</table>

**Table 3.1. Optimized widths of the switches for 1mA modules**

### 3.2.2. Power Drivers and Level-Shifters

The power drivers are needed to switch on and switch off the power transistors in the corresponding phase. From the Table A3.2 of Appendix 3, where are shown the drive voltages needed to switch on or off each transistor, it is obtained that three different types of driving circuits must be designed: a simple buffer driver, a high voltage buffer driver with an output voltage swing equal to the breakdown limit of GO3 devices and a cascode buffer for clock voltages above the breakdown limit.

The simple buffer is designed for the switches that need 3.3 V to GND gate drive voltages. The 3.3 V is taken directly from the output voltage of the converter, so is not necessary to generate an extra voltage. This buffer, as shown in Figure 3.3 (a), is implemented as a chain of inverters with increasing sizes towards the output, as a tapered buffer, to reduce the RC effect of the parasitic capacitors of the transistors.

The high voltage buffer is designed for the switches SW1 and SW8 that need gate voltages between two high voltage rails, but the voltage swing is at the breakdown limit. These drivers are designed as the simple ones but including a level-shifter to rise the input clock voltage levels. Figure 3.3 (b) shows the high voltage buffer designed for switch SW1.
The last buffer type, the cascoded buffer, is designed to drive switches SW6, SW7 and SW9. These switches need a clock swing greater than breakdown voltage, so, as is shown in Figure 3.4 (c), it is designed a cascoded structure with two level-shifters to increase the output voltage swing, without exceeding the breakdown voltage of the transistors of the output stage.

![Diagram of the cascoded buffer](image)

**Figure 3.4. Drivers design: (a) simple buffer (b) high voltage buffer at breakdown limit for SW1 (c) cascode buffer for clock voltages above the breakdown limit**

### 3.2.3. Auxiliary Supply Rails and Start-up

The previously designed drivers need three auxiliary constant supply voltages of 8 V, 12 V and 16 V that must be generated in an efficient way in order to avoid significant degradation of the overall power efficiency of the converter. As it can be seen in Figure 3.2, the converter generates by itself the required auxiliary voltages in some of the nodes, so it is designed a switching system to store those voltages. Using three transistors as switches and operating them according to the converter phase, three capacitors are connected to the desired nodes to store the voltages. As an example, Figure 3.5 shows the circuit designed to store 16 V.

![Diagram of the auxiliary supply rail](image)

**Figure 3.5. Auxiliary supply rail to store 16 V**
With a single SC converter module of 1 mA there would be some problems because the capacitors are only charged during one phase and the voltage stored would not be enough to supply all the drivers. Nevertheless, with the multi-module structure and interleaving operation will not be any problem: the auxiliary supply rail structure will be implemented in the node of each module and then connected to a common capacitor for all the modules. This way, at least one of the modules will inject charge to the capacitors due to the five switching phases equally distributed, as is explained and designed in section 3.3, and there will not be any lack of charge or significant voltage drop in the storage capacitors.

To implement this auxiliary supply rails option is necessary a start-up circuit to charge, first, the supply capacitors before the converter begins to work. Due to the limited time of this project, it is designed an auxiliary suboptimum circuit for the test chip of the converter. Hence, in advanced stages and after check the correct performance of the designed SC converter, a more compacted start-up should be designed.

3.2.4. Non-overlapping Switching Signals design

As explained in section 2.1, the switches of a SC converter are operated by two distinct non-overlapping clock signals, $\varphi_1$ and $\varphi_2$. These two signals are used to switch the SC converter between the two phases shown in Figure 3.1 (b) and (c). The non-overlapping period of the clock signals is an important parameter and it must be designed carefully, since it avoids shortcutting the capacitors when transistors switch from one phase to the other. If the lapse is too long, the inactivity period of the converter will be also long and the efficiency and the output power of the converter will decrease. The non-overlapping cannot be neither too short because otherwise there would be shortcuts between the converter capacitors.

Figure 3.6 (a) shows the circuit designed to obtain the two non-overlapping clock signals from a square signal. In this case, the signals would be considered active low.

![Non-overlapping Switching Signals design](image)

Figure 3.5. Non-overlapping: (a) circuit proposed (b) input and output graphics
The most important part of this circuit is the delay block showed in Figure 3.6 (a). This block will introduce the non-overlapping delay $\delta$ between the two phases, as can be seen in Figure 3.6 (b). For the proposed SC converter and after a study done with different $\delta$ values, the delay value is fixed as the 3 $\%$ of the switching period of the converter, $\delta=2.5$ ns. This delay block is designed as a row of inverters with big channel lengths in the transistors.

### 3.3. Five-Phases Oscillator

All the previous blocks are designed with the objective of implementing a multi-module structure. The five square clock signals shown in Figure 3.2 are needed as input of the non-overlapping circuit to generate the two phases for each power stage. These five signals must have the same switching frequency but they must be out of phase. The phase between the signals is necessary because, as is explained in section 2.3, one of the objectives of the multi-module structure is to switch the different power stage modules at different moments.

The distance between two consecutive signals must be the same, and knowing that the switching frequency of all the square signals is the one calculated in section 3.2.1, $f_s=10.77$ MHz, it is obtained that the out of phase must be $T_d= T_s/5=18.57$ ns. Figure 3.6 shows an example of the five out of phase square signals.

A ring oscillator is designed to obtain the five out of phase signals. This type of oscillator is composed by an odd number of inverters, which force the circuit to oscillate and to have the same phase between the consecutive signals. In Figure 3.7 is shown the ring oscillator designed.

![Figure 3.7. Ring oscillator circuit](image)

The frequency of the oscillator is obtained by modifying the length of the transistors, making the inverters slower. The ring oscillator designed also includes an enable signal by using a NAND gate to activate the oscillator when the start-up circuit finishes charging the auxiliary supply capacitors.
3.4. Multi-Module Structure

All the blocks previously designed are assembled to obtain the multi-module SC converter. The converter is composed by: one ring oscillator that generates five out of phase square signals, five blocks that generate two non-overlapping clock phase signals of each converter, five power stages with an output current of $I_o=1 \text{ mA}$, and three capacitors that store the auxiliary voltages needed by the drivers. The block diagram of the SC converter is shown in Figure 3.8.

![Diagram of the SC converter](image)

**Figure 3.8. SC converter blocks diagram**

The five outputs of the power stage modules are connected together to obtain the output current of $I_0=5 \text{ mA}$ requested in the specification. The objective of the multi-module structure is to reduce the big output buffer capacitor that SC converters need to reduce the output voltage ripple. Therefore, a capacitor of 50 pF is estimated to be sufficient and is included at the output of the converter.

Finally, the achieved power efficiency of the Switched-Capacitor DC-DC Power Converter with an output voltage of 3.3 V and an output current of 5mA is $\eta=71.6 \%$. The specifications of the converter are accomplished and the next step is to design a feedback loop to regulate the output voltage in front of $V_{IN}$ or $I_0$ variations.
4. Switched-Capacitor DC-DC Converter Control Design

In this chapter, it is designed the feedback loop for the SC converter presented before. This control is implemented with the objective of providing load regulation at the output voltage. Four different types of control have been identified, studied and compared to find the optimum for the designed converter. In Appendix 4, the three discarded controls studied are presented. Pulse Skipping Control is the chosen control for the proposed SC converter and it is presented and designed in the next sections.

4.1. Pulse Skipping Control

The proposed Pulse Skipping controller is implemented by two blocks: a comparator and a stat-machine. The block diagram of the control is shown in Figure 4.1. The first block is responsible of comparing the output voltage ($V_O$) with a reference voltage, using a clock comparator: if $V_O < V_{ref}$, the output of the comparator ($V_{error}$) will be a 0 V, and if $V_O > V_{ref}$, then $V_{error} = 3.3$ V. The used comparator is a block already designed that compares the two input signals at the falling edge of a clock signal and then it shows the comparison result at the rising edge.

The second block is composed by five state-machines (SM) and an oscillator, as can be seen in Figure 4.2. The output signals of the SMs will be used as the inputs of the non-overlapping blocks of the converter. For $V_{error} = 3.3$ V, the outputs of the SMs will remain constant, and the non-overlapping blocks will also generate two constant signals each. This will freeze the operation of the converters. For $V_{error} = 0$ V, the output will switch from $3.3$ V/0 V to 0 V/3.3 V till $V_O$ rises.

![Figure 4.1. Pulse Skipping control block diagram](image)
The performance of this control is as follows: when \( V_O > 3.3 \, \text{V} \), the state-machines outputs will be constant, so the non-overlapping circuits will not generate any switching phases, the converter will remain frozen and the output voltage will decrease due to \( I_O \) discharging the output capacitance. On the other hand, when \( V_O < 3.3 \, \text{V} \), the state-machines will operate as an oscillator and will generate five square signals till \( V_O \) rises above \( V_{\text{ref}} \). As an example, Figure 4.3 shows a graphic with the significant signals of the control and it is also shown the performance of one state-machine. The other state-machines work as the one shown in the figure but with different phases.
4.1.1. Comparator Block Design

The output voltage of the SC converter must be 3.3 V, but it might change due to $V_{IN}$ or $I_O$ variations. Therefore, a comparator is used to detect when $V_O$ is lower or higher than 3.3 V. The comparator block is composed by a clocked comparator, already designed before the execution of this project, that compares the two input signals at the falling edge of the clock and then it shows the comparison result at the rising edge. A voltage divider, a bandgap reference and a ring oscillator, that generates the clock signal required by the comparator circuit, complete this comparator block. The block diagram is shown in Figure 4.4.

![Figure 4.4. Comparator block circuit](image)

The bandgap reference is a block already designed that provides a $V_{ref}=1.27$ V. Consequently, a voltage divider is designed to adapt $V_O$ to the $V_{ref}$ range. The total value of the two resistances of the voltage divider must be big to reduce their current consumption. The calculated values to obtain an auxiliary output voltage of the divider of $V_{ref}=1.27$ V when $V_O=3.3$ V are $R_1=307.6$ kΩ and $R_2=192.4$ kΩ, with a total value of 500 kΩ.

The most important parameter of the comparator block is the sampling frequency ($f_{comp}$) provided by the ring oscillator composed by three inverters. If $f_{comp}$ is too high, the power consumption of the comparator will be high, reducing significantly the efficiency. On the other hand, if $f_{comp}$ is too low, the comparator will not be fast enough to detect when the output voltage will cross the reference, so $V_O$ will rise or fall too much and the SC converter will not accomplish the ripple specification. A study is done to obtain the optimum $f_{comp}$ with an equal compromise between efficiency and ripple results, and it is obtained that the sampling frequency must be 200 MHz. Then, a ring oscillator is designed as the one presented in section 3.3, but just with three stages and a channel length of 2.3 µm.
4.1.2. State-Machine Design

As is explained at the beginning of section 4.1, each one of the state-machines has two different states depending on $V_{\text{error}}$. For $V_{\text{error}}=0$ V, $V_O$ is lower than $V_{\text{ref}}$, and the converter needs to supply more power at the output. This required power is given by changing the phase of the converter (switch between the two circuit phases shown in Figure 3.1 (b) and (c)). Thus, the state-machine will switch its output from 3.3 V/0 V to 0 V/3.3 V. On the other side, when $V_{\text{error}}=3.3$ V, $V_O$ is higher than the voltage reference and the converter does not need to supply any more power. Hence, the phase of the converter will not be switched and the output of the state-machine will remain with the previous value. Figure 4.5 (a) shows the corresponding states diagram, and in Figure 4.5 (b) the logic circuit obtained from the states diagram is shown.

![Diagram](image)

Figure 4.5. State-Machine: (a) states diagram (b) circuit designed

If $V_{\text{error}}=0$ V, the SMs have to switch between 3.3 V and 0 V. The component that fixes the switching frequency is the clock of the flip-flop. This flip-flop is activated at the rising edge, so the clock frequency must be twice the desired switching frequency of the converter to change the state and provide the correct output square signal when $V_{\text{error}}=0$ V. The oscillator used for the flip-flops is the one designed in section 3.3, but with different lengths, $L=4.1$ µm, to obtain a switching frequency of 21.54 MHz.
5. Results

The feedback loop circuit designed in chapter 4 is assembled together with the converter designed in chapter 3. A first simulation is done with a temperature of 105 °C and under a nominal process corner to check the correct performance of the full SC converter. In Table 5.1, are shown the results obtained from the designed converter and they are compared with the specification values.

<table>
<thead>
<tr>
<th>Specifications</th>
<th>SC converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Integrated</td>
<td>Yes</td>
</tr>
<tr>
<td>Efficiency</td>
<td>&gt;65 %</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Output Current</td>
<td>5 mA</td>
</tr>
<tr>
<td>Output Ripple</td>
<td>&lt;330 mV</td>
</tr>
<tr>
<td>Area</td>
<td>0.75 mm$^2$</td>
</tr>
</tbody>
</table>

Table 5.1. Specifications and obtained results comparison

The results obtained with the converter are adhered to the specifications. During this project, a Switched-Capacitor DC-DC power converter fully integrated has been successfully designed with a conversion ratio of 20 V to 3.3 V, an output current of 5 mA and an efficiency of 68.78 %, greater than 65 %. The main drawback of the implementation is the area used by the converter, which is estimated to exceed the original specifications. The layout of the designed converter is not done, so the final area cannot be certainty known, but with an approximation is obtained that the total area will be 0.85 mm$^2$. The SC converter designed will be implemented in a test chip, so it is just designed to have an approximation of how the converter will work and correct the possible mistakes. After evaluating the test chip, a re-design of the circuit will be required with more focus on its production. That means that the final area will not be the same as the estimated on.

The significant signals of the SC converter obtained with the simulation are shown in Figure 5.1. The signal (a) is the comparator clock signal of 200 MHz that sample the output voltage, shown in (b). In the output voltage signal graphic, it can be seen the effect of the multi-module structure: when each SC converter module inject power to the output with different phases, the output voltage rises up. The result of the comparator, $V_{error}$, is shown in signal (c), which is high or low depending if the output voltage is higher or lower than the voltage reference. Then, the output of the comparator is connected to the five state machines. In the graphic (d) are shown the five clock signals of each state-machine and in (e) are shown their outputs, which remain constant if the $V_O$ is than 3.3 V or oscillate if $V_O$ is lower. The high level voltage of all the clock signals shown in Figure 5.1 is not constant at 3.3 V because, due to the design of the different blocks of the SC converter, the 3.3 V are directly the output voltage and all the signals follow its shape when are in high level.
A part from the previous simulation results, it is also necessary to check the behavior of the converter with other temperature and process corners, and verify that it accomplishes the specification. The typical temperature values tested are -40 °C, 25 °C, 105 °C and 125 °C, and for the process corners the NMOS and PMOS transistors speed is the parameter modified. The speed variations of the transistors are simulated because there are small variations in the implementation process of each transistor that can affect the speed of each transistor, making them faster or slower. The simulator has three limit process corners to simulate these manufacturing variations: nominal (without any implementation variation), snsp (Slow NMOS, Slow PMOS) and fnfp (Fast NMOS, Fast PMOS). In Figure 5.2, the results obtained by simulating the SC converter designed with different temperatures and the three corners are shown.

As it can be seen, the results obtained fit the specifications, except a couple of cases. One problem is the low efficiency at the fnfp corner at 125 °C. The efficiency drops below 65 % because the consumption of the level-shifters is increased at that temperature and process corner. It must be said that the fnfp and the snsp processes are the worst cases, so the probability of obtaining these limit characteristics in all the transistors is rear, and, even so, the converter would still remain functional.
Figure 5.2. Temperature and corners variation results of (a) Efficiency (b) Output Voltage (c) Output Current (d) Output ripple
6. Budgets

The project’s budgets have been divided into two groups: human and the software resources costs. This project has been executed in a company, so, due to the confidentiality agreement, the budgets presented below are just a realistic approximation. The total costs of the project is derived from the sum of the following items:

**Human Resources**

In the human resources costs are included the salaries of the people involved on this project: one student, which has been the developer, under the supervision of one senior member of the company. Taking as a reference the average salaries of a junior and a telecommunications engineers in the Netherlands, it has been considered a salary of 6 € per hour and 23 € per hour for the student and the supervisor. The project has lasted for 9 months, and the student has worked full-time during all the period, meanwhile the supervisor has devoted 4 hours per week on face to face meetings and other supervising tasks. The total human resources costs are summarized in Table 6.1.

<table>
<thead>
<tr>
<th>Role</th>
<th>Price</th>
<th>Working hours</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Student</td>
<td>6 € per hour</td>
<td>1440 h</td>
<td>8640 €</td>
</tr>
<tr>
<td>Supervisor</td>
<td>23 € per hour</td>
<td>144 h</td>
<td>3312 €</td>
</tr>
</tbody>
</table>

Table 6.1. Human resources associated costs

**Software Resources**

The software used for this project is:


- *Cadence, Virutoso plataform.* Tool for design full-custom integrated circuits. Developed by Cadence Design Systems, Inc. Price: 42€. Available at: [https://www.cmc.ca/WhatWeOffer/Products/CMC-00200-00470.aspx](https://www.cmc.ca/WhatWeOffer/Products/CMC-00200-00470.aspx)

A realistic amortization study of the software used for this project cannot be done because all the licenses bought by the company are available for all the workers. Therefore, to obtain the budgets overview it is assumed that 2000 hours of work can carried out with each software during 2 years. Table 6.2 shows the software resources associated costs.
<table>
<thead>
<tr>
<th>Software</th>
<th>Price</th>
<th>Amortized prize</th>
<th>Work time (h)</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Matlab</td>
<td>69 €</td>
<td>0.017 € per hour</td>
<td>500</td>
<td>9 €</td>
</tr>
<tr>
<td>Cadence</td>
<td>42 €</td>
<td>0.01 € per hour</td>
<td>1200</td>
<td>12 €</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>21 €</td>
</tr>
</tbody>
</table>

Table 6.2. Software resources associated costs

**Total Budget**

The total costs of this project are the sum of the human and software resources, as is shown in Table 6.3. It must be considered that this project is entirely a design project, so the main costs are from the engineer developer.

<table>
<thead>
<tr>
<th>Concept</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human Resources</td>
<td>11952 €</td>
</tr>
<tr>
<td>Software</td>
<td>21 €</td>
</tr>
<tr>
<td></td>
<td>11972 €</td>
</tr>
</tbody>
</table>

Table 6.3. Total budget
7. Conclusions and Future Work

This thesis presents the design of a multi-module and fully integrated Switched-Capacitor DC-DC Power Converter, requested to the R&D department of NXP Semiconductors. With a conversion ratio of 20 V to 3.3 V, it is obtained an efficiency of 68.78% with an output current of 5 mA. A high efficiency is obtained with the designed converter, compared with the previous one used, which was a LDO converter with an efficiency of 16.5 %. The main components of the converter, the capacitors and the switches, are mathematically optimized with the aim of reducing the switching and the bottom plate losses to obtain the optimum efficiency.

The converter is designed with a Switched-Capacitor architecture instead of an Inductive or Linear regulator topology, to reduce the total area and enable its full integration. The area is also reduced by designing the converter with an innovative multi-module structure that allows to reduce the output load capacitor size. The multi-module is implemented by designing 5 equal SC converter modules with an output current of 1 mA each one, and then, to obtain an output current of 5 mA, the outputs are connected in parallel.

A feedback loop is designed with the objective of provide load regulation. The feedback loop implemented is a Pulse Skipping control composed by a comparator, two ring oscillators and five state-machines that, depending on the output voltage, will drive the converter to inject more power or not to the output.

The implemented Switched-Capacitor converter is built from scratch and there are only used three already existing blocks. The new generated blocks have been designed starting from ideal blocks, switches and capacitors, and finishing with components at transistor-level. The SC converter is completely designed, so the next step is implement the layout of a test chip to verify the correct performance of the converter designed.
Bibliography


Appendices
1. Topologies study

Section 1. Input to Output Ratio selection

To determine the circuit architecture that is going to be implemented in the converter, it is necessary to determine first the input-to-output voltage-ratio parameter M. This parameter can only take certain values depending on the number of floating capacitors, as is shown in Table 2.1. The equations (2.1) an (2.2), obtained from the equivalent model of a SC DC-DC converter, determine that the maximum power efficiency, $\eta_{\text{max}}$, and the equivalent output resistance, $R_{\text{out}}$, depend directly from the conversion ratio. The next equations are obtained by replacing the voltage and current variables with the values given in the specifications of the converter:

$$\eta_{\text{max}} = \frac{V_o}{M \cdot V_{\text{in}}} = \frac{3.3 \, V}{M \cdot 20 \, V}$$  \hspace{1cm} (A1.1)

$$R_{\text{out}} = \frac{M \cdot V_{\text{in}} - V_o}{I_o} = \frac{M \cdot 20 \, V - 3.3 \, V}{5 \, mA}$$  \hspace{1cm} (A1.2)

From the obtained equations for $\eta_{\text{max}}$ and $R_{\text{out}}$, the possible ratios M that can be used to achieve the required specifications are computed and shown in Table A1.1:

<table>
<thead>
<tr>
<th>Ratio (M)</th>
<th>$\eta_{\text{max}}$</th>
<th>$R_{\text{out}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\frac{1}{6}$</td>
<td>99 %</td>
<td>6.7 Ω</td>
</tr>
<tr>
<td>$\frac{1}{5}$</td>
<td>82.5 %</td>
<td>140 Ω</td>
</tr>
<tr>
<td>$\frac{1}{4}$</td>
<td>66 %</td>
<td>340 Ω</td>
</tr>
<tr>
<td>$\frac{2}{7}$</td>
<td>57.75 %</td>
<td>482 Ω</td>
</tr>
</tbody>
</table>

Table A1.1. M ratio study table

The output resistance ($R_{\text{out}}$) is inversely proportional to the switching frequency ($f_s$) of the converter and to the size of the capacitors, as can be deducted from (2.3). Therefore, the ratio $1/6$ was discarded because with a $R_{\text{out}}$ so low, the $f_s$ and the capacitors should be significantly big, increasing the switching losses and the area, and reducing the efficiency. On the other side, the efficiency showed at Table A1.1 is the theoretical maximum efficiency that could be obtained with each ratio, so, if the switching and bottom plate losses are taken into account, the real efficiency of the ratios $1/4$ and $2/7$ would be lower than the efficiency in the specifications. After discarding all the other results, the ratio that fits better for the converter is $M=1/5$. 
Section 2. Topology selection

With a conversion ratio of 1/5 and applying the specifications of the converter at (2.2), the required output resistance is $R_{\text{out}} = 140 \, \Omega$. The output resistance can be approximated by (2.3), where $R_{\text{FSL}}$ and $R_{\text{SSL}}$, (2.4) and (2.5), represent the asymptotic values of the Fast-Switching Limit (FSL) and the Slow-Switching Limit (SSL) shown in Figure 2.4 (a). For $R_{\text{SSL}} > R_{\text{FSL}}$, the capacitors and the switching frequency can be smaller but the switches need to be bigger in order to reduce the $R_{\text{ON}}$ resistance. On the other side, for $R_{\text{SSL}} < R_{\text{FSL}}$, the switches would be smaller but the capacitor and the switching frequency should be higher to obtain the same output impedance. The optimum situation is at the crossing point of SSL and FSL limit, where $R_{\text{out}}$ is set to its minimum value for the lowest switching frequency, which is good compromise between the efficiency and the output power capability. Thus, from (2.3) is obtained that:

$$R_{\text{FSL}} = R_{\text{SSL}} = 70 \sqrt{2} \, \Omega$$

With a ratio of 1/5, the converter topology that is going to be implemented must has, at least, three or more floating capacitors, as is shown in Table 2.1. Figure A1.1 shows three possible topologies of SC DC-DC power converters with a conversion factor $M=1/5$. The three of them have different switches configuration and different number of capacitors and transistors, but all of them have the same ratio conversion, so they are the perfect example that for the same conversion ratio different topologies exist.

![Figure A1.1. Proposed SC topologies for $M=1/5$: (a) Series-Parallel (b) Fibonacci (c) 4C1M5](image)

With a ratio of 1/5, the converter topology that is going to be implemented must has, at least, three or more floating capacitors, as is shown in Table 2.1. Figure A1.1 shows three possible topologies of SC DC-DC power converters with a conversion factor $M=1/5$. The three of them have different switches configuration and different number of capacitors and transistors, but all of them have the same ratio conversion, so they are the perfect example that for the same conversion ratio different topologies exist.
The three topologies presented in Figure A1.1 can be implemented on this project, so is necessary to make a deep study to know which one is the best. The study is focused on the parameters $m$ and $p$ of the equations (2.4) and (2.5): the slow-switching limit resistance equation ($R_{SSL}$) and the fast-switching limit resistance equation ($R_{FSL}$). These two parameters are constants that depend on the topology of the converter, even when they provide the same conversion ratio $M$. The parameter $m$ depends on the charge that pass through the capacitors, while the parameter $p$ depends on the charge that pass through the transistors when they are in conduction.

Following the procedure explained at [9], the $m$ and $p$ values of each topology are calculated and presented in Table A1.2:

<table>
<thead>
<tr>
<th>Topology</th>
<th>$m$</th>
<th>$p$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Series-Parallel</td>
<td>0.64</td>
<td>2.16</td>
</tr>
<tr>
<td>Fibonacci</td>
<td>0.64</td>
<td>1.04</td>
</tr>
<tr>
<td>4C1M5</td>
<td>0.32</td>
<td>1.04</td>
</tr>
</tbody>
</table>

Table A1.2. $m$ and $p$ parameters study

The parameter $m$ is a multiplier of the inverse of the product of the switching frequency ($f_s$) and the total capacitance of the floating capacitors ($C_T$), as can be seen in (2.5). The $f_s$ and the $C_T$ are directly proportional to the switching losses and the area of the converter, respectively. Thus, for a small value of $m$, less switching losses will be produced and smaller capacitors could be implemented, reducing the total area of the converter. In the same way, at (2.4) is presented that the parameter $p$ is a multiplier of the impedance of the transistors when they are in conduction ($R_{on}$). The $R_{on}$ is at the same time inversely proportional to the width (W) of the transistor. Therefore, if $p$ is reduced, the size of the transistors will be also reduced, reducing the occupied area by the transistors. Thus, the 4C1M5 is the topology chosen for this project because it has the lowest $m$ and $p$ values.
2. Design and Implementation of Capacitors for SCPC

Four types of integrated capacitors were available for the proposed design. The Table A2.1 shows the different characteristics of these capacitors. Each one of the four technologies presented has a limit breaking down voltage that, if it is overpassed, the capacitor would be damaged. The capacitors of the proposed design, showed at Figure 3.1 (a), must withstand: $C_1=16$ V, $C_2=8$ V, $C_3=12$ V and $C_4=4$ V. With these voltage limits, the capacitors $C_1$, $C_2$ and $C_3$ have to be designed with Fringe Capacitors (FC) technology, while $C_4$ can be designed with GO3 or FC.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Voltage rating (V)</th>
<th>Capacity density (nF/mm$^2$)</th>
<th>Parasitic (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GO1</td>
<td>1.8</td>
<td>9</td>
<td>2.6</td>
</tr>
<tr>
<td>GO2</td>
<td>3.3</td>
<td>4.8</td>
<td>5</td>
</tr>
<tr>
<td>GO3</td>
<td>5</td>
<td>2.7</td>
<td>8.8</td>
</tr>
<tr>
<td>Fringe Capacitors</td>
<td>20</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table A2.1. Integrated capacitors characteristics

An easy way to design the capacitors and the switching frequency is by applying the values of $m$ and $R_{SSL}$ obtained at Appendix 1, on equation (2.5), and make approximations with the different technologies. That is why for this project it is developed an equation to find the optimum switching frequency as function of the technology of the capacitors, obtaining the minimum switching losses and optimizing the area used by the capacitors.

The reference [9] develops the equation (A2.1) to calculate the slow-switching resistance limit, where $q_i$ is the charge that pass through the capacitors in the two phases. This equation considers that all the capacitors are designed with the same technology.

$$R_{SSL} = \frac{1}{C_T \cdot f_s} \left( \sum_{i} |q_i| \right)^2 \quad (A2.1)$$

The value of $C_T$ is the sum of the floating capacitors of the converter, and each capacitor is given as the product of its area and the technology density (for this explanation $C_4$ is considered GO3). From (A2.1) and applying that different technologies are used, the $R_{SSL}$ equation is obtained as function of the four capacitors:

$$R_{SSL} = \frac{1}{f_s} \cdot \left[ \frac{q_1^2}{C_1} + \frac{q_2^2}{C_2} + \frac{q_3^2}{C_3} + \frac{q_4^2}{C_4} \right] \quad (A2.2)$$

The optimum way to split the area is by designing the capacitors of same technology with the same size. This is because, in this topology, the charges $q_i$ of each capacitor are the same. Using the parameter $x$ as the ratio between the total area occupied by the capacitors and the area of one FC capacitor, the areas for each of them can be expressed as is shown in (A2.3):

$$A_{C_1} = A_{C_2} = A_{C_3} = xA_T \quad ; \quad A_{C_4} = (1 - 3x)A_T \quad (A2.3)$$
Therefore, the capacitors values as a function of the different technologies and area are shown in (A2.4):

\[ C_1 = C_2 = C_3 = x \cdot A_T \cdot \delta_{FC} \quad ; \quad C_4 = (1 - 3x) \cdot A_T \cdot \delta_{GO3} \quad (A2.4) \]

Finally, (A2.4) is applied to (A2.1) to obtain the switching frequency equation as a function of the capacitors parameters:

\[ f_s = \frac{1}{A_T R_{SSL}} \left[ \frac{3q_1^2}{\delta_{FC}} \cdot \frac{1}{x} + \frac{q_4^2}{\delta_{GO3}} \cdot \frac{1}{1 - 3x} \right] \quad (A2.5) \]

The relative extremes procedure is applied to this formula with the objective of find the minimum switching frequency with an optimum capacitor sizing. The total area of the chip must be 0.75 mm², as is presented at the specifications, so the total area for the integrated capacitors is decided to be 0.6 mm². Once all the parameters are known, the results for the two different C₄ options are shown in Table A2.2 and Table A2.3:

<table>
<thead>
<tr>
<th>Technology</th>
<th>Area (mm²)</th>
<th>Capacitance (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C₄</td>
<td>FC</td>
<td>0.166</td>
</tr>
<tr>
<td></td>
<td>GO3</td>
<td>0.1</td>
</tr>
</tbody>
</table>

\[ f_s = 8.16 \text{ MHz} \]

Table A2.2. Capacitors and \( f_s \) optimized values for C₄ as GO3

<table>
<thead>
<tr>
<th>Technology</th>
<th>Area (mm²)</th>
<th>Capacitance (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C₄</td>
<td>FC</td>
<td>0.15</td>
</tr>
<tr>
<td></td>
<td>FC</td>
<td>0.15</td>
</tr>
</tbody>
</table>

\[ f_s = 10.77 \text{ MHz} \]

Table A2.3. Capacitors and \( f_s \) optimized values for C₄ as FC

With the obtained results, is necessary to check the characteristics of the technologies to determine which one must be chosen, because the results of the tables are quite equal, without showing any big advantage of one technology over the other.

As is explained in section 2.2, the SC converters are quite sensitive to the bottom plate losses due to the presence of floating capacitors, and in this case, the parasitic losses of the GO3 technology are significantly larger. So, in regard of the smaller bottom plate parasitic losses, Fringe Capacitors offer the best choice even though the smaller capacitance density.
3. Design and Implementation of Power Switches for SCPC

Section 1. Transistors design

The main difficulty of the transistors design is the high input voltage of the converter. The native transistors of the technology have a break down voltage around 1.8 V and 3.3 V, but with the high input voltage transistors with a higher break down voltage are needed. The proposed converter, with the minimum and maximum node voltages of each phases in green, is shown in Figure A3.1. The voltages in the figure are calculated with assumption of no-load condition and ideal switches.

![Converter Diagram](image)

**Figure A3.1. Maximum voltage conditions for the converter**

It can be seen that SW6, SW7 and SW9 have a maximum voltage of 8V across them in the phase in which they are off. For this reason, some special technologies are needed. The different types of transistors available, with their maximum drain-to-source break down voltage, are presented in Table A3.1.

<table>
<thead>
<tr>
<th>Switches technologies</th>
<th>GO1</th>
<th>GO2</th>
<th>GO3</th>
<th>EXT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Voltage</td>
<td>1.8 V</td>
<td>3.3 V</td>
<td>5 V</td>
<td>16 V</td>
</tr>
</tbody>
</table>

**Table A3.1. Break down voltages of transistors' technologies**

A part from the technology, also the transistor type must be chosen: NMOS or PMOS. The NMOS transistors are used more often than the PMOS because they have smaller size for the same on-resistance. This choice also depends on the drive voltage, because in some cases the drive voltage is easier to generate if the transistor is PMOS, or the drive voltage of other transistors can be used. Table A3.2 shows the technology chosen for each switch and their gate drive voltages to switch-on or switch-off the transistors.
Once the transistors implementation is decided, their parameters must be designed according the $P$ and $R_{FSL}$ values obtained in Appendix 1 section 2. With those values and the equation (2.4), it is found that the on-resistances of each MOS transistors for the proposed converter is:

$$R_{ON}=95.12 \, \Omega$$

The design parameters of the transistors are the width ($W$) and the length ($L$). The $R_{ON}$ value depends directly from the quotient $L/W$. The on-resistance is big for the minimum values of $W$ and $L$, hence it is decided to fix the length to its minimum value and modify the $W$ to obtain the desired $R_{ON}$. Table A3.3 shows the widths of the different technologies and MOS types for the $R_{ON}$ calculated.

<table>
<thead>
<tr>
<th>SW Technology</th>
<th>MOS Topology</th>
<th>Widths for $R_{ON}=95.12 , \Omega$ (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXT</td>
<td>N</td>
<td>52</td>
</tr>
<tr>
<td></td>
<td>P</td>
<td>148.2</td>
</tr>
<tr>
<td>GO3</td>
<td>N</td>
<td>21.4</td>
</tr>
<tr>
<td></td>
<td>P</td>
<td>50.87</td>
</tr>
<tr>
<td>GO2</td>
<td>N</td>
<td>15.96</td>
</tr>
<tr>
<td></td>
<td>P</td>
<td>37.53</td>
</tr>
</tbody>
</table>

Table A3.3. Widths of the transistors for $R_{ON}=95.12 \, \Omega$
Section 2. Switching losses optimization

The widths of the Table A3.3 are designed in order to have all the transistors with the same on-resistance, but the method used to calculate the widths does not take into account that depending on the location and the driving voltages, each transistor has different power consumption. The power consumption are the switching losses, and they depend directly on the widths of the transistor and the voltage swings around them. Therefore, the switching losses must be optimized as a function of the widths of the transistors and the position of the different switches in the circuit.

To optimize the switching losses is used the ‘fmincon’ function from Matlab. It searches the minimum value of a given equation as a function of some variables. When the function is executed, it begins to iterate, modifying the value of each variable at each step, trying to obtain the minimum result. In this case, the variables used for the minimization of the switching losses are the widths of the transistors.

At (A3.1) is shown the proposed equation of the switching losses, extrapolated from (2.10). For each transistor, the switching losses are modeled as the power required to drive the switches, and this power is normalized with the widths obtained in Table A3.3 for an on-resistance of 95.12 Ω. The power is expressed as the product of the driving voltage (\(V_{oi}\)) and driving current (\(I_{oi}\)), and the normalization is used to determine that for higher widths the consumption is increased, and for smaller widths it is the opposite.

\[
P_{sw} = \sum_i V_{oi} \cdot I_{oi} \cdot \frac{W_i}{W_{oi}}
\]

(A3.1)

To minimize the switching losses is also needed a boundary equation to determine which are the optimum values of the width variable. The boundary equation used is the \(R_{FSL}\) expression developed at [9] and presented at (A3.2):

\[
R_{FSL} = 2 \cdot \sum_i |q_i|^2 \cdot R_{ONi}
\]

(A3.2)

The \(q_i\) parameter represents the charge that flows through each switch when they are ON. In the proposed SC converter topology, all the switches have the same charge. At [9] is considered that all the transistors have the same \(R_{ON}\), but for this optimization the on-resistance values are modified to obtain the minimum switching losses, and still result in the same total value of \(R_{FSL}\). At (A3.3) is presented the formula of \(R_{FSL}\) under the conditions described, where the on-resistances are normalized with the widths of Table A3.3:

\[
R_{FSL} = 2 \cdot q^2 \cdot \sum_i \left( R_{ONi} \cdot \frac{W_i}{W_{oi}} \right)
\]

(A3.3)

With the optimizing equation (A3.1) and the boundary equation (A3.3), the switching losses are optimized using the function ‘fmincon’ of Matlab. The used driving voltage values (\(V_{oi}\)) are the difference between the on and off switching voltages shown in Table A3.2, the on-switching driving current (\(I_{oi}\)) are obtained from the simulation mentioned before, and the \(W_{oi}\) values are the widths presented at Table A3.3. With these parameters, the optimization function is done. The widths values of the switches for \(R_{ON}=95.12\ \Omega\) and the ones obtained with the switching losses optimization are presented in Table A3.4.
### Table A3.4. $R_{ON}=95.12\Omega$ widths and optimized widths for 5mA

<table>
<thead>
<tr>
<th>Switch</th>
<th>Widths for $R_{ON}=95.12\Omega$ (µm)</th>
<th>Optimized widths (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW1</td>
<td>50.87</td>
<td>53.46</td>
</tr>
<tr>
<td>SW2</td>
<td>15.96</td>
<td>26.39</td>
</tr>
<tr>
<td>SW3</td>
<td>37.53</td>
<td>54.75</td>
</tr>
<tr>
<td>SW4</td>
<td>15.96</td>
<td>26.47</td>
</tr>
<tr>
<td>SW5</td>
<td>37.53</td>
<td>55.54</td>
</tr>
<tr>
<td>SW6</td>
<td>52</td>
<td>28.83</td>
</tr>
<tr>
<td>SW7</td>
<td>148.2</td>
<td>59.29</td>
</tr>
<tr>
<td>SW8</td>
<td>21.4</td>
<td>25.69</td>
</tr>
<tr>
<td>SW9</td>
<td>52</td>
<td>29.1</td>
</tr>
<tr>
<td>SW10</td>
<td>15.96</td>
<td>26.48</td>
</tr>
<tr>
<td>SW11</td>
<td>37.53</td>
<td>55.77</td>
</tr>
<tr>
<td>SW12</td>
<td>37.53</td>
<td>55.36</td>
</tr>
<tr>
<td>SW13</td>
<td>15.96</td>
<td>26.57</td>
</tr>
</tbody>
</table>

In each iteration of the Matlab function, the widths of the switches are modified to obtain the smallest switching losses. Figure A3.2 shows how the switching losses are reduced through the different iterations till arrive to the optimum widths values where the switching losses are minimum.

In section 3.1, it is explained that the switching frequency and the output resistance of the converter should be chosen around the midpoint between the Slow-Switching Limit and the Fast-Switching Limit from Figure 2.1. At that midpoint, it is obtained a $R_{FSL}=70\sqrt{2}$ Ω and an on-resistance value of 95.12 Ω for each transistor. With the optimization, the on-resistance value of all the transistors is modified, but their non-linear combination still provides the required $R_{FSL}$. 
4. Control Strategies

The three controls discarded for the SC converter are compiled in this appendix. For each control strategy, there is a brief explanation of its performance, accompanied by the block diagram.

Continuous Time Control

This control is composed by two blocks. The first one is responsible of comparing the output voltage ($V_O$) with a reference voltage, using a continuous time comparator. The second block is composed by five state-machines, where their outputs are the inputs of the non-overlapping blocks of the converters.

The performance of the control is the following: when $V_O> V_{ref}$, the state-machines output will be constant, so the non-overlapping circuits will not generate the clocks signals required by the SC converter. Therefore, the output voltage will decrease because the converter will remain frozen. On the other hand, when $V_O<V_{ref}$, the state-machines will generate five clock signals with the switching frequency required by the SC converter till $V_O$ rises again above $V_{ref}$. In order to achieve this operation, the second block requires an oscillator with a frequency $f_d=2f_s$ to drive the state-machines.

The block diagram of this converter is shown in Figure A4.1. This converter is not chosen because the continuous time comparator has a high power consumption and this reduces significantly the efficiency.

![Figure A4.1. Continuous Time Control](image-url)
Ring Oscillator Enable Control

As is shown in Figure A4.2, this control is composed by a clocked comparator and a ring oscillator. The clock comparator works as the continuous time comparator explained in the previous control, but this one just compares at the falling edge and then it shows the result at the rising edge. The output of the comparator is connected to the enable of the ring oscillator, so, when $V_O > 3.3 \text{ V}$, the oscillator signals will remain constant, and when $V_O < 3.3 \text{ V}$, the oscillator will be activated and the clock signals will drive the converter.

![Figure A4.2. Ring Oscillator Enable Control](image)

The problem of this comparator is when the enable is deactivated: the five oscillating signals, instead of being switched off at the same time, they are deactivated in order with an out of phase between them, so this control is not fast enough to stop the power stage performance before the $V_O$ rises too much.

This problem cannot be solved neither by implementing all the stages of the ring oscillator with NAND gates instead of inverters, because when the enable is activated, the ring oscillator requires a period of time to stabilize the clock signals with the correspondent out of phases.

Pulse Frequency Modulation (PFM)

By controlling the frequency of the clock pulse in SC converters, the injection of power from the converter to the output can be controlled. As is shown in Figure 4.3, a difference block to adapt the output voltage and a Voltage Control Oscillator (VCO) compose the PFM control. The VCO is the main part of this control strategy because, depending on its input voltage, the frequency of its output clock signal will be modified, as is shown in Figure A4.4. If the output voltage is higher than the voltage reference, the frequency of the output clock signal of the VCO will decrease in order to reduce the injection power to the output. On the other side, the frequency is increased when the output voltage is lower than the reference with the objective of raises the output voltage by injecting power to the output more often.
Figure A4.3. PFM control blocks diagram

Figure A4.4. PFM control signals representation
## Glossary

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-DC</td>
<td>Direct Current to Direct Current</td>
</tr>
<tr>
<td>FC</td>
<td>Fringe Capacitors</td>
</tr>
<tr>
<td>FSL</td>
<td>Fast-Switching Limit</td>
</tr>
<tr>
<td>LDO</td>
<td>Low-Dropout Regulator</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>PFM</td>
<td>Pulse Frequency Modulation</td>
</tr>
<tr>
<td>SC</td>
<td>Switched-Capacitor</td>
</tr>
<tr>
<td>SM</td>
<td>State-Machine</td>
</tr>
<tr>
<td>SSL</td>
<td>Slow-Switching Limit</td>
</tr>
<tr>
<td>SW</td>
<td>Switch</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Control Oscillator</td>
</tr>
</tbody>
</table>